CMOS
DATABOOK

NATIONAL
SEMICONDUCTOR
CORPORATION

CMOS DATABOOK

Introduction

This Databook contains information on National Semiconductor's standard SSI/MSI CMOS products. This includes the popular 54C/74C series logic family, which is pin for pin, function for function equivalent to the 7400 family of TTL devices. All device outputs are LPTTL compatible, capable of sinking more than 360μA (≈1 LSTTL load). The AC parameters are specified with a 50pF capacitive load.

In addition this book describes National Semiconductor's extensive line of CD40XXB and CD45XXB series devices. These parts meet the standard JEDEC "B-Series" specifications.

Special Function, LSI, A/D Converters and Memory device specifications contained herein offer the designer unique high density low power system solutions. All devices are compatible with 54C/74C series and CD4XXB series products.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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CMOS Microprocessor and Support Circuits

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NSC800 High Performance Low Power Microprocessor
NSC810 RAM-I/O-Timer
NSC830 ROM-I/O
NSC831 I/O

MOS/LSI CMOS Circuits

(see MOS/LSI Databook for data sheets.)

MM5368 Oscillator Divider 32 kHz to 50 or 60 Hz & 1 & 10 Hz Output
MM5369AA Oscillator/Divider 3.58 MHz to 60 Hz
MM5369EST Oscillator/Divider 3.58 MHz to 100 Hz
MM5369EYR Oscillator/Divider 3.58 MHz to 50 Hz
MM5393 Push Button Pulse Dialer
MM5494 Push Button Pulse Dialer
MM5395 DTMF (Touch Tone®) Generator
MM53100 Programmable TV Timer
MM53105 Programmable TV Timer
MM53107AA Oscillator/Divider 2.097152 MHz to 60 Hz
MM53107FDU Oscillator/Divider 2.097152 MHz to 60 Hz
MM53125 DTMF (Touch Tone) Generator
MM53130 DTMF (Touch Tone) Generator
MM53143 Push Button Pulse Dialer
MM53144 Push Button Pulse Dialer
MM53190 Push Button Pulse Dialer
MM5452 32-Segment LCD Display Controller (Serial Input)
MM5453 33-Segment LCD Display Controller (Serial Input)
MM55108 PLL Frequency Synthesizer
MM55110 PLL Frequency Synthesizer
MM55121 PLL Frequency Synthesizer
MM55122 PLL Frequency Synthesizer
MM55123 PLL Frequency Synthesizer
MM55126 PLL Frequency Synthesizer
MM5840 TV Channel Number/Time Display
MM58106 Digital Clock/TV Channel Display
MM58143 LCD Clock Radio
MM58144 LCD Travel Alarm Clock
MM58167 μP Real Time Clock
MM58174 μP Real Time Clock
MM58183 LCD Clock Radio
MM58184 LCD Travel Alarm Clock
MM58201 Multiplexed LCD Matrix Display Driver
MM58313 TV Varactor Tuner Display

CMOS Product Guide

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NOR Gates

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Analog to Digital Converters

54C/74C Family Characteristics Guide

Typical Characteristics $T_A = 25°C$

Device Type/Description	C_{PD} (pF) (Note 3)	t_{PD} (ns) $C_L = 50\,pF$, $V_{CE} = 5V$	Δt_{PD} Curve	FANOUT		
				LP	LS	TTL
MM54C00/MM74C00 Quad 2-Input NAND Gate	12	50	A	2	1	—
MM54C02/MM74C02 Quad 2-Input NOR Gate	12	50	A	2	1	—
MM54C04/MM74C04 Hex Inverter	12	50	A	2	1	—
MM54C08/MM74C08 Quad 2-Input AND Gate	14	80	A	2	1	—
MM54C10/MM74C10 Triple 3-Input NAND Gate	18	60	A	2	1	—
MM54C14/MM74C14 Hex Schmitt Trigger	20	220	A	2	1	—
MM54C20/MM74C20 Dual 4-Input NAND Gate	30	70	A	2	1	—
MM54C30/MM74C30 8-Input NAND Gate	26	125	A	2	1	—
MM54C32/MM74C32 Quad 2-Input OR Gate	15	80	A	2	1	—
MM54C42/MM74C42 BCD-to-Decimal Decoder	50	200	A	2	1	—
MM54C48/MM74C48 BCD-to-7-Segment Decoder	NA	450(1)	NA	2	1	—
MM54C73/MM74C73 Dual J-K Flip-Flops	40	180	A	2	1	—
MM54C74/MM74C74 Dual D Flip-Flop	40	180	A	2	1	—
MM54C76/MM74C76 Dual J-K Flip-Flops	40	180	A	2	1	—
MM54C83/MM74C83 4-Bit Binary Full Adder	120	300	A	2	1	—
MM54C85/MM74C85 4-Bit Magnitude Comparator	45	220	A	2	1	—
MM54C86/MM74C86 Quad 2-Input	20	110	A	2	1	—
MM54C89/MM74C89 64-Bit RAM	230	270	A	2	1	—
MM54C90/MM74C90 4-Bit Decade Counter	45	400	A	2	1	—
MM54C93/MM74C93 4-Bit Binary Counter	45	400	A	2	1	—
MM54C95/MM74C95 4-Bit Shift Register	100	200	A	2	1	—
MM54C107/MM74C107 Dual J-K Flip-Flops	40	180	A	2	1	—
MM54C150/MM74C150 16-Line to 1-Line Multiplexer	100	250	A	10	5	1
MM54C151/MM74C151 8-Channel Digital Multiplexer	50	200(1)	A	2	1	—
MM54C154/MM74C154 4-16 Decoder/Demultiplexer	60	275(1)	A	2	1	—
MM54C157/MM74C157 Quad 2-Input Multiplexer	20	150(1)	A	2	1	—
MM54C160/MM74C160 Decade Counter	95	250(2)	A	2	1	—
MM54C161/MM74C161 Binary Counter	95	250(2)	A	2	1	—
MM54C162/MM74C162 Decade Counter	95	250(2)	A	2	1	—
MM54C163/MM74C163 Binary Counter	95	250(2)	A	2	1	—
MM54C164/MM74C164 8-Bit Shift Register	140	230(2)	A	2	1	—
MM54C165/MM74C165 8-Bit Shift Register	55	210(2)	A	2	1	—
MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop	100	220(2)	A	2	1	—
MM54C174/MM74C174 Hex D Flip-Flop	95	150(2)	A	2	1	—
MM54C175/MM74C175 Quad D Flip-Flop	130	190(2)	A	2	1	—
MM54C192/MM74C192 Decade Up/Down Counter	100	250(2)	A	2	1	—
MM54C193/MM74C193 Binary Up/Down Counter	100	250(2)	A	2	1	—
MM54C195/MM74C195 4-Bit Register	130	200(2)	A	2	1	—
MM54C200/MM74C200 256-Bit RAM	400	850	A	2	1	—
MM54C221/MM74C221 Dual Monostable Multivibrator	NA	250	A	2	1	—
MM54C240/MM74C240 Octal Buffers	100	60	B	13	6	1
MM54C244/MM74C244 Octal Buffers	100	45	B	13	6	1
MM54C373/MM74C373 Octal Latch	200	165	B	10	5	1
MM54C374/MM74C374 Octal D-Type Flip-Flop	250	165	B	10	5	1
MM54C901/MM74C901 Hex Inverting TTL Buffer	30	38	B	2	1	—
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer	50	57	B	2	1	—
MM54C903/MM74C903 Hex Inverting PMOS Buffer	30	57	B	2	1	—
MM54C904/MM74C904 Hex Non-Inverting PMOS Buffer	50	38	B	2	1	—
MM54C905/MM74C905 12-Bit SAR	100	200	A	2	1	—
MM54C906/MM74C906 Hex Open Drain Buffer	30	NA	NA	2	1	—
MM54C907/MM74C907 Hex Open Drain Buffer	30	NA	NA	2	1	—
MM74C908 Dual CMOS 30 Volt Driver	NA	150	NA	NA	NA	NA
MM54C914/MM74C914 Hex Schmitt Trigger	20	220	A	2	1	—
MM54C915/MM74C915 7-Segment-to-BCD Converter	NA	150	NA	10	5	1
MM54C918 Dual CMOS 30 Volt Driver	NA	60	B	NA	NA	NA
MM54C922/MM74C922 16-Key Encoder	NA	NA	B	2	1	—
MM54C923/MM74C923 20-Key Encoder	NA	NA	B	2	1	—

54C/74C Family Characteristics Guide (Cont'd.)

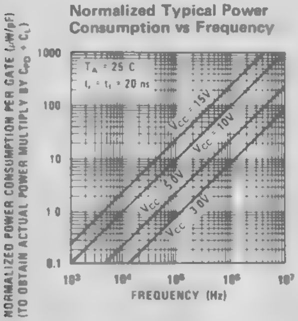
Typical Characteristics $T_A = 25°C$

Device Type/Description	C_{PD} (pF) (Note 3)	t_{PD} (ns) $C_L = 50\,pF$, $V_{CE} = 5V$	Δt_{PD} Curve	FANOUT		
				LP	LS	TTL
MM54C932/MM74C932 Phase Comparator	NA	NA	B	NA	NA	NA
MM54C941/MM74C941 Octal Buffer	100	70	B	13	6	1
MM70C95/MM80C95 TRI-STATE® Hex Buffers	60	60	B	10	5	1
MM70C96/MM80C96 TRI-STATE Hex Inverters	60	70	B	10	5	1
MM70C97/MM80C97 TRI-STATE Hex Buffers	60	60	B	10	5	1
MM70C98/MM80C98 TRI-STATE Hex Inverters	60	70	B	10	5	1
MM72C19/MM82C19 TRI-STATE 16–1 Multiplexer	100	250	A	10	5	1
MM78C29/MM88C29 Quad Single-Ended Line Driver	150	200	NA	NA	NA	NA
MM78C30/MM88C30 Dual Differential Line Driver	200	350	NA	NA	NA	NA

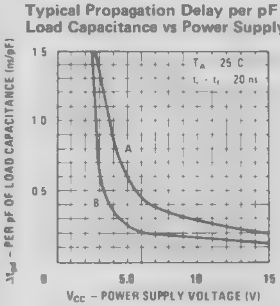
Note 1: t_{PD} shown is from data input to output. For more detailed specifications see individual data sheet.

Note 2: t_{PD} shown is from clock to output. For more detailed specifications see individual data sheet.

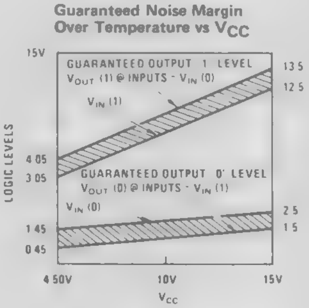
Note 3: C_{PD} numbers shown are for independent identical functions within a package. For instance the total C_{PD} for a MM74C157 is $4 \times 20\,pF = 80\,pF$ while the total C_{PD} for the MM74C173 is 100 pF because all flip-flops have a common clock.


Normalized Typical Power Consumption vs Frequency

TOTAL POWER = $V_{CC}^2 \times f \times (C_{PD} + C_L) + V_{CC}\,I_{LEAKAGE}$


Typical Propagation Delay per pF of Load Capacitance vs Power Supply

$t_{pd}\ \left|t_{pd}\right|_{C_L = C} = (C - 50)\,pF \times \frac{\Delta t_{pd}}{pF} + t_{pd}\Big|_{C_L = 50\,pF}$


Guaranteed Noise Margin Over Temperature vs V_{CC}

For complete explanation on use of curves see application note AN-90, 54C/74C Family Characteristics.

National Semiconductor's Megarad Radiation Hardened Product List

The following device types are currently available from National Semiconductor as a radiation hardened product to the 10^6 RADS (Si) level. These parts will be processed to National's 883S/RETS flow in the bottom braised flat (F) or side braised dual-in-line (D) packages.

RAD Hard CMOS

Device	Series	Device	Series	Device	Series	Device	Series	Device
CD4001	A/B	CD4019	B	CD4042	B	CD4075	B	MM54C04
CD4002	A	CD4020	A	CD4043	A	CD4076	B	MM54C14
CD4006	A	CD4021	A	CD4044	A	CD4081	B	MM54C86
CD4007	A	CD4022	B	CD4048	B	CD4093	B	MM54C173
CD4008	B	CD4023	A/B	CD4049	A	CD4099	B	MM54C174
CD4009	A	CD4024	B	CD4050	B	CD40106	B	MM54C192
CD4010	A	CD4025	A/B	CD4051	B	CD40174	B	MM54C193
CD4011	A	CD4027	B	CD4052	B	CD40192	B	MM54C200
CD4012	A	CD4028	B	CD4053	B	CD40193	B	MM54C901
CD4013	B	CD4029	B	CD4066	B	CD4514	B	MM54C902
CD4014	A	CD4030	A	CD4069	A	CD4515	B	MM54C903
CD4015	A	CD4031	B	CD4070	B	CD4518	B	MM54C904
CD4016	A	CD4035	B	CD4071	B	CD4520	B	MM54C906
CD4017	B	CD4040	A	CD4073	B	CD4584	B	MM54C907
CD4018	B	CD4041	A					

Cross Reference Guide

A Listing of CD4000 Series Parts that make up the National Semiconductor family, with competitor equivalents, for easy reference

Product	Description	RCA	Motorola	Fairchild
CD4000	Dual 3-Input NOR Gate Plus Inverter	CD4000	MC14000	—
CD4001	Quad 2-Input NOR Gate	CD4001	MC14001	—
CD4001B	Buffered Quad 2-Input NOR Gate	CD4001B	MC14001B	4001B
CD4002	Dual 4-Input NOR Gate	CD4002	MC14002	—
CD4002B	Dual Buffered 4-Input NOR Gate	CD4002B	MC14002B	—
CD4006B	18-Bit S/R	CD4006B	MC14006B	4006B
CD4007	Dual Complementary Pair Plus Inverter	CD4007	MC14007	4007
CD4008B	4-Bit Full Adder with Parallel Carry	CD4008B	MC14008B	4008B
CD4009	Hex Inverting Buffer	CD4009	—	—
CD4010	Hex Buffer	CD4010	—	—
CD4011	Quad 2-Input NAND Gate	CD4011	MC14011	4011
CD4011B	Buffered Quad 2-Input NAND Gate	CD4011B	MC14011B	4011B
CD4012	Dual 4-Input NAND Gate	CD4012	MC14012	—
CD4012B	Dual Buffered 4-Input NAND Gate	CD4012B	MC14012B	—
CD4013B	Dual D Flip-Flop	CD4013B	MC14013B	4013B
CD4014B	8-Bit S/R	CD4014B	MC14014B	4014B
CD4015B	Dual 4-Bit S/R	CD4015B	MC14015B	4015B
CD4016B	Quad Bilateral Switch	CD4016B	MC14016B	4016B
CD4017B	Decade Counter Divider	CD4017B	MC14017B	4017B
CD4018B	Presettable Divide by "N" Counter	CD4018B	MC14018B	4018B
CD4019B	Quad AND/OR Select Gate	CD4019B	—	4019B
CD4020B	14-Bit Ripple Carry Binary Counter/Divider	CD4020B	MC14020B	4020B
CD4021B	8-Bit S/R	CD4021B	MC14021B	4021B
CD4022B	Divide-by-8 Counter Divider	CD4022B	MC14022B	4022B
CD4023	Triple 3-Input NAND Gate	CD4023	MC14023	4023
CD4023B	Buffered Triple 3-Input NAND Gate	CD4023B	MC14023B	4023B
CD4024B	7-Bit Binary Counter	CD4024B	MC14024B	4024B
CD4025	Triple 3-Input NOR Gate	CD4025	MC14025	—
CD4025B	Double Buffered Triple 3-Input NOR Gate	CD4025B	MC14025B	4025B
CD4027B	Dual J-K Flip-Flop	CD4027B	MC14027B	4027B
CD4028B	BCD-to-Decimal Decoder	CD4028B	MC14028B	4028B
CD4029B	Presettable Up/Down Counter	CD4029B	MC14029B	4029B
CD4030	Quad EX-OR Gate (dual marked as MM74C86)	CD4030	MC14030	4030B
CD4031B	64-Bit S/R	CD4031B	MC14031B	—
CD4034B	8 Bit S/R	CD4034B	MC14034B	4034B
CD4035B	4-Bit P-In—P-Out S/R	CD4035B	MC14035B	4035B
CD4040B	12-Bit Binary/Ripple Counter	CD4040B	MC14040B	4040B
CD4041	Quad True/Complement Buffer	CD4041UB	—	4041B
CD4042B	Quad D Latch	CD4042B	MC14042B	4042B
CD4043B	Quad 3-State NOR R/S Latch	CD4043B	MC14043B	4043B
CD4044B	Quad 3-State NAND R/S Latch	CD4044B	MC14044B	4044B
CD4046B	Phase-Locked Loop	CD4046B	MC14046B	—
CD4047B	Monostable-Astable Multivibrator	CD4047B	—	4047B
CD4048B	Expandable 8-Input Gate	CD4048B	MC14048B	4048B
CD4049	Hex Inverting Buffer	CD4049UB	MC14049UB	4049B
CD4050B	Hex Buffer	CD4050B	MC14050B	4050B
CD4051B	Single 8-Channel Multiplexer	CD4051B	MC14051B	4051B
CD4052B	Differential 4-Channel Multiplexer	CD4052B	MC14052B	4052B
CD4053B	Triple 2-Channel Multiplexer	CD4053B	MC14053B	4053B
CD4060B	14-Stage Ripple Carry Binary Counter & Osc.	CD4060B	MC14060B	—
CD4066B	Quad Bilateral Switch	CD4066B	MC14066B	4066B
CD4069	Hex Inverter (dual marked as MM74C04)	CD4069UB	MC14069UB	4069

CD4070B	Quad Exclusive-OR Gate (dual marked as MM74C86)	CD4070B	MC14070B	4070B
CD4071B	Quad 2-Input OR Gate	CD4071B	MC14071B	4071B
CD4072B	Dual 4-Input OR Gate Buffered B Series	CD4072B	MC14072B	—
CD4073B	Triple 3-Input AND Gate	CD4073B	MC14073B	4073B
CD4075B	Triple 3-Input OR Gate	CD4075B	MC14075B	4075B
CD4076B	TRI-STATE® Quad D Flip-Flop (dual marked as MM74C173)	CD4076B	MC14076B	4076B
CD4081B	Quad 2-Input AND Gate	CD4081B	MC14081B	4081B
CD4082B	Dual 4-Input OR Gate Buffered B Series	CD4082B	MC14082B	—
CD4089B	Binary Rate Multiplier	CD4089B	—	—
CD4093B	Quad 2-Input NAND Schmitt Trigger	CD4093B	MC14093B	4093B
CD4099B	8-Bit Addressable Latch	CD4099B	MC14099B	4099B
CD40106B	Hex Schmitt Trigger (dual marked as MM74C14)	CD40106B	MC14584B	40014
CD40160B	Sync Decade Counter (dual marked as MM74C160)	CD40160B	MC14160B	—
CD40161B	Sync Binary Counter (dual marked as MM74C161)	CD40161B	MC14161B	40161B
CD40162B	Fully Sync Decade Counter (dual marked as MM74C162)	CD40162B	MC14162B	—
CD40163B	Fully Sync Binary Counter (dual marked as MM74C163)	CD40163B	MC14163B	40163B
CD40174B	Hex D Flip-Flop (dual marked as MM74C174)	CD40174B	MC14174B	40174B
CD40175B	Quad D Flip-Flop (dual marked as MM74C175)	—	MC14175B	40175B
CD40192B	Sync Up/Down Decade Counter (dual marked as MM74C192)	CD40192B	—	—
CD40193B	Sync Up/Down Binary Counter (dual marked as MM74C193)	CD40193B	MC140193B	40193B
CD4503B	Hex Bus Driver (dual marked as MM80C97)	CD4503B	MC14503B	40097
CD4510B	BCD Up/Down Counter	CD4510B	MC14510B	4510B
CD4511B	BCD-to-7 Segment Latch/Decoder/Driver	CD4511B	MC14511B	4511B
CD4512B	8-Channel Data Selector	CD4512B	MC14512B	4512B
CD4514B	4-Bit Latch/4 to 16 Line Decoder (High)	CD4514B	MC14514B	4514B
CD4515B	4-Bit Latch/4 to 16 Line Decoder (Low)	CD4515B	MC14515B	4515B
CD4516B	Binary Up/Down Counter	CD4516B	MC14516B	4516B
CD4518B	Dual BCD Up Counter	CD4518B	MC14518B	4518B
CD4519B	4-Bit AND/OR Selector	—	MC14519B	4519B
CD4520B	Dual Binary Up Counter	CD4520B	MC14520B	4520B
CD4522B	Programmable Divide-by-N Counter (BCD)	—	MC14522B	—
CD4526B	Programmable Divide-by-N Counter (Binary)	—	MC14526B	—
CD4527B	BCD Rate/Multiplier	CD4527B	MC14527B	—
CD4528B	Dual Retriggerable/Resettable Monostable Multivibrator	CD4528B	MC14528B	4528
CD4529B	Dual 4-Channel Analog Data Selector	—	MC14529B	—
CD4538B	Dual Monostable Multivibrator	—	MC14538	—
CD4541B	Programmable Oscillator Timer	—	MC14541B	—
CD4543B	BCD-to-7-Segment Decoder (LCD)	—	MC14543B	—
CD4584B	Hex Schmitt Trigger (marked as MM74C14N)	40106B	MC14584B	40014
CD4723B	Dual 4-Bit Addressable Latch	—	—	4723
CD4724B	8-Bit Addressable Latch	CD4724B	—	4724

A/D Converter Cross Reference Guide

Product	Description	T.I.	Mostek	
ADC0808CCN	8-Bit A/D w/8-Channel Analog Mux	ADC0808CN	MK50808N	
ADC0809CCN	8-Bit A/D w/8-Channel Analog Mux	ADC0809CN	MK50809N	
ADC0816CCN	8-Bit A/D w/16-Channel Analog Mux	ADC0816CN	MK50816N	
ADC0817CCN	8-Bit A/D w/16-Channel Analog Mux	ADC0817CN	MK50817N	

Specifications for "B" Series

National Semiconductor complies with the CMOS "B" Series specification as called out in JEDEC Standard No. 13A. All parts called out as "B" are double buffered and will meet as a minimum the electrical parameters listed in table A. As agreed upon in the JEDEC Spec, products callout out as "UB" are not double buffered but meet table A specifications with the exception of V_{IL} and V_{IH}, which will be 20% and 80%, respectively, of V_{DD}. **The 54C/74C family meets or exceeds the "B"/"UB" specifications as given in table A but are not marked "B"/"UB".**

Table A

					Limits							
					T_{LOW}*		+25°C			T_{HIGH}**		
	Parameter	Temp. Range	V_{DD} (Vdc)	Conditions	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Units
I_{DD}	Quiescent Device Current GATES	Mil.	5	$V_I = V_{SS}$ or V_{DD} All valid input combinations		0.25			0.25		7.5	μAdc
			10			0.5			0.5		15	
			15			1.0			1.0		30	
		Comm.	5			1.0			1.0		7.5	μAdc
			10			2.0			2.0		15	
			15			4.0			4.0		30	
	BUFFERS, FLIP-FLOPS	Mil.	5	$V_I = V_{SS}$ or V_{DD} All valid input combinations		1.0			1.0		30	μAdc
			10			2.0			2.0		60	
			15			4.0			4.0		120	
		Comm.	5			4.0			4.0		30	μAdc
			10			8.0			8.0		60	
			15			16			16		120	
	MSI	Mil.	5	$V_I = V_{SS}$ or V_{DD} All valid input combinations		5.0			5.0		150	μAdc
			10			10			10		300	
			15			20			20		600	
		Comm.	5			20			20		150	μAdc
			10			40			40		300	
			15			80			80		600	
V_{OL}	Low-Level Output Voltage	All	5	$V_I = V_{SS}$ or V_{DD} $\|I_O\| < 1\,\mu A$		0.05			0.05		0.05	Vdc
			10			0.05			0.05		0.05	
			15			0.05			0.05		0.05	
V_{OH}	High-Level Output Voltage	All	5	$V_I = V_{SS}$ or V_{DD} $\|I_O\| < 1\,\mu A$	4.95		4.95			4.95		Vdc
			10		9.95		9.95			9.95		
			15		14.95		14.95			14.05		
V_{IL}	Input Low Voltage	All	5	$V_O = 0.5\,V$ or $4.5\,V$, $\|I_O\| < 1\,\mu A$		1.5			1.5		1.5	Vdc
			10	$V_O = 1.0\,V$ or $9.0\,V$, $\|I_O\| < 1\,\mu A$		3.0			3.0		3.0	
			15	$V_O = 1.5\,V$ or $13.5\,V$, $\|I_O\| < 1\,\mu A$		4.0			4.0		4.0	
V_{IH}	Input High Voltage	All	5	$V_O = 0.5\,V$ or $4.5\,V$, $\|I_O\| < 1\,\mu A$	3.5		3.5			3.5		Vdc
			10	$V_O = 1.0\,V$ or $9.0\,V$, $\|I_O\| < 1\,\mu A$	7.0		7.0			7.0		
			15	$V_O = 1.5\,V$ or $13.5\,V$, $\|I_O\| < 1\,\mu A$	11		11			11		
I_{OL}	Output Low (Sink) Current	Mil.	5	$V_O = 0.4\,V$, $V_I = 0\,V$ or $5\,V$	0.64		0.51			0.36		mAdc
			10	$V_O = 0.5\,V$, $V_I = 0\,V$ or $10\,V$	1.6		1.3			0.9		
			15	$V_O = 1.5\,V$, $V_I = 0\,V$ or $15\,V$	4.2		3.4			2.4		
		Comm.	5	$V_O = 0.4\,V$, $V_I = 0\,V$ or $5\,V$	0.52		0.44			0.36		mAdc
			10	$V_O = 0.5\,V$, $V_I = 0\,V$ or $10\,V$	1.3		1.1			0.9		
			15	$V_O = 1.5\,V$, $V_I = 0\,V$ or $15\,V$	3.6		3.0			2.4		
I_{OH}	Output High (Source) Current	Mil.	5	$V_O = 4.6\,V$, $V_I = 0\,V$ or $5\,V$	−0.25		−0.2			−0.14		mAdc
			10	$V_O = 9.5\,V$, $V_I = 0\,V$ or $10\,V$	−0.62		−0.5			−0.35		
			15	$V_O = 13.5\,V$, $V_I = 0\,V$ or $15\,V$	−1.8		−1.5			−1.1		
		Comm.	5	$V_O = 4.6\,V$, $V_I = 0\,V$ or $5\,V$	−0.2		−0.16			−0.12		mAdc
			10	$V_O = 9.5\,V$, $V_I = 0\,V$ or $10\,V$	−0.5		−0.4			−0.3		
			15	$V_O = 13.5\,V$, $V_I = 0\,V$ or $15\,V$	−1.4		−1.2			−1.0		
I_I	Input Current	Mil.	15	$V_I = 0\,V$ or $15\,V$		±0.1			±0.1		±1.0	μAdc
		Comm.	15	$V_I = 0\,V$ or $15\,V$		±0.3			±0.3		±1.0	μAdc
C_I	Input Capacitance per Unit Load	All	—	Any Input					7.5			pF

Note: For current flow the convention is positive for current flowing into the device and negative flowing out of the device.
*T_{LOW} = −55°C for Military Temp. Range device, −40°C for Commercial Temp. Range device.
**T_{HIGH} = +125°C for Military Temp. Range device, +85°C for Commercial Temp. Range device.

Section 1

MM54CXX/MM74CXX Series Logic

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

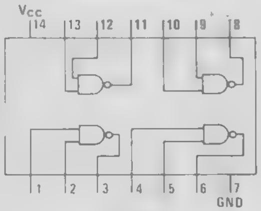
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power consumption	10 nW/package (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

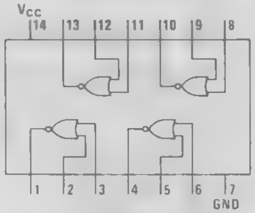
Connection Diagrams

MM54C00/MM74C00



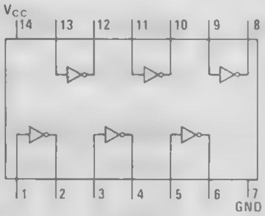
TOP VIEW

MM54C02/MM74C02



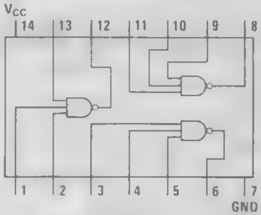
TOP VIEW

MM54C04/MM74C04



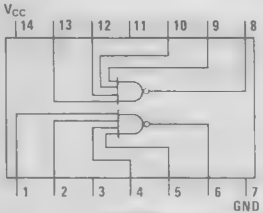
TOP VIEW

MM54C10/MM74C10



TOP VIEW

MM54C20/MM74C20



TOP VIEW

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
54C	−55°C to +125°C
74C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Operating V_{CC} Range	3.0V to 15V
Maximum V_{CC} Voltage	18V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
	Low Power to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-10\mu A$	4.4			V
		74C, $V_{CC}=4.75V$, $I_O=-10\mu A$	4.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+10\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=+10\mu A$			0.4	V
	CMOS to Low Power					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	4.0			V
		74C, $V_{CC}=4.75V$	4.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			1.0	V
		74C, $V_{CC}=4.75V$			1.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
	MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04					
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
C_{IN}	Input Capacitance	(Note 2)		6.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate or Inverter		12		pF
	MM54C10/MM74C10					
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		60	100	ns
		$V_{CC} = 10V$		35	70	ns
C_{IN}	Input Capacitance	(Note 2)		7.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		18		pF
	MM54C20/MM74C20					
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		70	115	ns
		$V_{CC} = 10V$		40	80	ns
C_{IN}	Input Capacitance	(Note 2)		9		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		30		pF

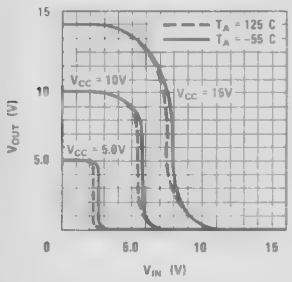
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

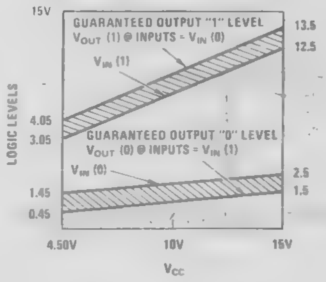
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

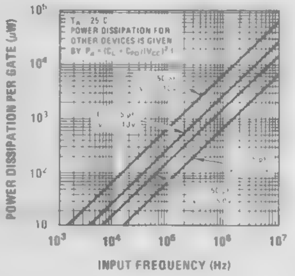
Gate Transfer Characteristics



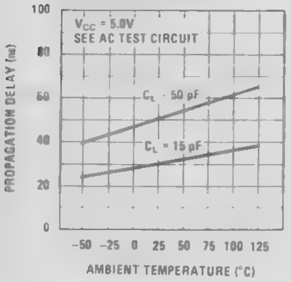
Guaranteed Noise Margin Over Temperature vs V_{CC}



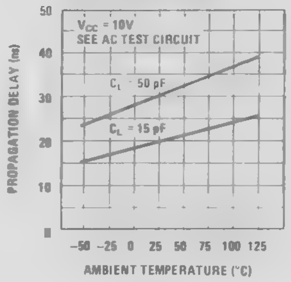
Power Dissipation vs Frequency
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04



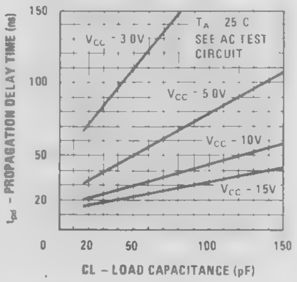
Propagation Delay vs Ambient Temperature
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04



Propagation Delay vs Ambient Temperature
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04

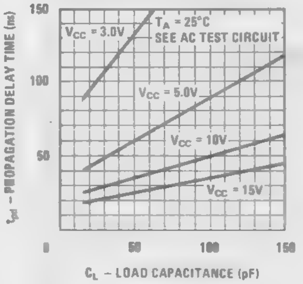


Propagation Delay Time vs Load Capacitance
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04

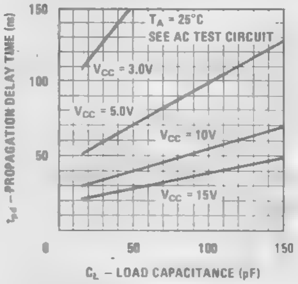


Typical Performance Characteristics (Cont'd)

Propagation Delay Time vs Load Capacitance MM54C10/MM74C10

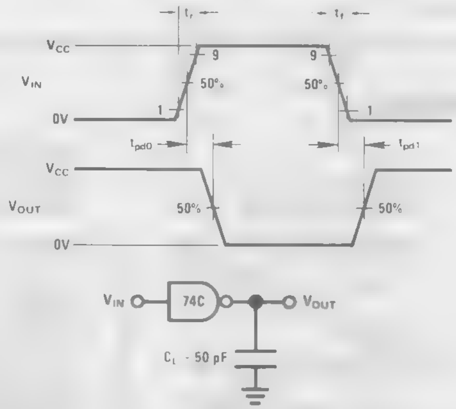


Propagation Delay Time vs Load Capacitance MM54C20/MM74C20



Switching Time Waveforms and AC Test Circuits

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT t_r, $t_f \leq 20$ ns.

MM54C08/MM74C08 Quad 2-Input AND Gate

General Description

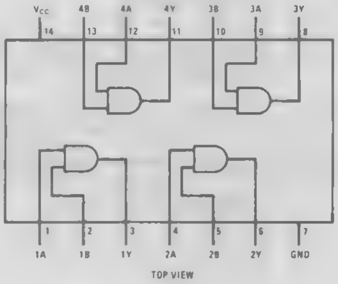
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	10 nW/package (typ.)

Connection Diagrams

MM54C08/MM74C08



Truth Tables

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level L= Low Level

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C08, MM54C86	−55°C to +125°C
MM74C08, MM74C86	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=+360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics

(MM54C08/MM74C08) $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		80	140	ns
		$V_{CC} = 10V$		40	70	ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		14		pF

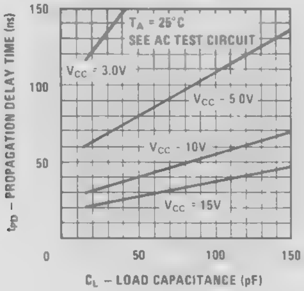
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

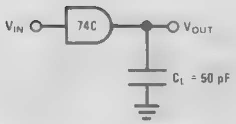
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C08/MM74C08

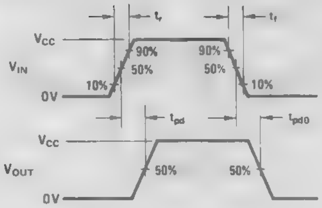


AC Test Circuits



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

Switching Time Waveforms



National Semiconductor

MM54C14/MM74C14 Hex Schmitt Trigger

General Description

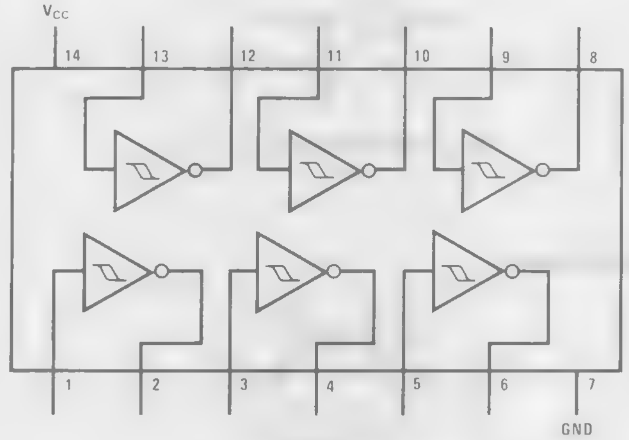
The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ. 0.0005 V/°C at $V_{CC} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geqslant 0.2V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} (typ.)
■ Low power TTL compatibility	0.4 V_{CC} (typ.) 0.2 V_{CC} guaranteed
■ Hysteresis	0.4 V_{CC} typ. 0.2 V_{CC} guaranteed

Connection Diagram



TOP VIEW

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C14	−55°C to +125°C
MM74C14	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
V_{T+}	Positive Going Threshold Voltage	$V_{CC} = 5V$	3.0	3.6	4.3	V
		$V_{CC} = 10V$	6.0	6.8	8.6	V
		$V_{CC} = 15V$	9.0	10.0	12.9	V
V_{T-}	Negative Going Threshold Voltage	$V_{CC} = 5V$	0.7	1.4	2.0	V
		$V_{CC} = 10V$	1.4	3.2	4.0	V
		$V_{CC} = 15V$	2.1	5.0	6.0	V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = 5V$	1.0	2.2	3.6	V
		$V_{CC} = 10V$	2.0	3.6	7.2	V
		$V_{CC} = 15V$	3.0	5.0	10.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = +10\mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = +10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, $V_{IN} = 0V/15V$		0.05	15	μA
		$V_{CC} = 5V$, $V_{IN} = 2.5V$ (Note 4)		20		μA
		$V_{CC} = 10V$, $V_{IN} = 5V$ (Note 4)		200		μA
		$V_{CC} = 15V$, $V_{IN} = 7.5V$ (Note 4)		600		μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay from Input to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		220 80	400 200	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

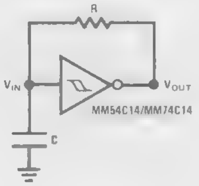
Note 2: Capacitance is guaranteed by periodic testing.

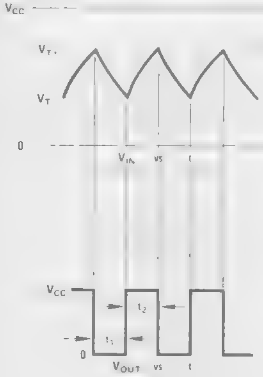
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Note 4: Only one of the six inputs is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

Typical Applications

Low Power Oscillator





$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

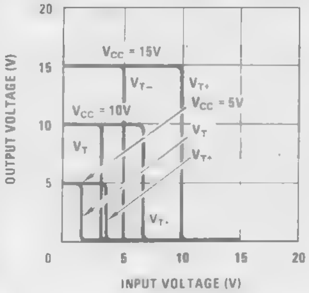
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}\,(V_{CC} - V_{T-})}{V_{T-}\,(V_{CC} - V_{T+})}} \approx \frac{1}{1.7\,RC}$$

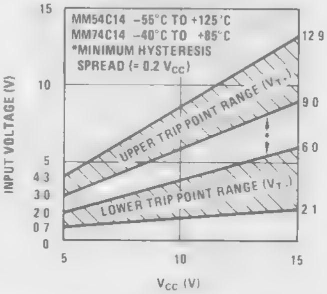
Note: The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$

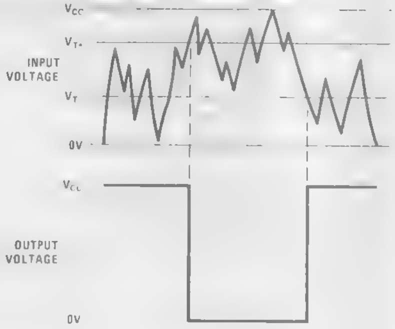
Typical Performance Characteristics

Typical Transfer Characteristics



Guaranteed Trip Point Range





Note: For more information on output drive characteristics, power dissipation, and propagation delays, see AN-90.

National Semiconductor

MM54C30/MM74C30 8-Input NAND Gate

General Description

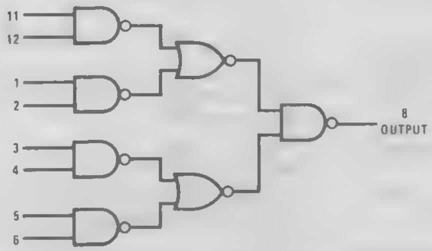
The logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

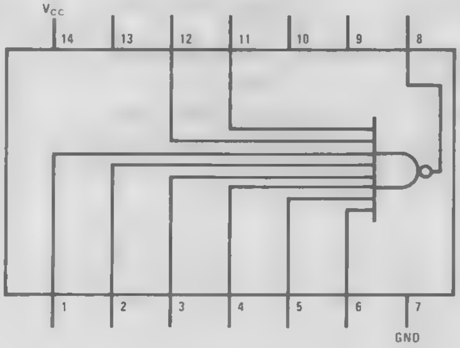
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Logic and Connection Diagrams





TOP VIEW

1

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C30	−55°C to +125°C
MM74C30	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

	Logical "1" or "0"	$V_{CC}=10V$		55	90	ns
C_{IN}	Input Capacitance	(Note 2)		4.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		26		pF

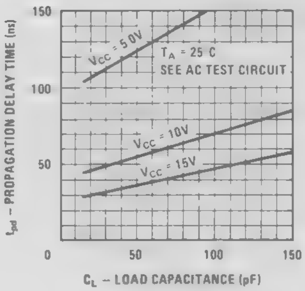
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

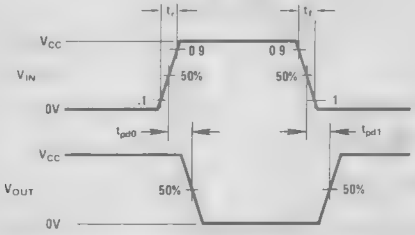
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance

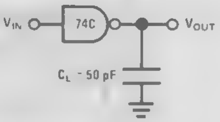


Switching Time Waveforms



NOTE DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns.

AC Test Circuit



National Semiconductor

MM54C32/MM74C32 Quad 2-Input OR Gate

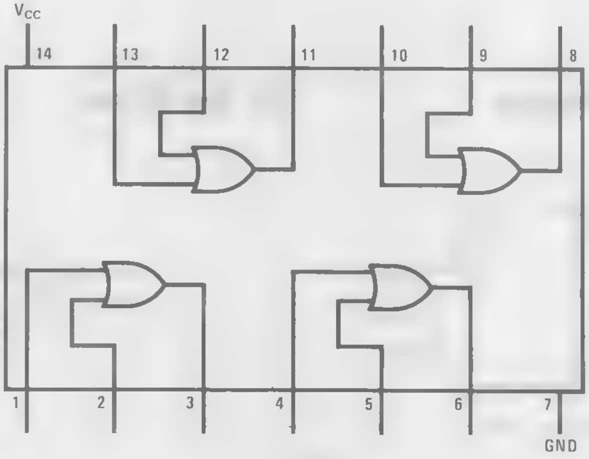
General Description

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C32	−55°C to +125°C
MM74C32	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	15	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C32	$V_{CC}=4.5V$	$V_{CC}-1.5$			V
	MM74C32	$V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C32	$V_{CC}=4.5V$			0.8	V
	MM74C32	$V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage					
	MM54C32	$V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
	MM74C32	$V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C32	$V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
	MM74C32	$V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC}=5.0V$		80	150	ns
		$V_{CC}=10V$		35	70	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 3)		15		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

National Semiconductor

MM54C42/MM74C42 BCD-to-Decimal Decoder

General Description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

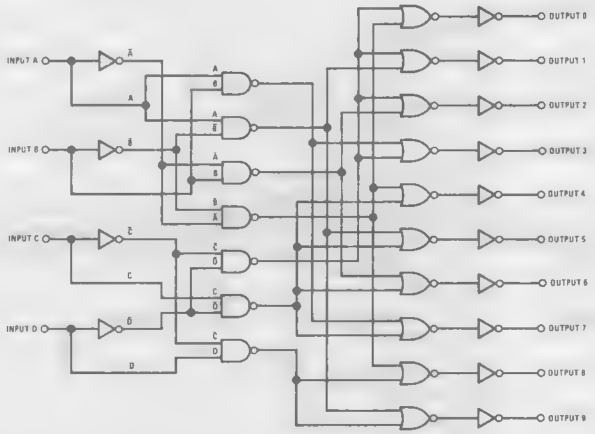
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.) with 10V V_{CC}

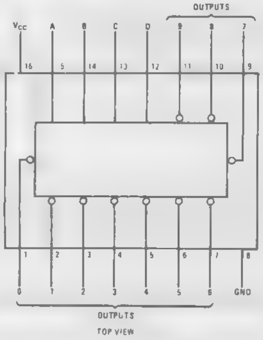
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Schematic Diagram



Connection Diagram



Truth Table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

MM74C42	−40°C to +85°C	Absolute Maximum V_{CC}	18V
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=10\mu A$ $V_{CC}=10V$, $I_O=10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0		300	µA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	µA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) $T_A=25°C$ **(short circuit current)**					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$, $V_{OUT}=0V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$, $V_{OUT}=0V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to Logical "0" or "1"	$V_{CC}=5.0V$ $V_{CC}=10V$		200 90	300 140	ns ns
C_{IN}	Input Capacitance	(See note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(See note 3)		50		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

National Semiconductor

MM54C48/MM74C48 BCD-to-7 Segment Decoder

General Description

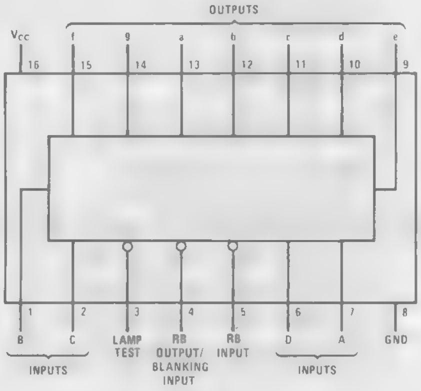
The MM54C48/MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

Features

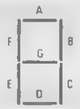
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

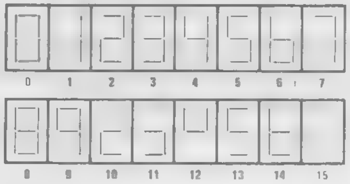
Connection Diagram



TOP VIEW



Segment Identification



Numerical Designations
and Resultant Displays

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C48	−55°C to +125°C
MM74C48	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15.0V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	54C, $V_{CC}=4.5V$, $I_O=-50\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-50\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current (P-Channel) (RB Output Only)	$V_{CC}=4.75V$, $V_{OUT}=0.4V$			−0.80	mA
		$V_{CC}=10V$, $V_{OUT}=0.5V$			−4.0	mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA
	Output Source Current (NPN Bipolar)	$V_{CC}=5.0V$, $V_{OUT}=3.4$	−20	−50		mA
		$V_{CC}=5.0V$, $V_{OUT}=3.0$		−65		mA
		$V_{CC}=10V$, $V_{OUT}=8.4$	−20	−50		mA
		$V_{CC}=10V$, $V_{OUT}=8.0$		−65		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

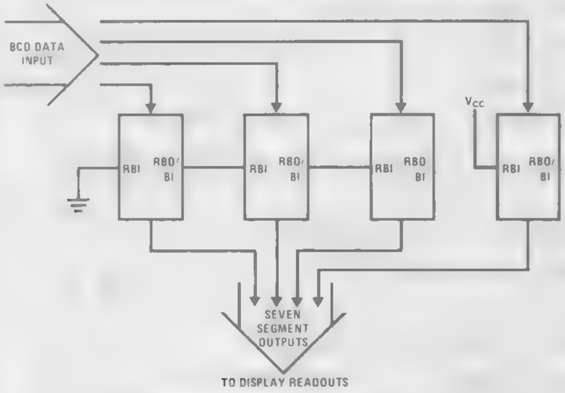
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	1500 500	ns ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		500 180	1600 550	ns ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		350 140	1200 450	ns ns
t_{pd1}	Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	1500 500	ns ns
t_{pd1}	Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		600 250	2000 800	ns ns
t_{pd0}	Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		140 50	450 150	ns ns

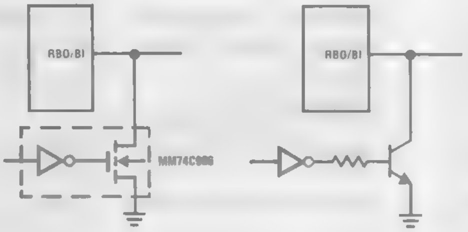
Typical Applications

Typical Connection Utilizing the Ripple-Blanking Feature



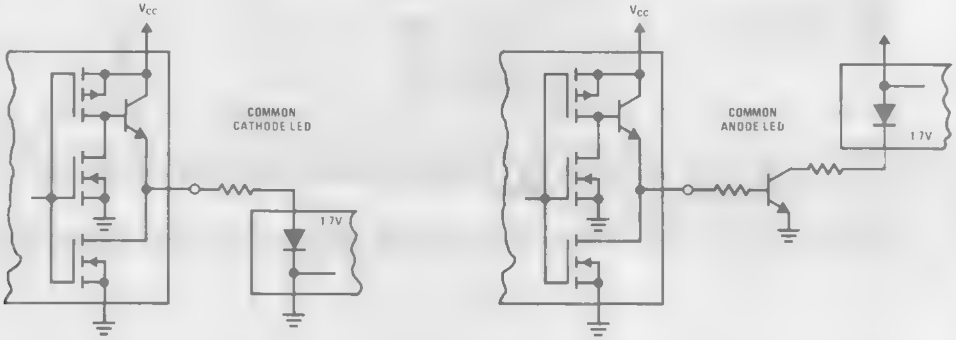
(First three stages will blank leading zeros, the fourth stage will not blank zeros)

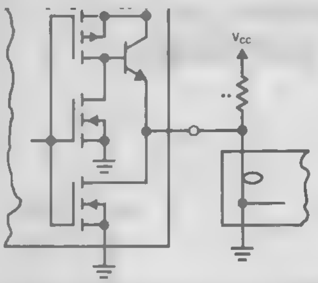
Blanking Input Connection Diagram



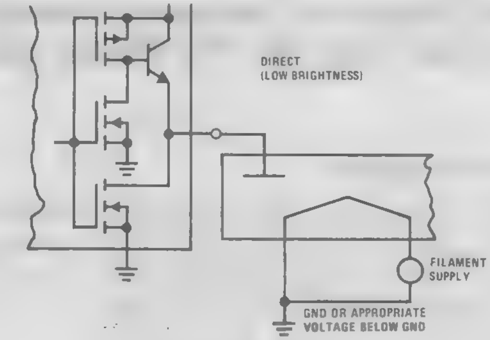
(When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition)

Light Emitting Diode (LED) Readout

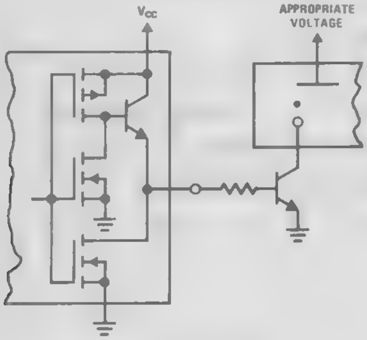




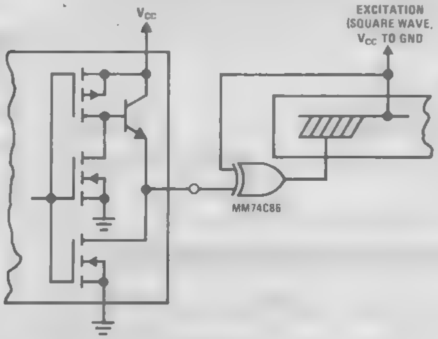
**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts

Truth Table

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RB	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be high, if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open and a low is applied to the lamp-test input, all segment outputs are high.

† One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

National Semiconductor

MM54C73/MM74C73/MM54C76/MM74C76/MM54C107 MM74C107 Dual J-K Flip-Flops with Clear and Preset

General Description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

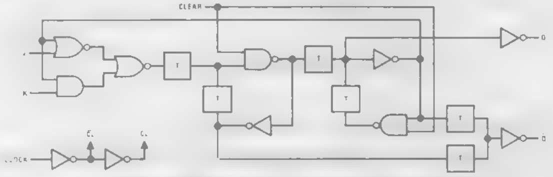
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.) with 10V supply

Applications

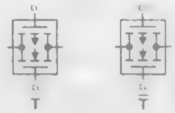
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

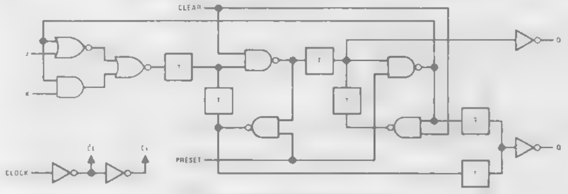
Logic and Connection Diagrams



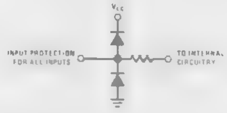
MM54C73/MM74C73 and MM54C107/MM74C107

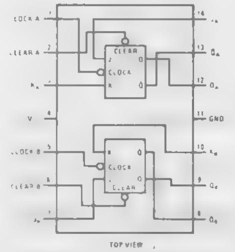
Transmission Gate





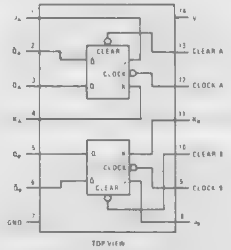
MM54C76/MM74C76





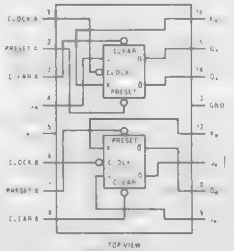
Note. A logic "0" on clear sets Q to logic "0."

MM54C73/MM74C73



Note: A logic "0" on clear sets Q to logic "0."

MM54C107/MM74C107



Note 1: A logic "0" on clear sets Q to a logic "0."
Note 2: A logic "0" on preset sets Q to a logic "1."

MM54C76/MM74C76

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54CXX	−55°C to 125°C
MM74CXX	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating V_{CC} Range	+3V to 15V

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$	4.5			V
		$V_{CC}=10V$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$			0.5	V
		$V_{CC}=10V$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15.0V$			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15.0V$	−1.0			µA
I_{CC}	Supply Current	$V_{CC}=15.0V$		0.050	60	µA
	Low Power TTL to CMOS Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50 pF$, unless otherwise noted.

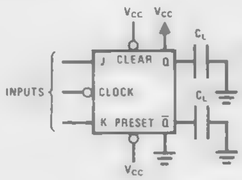
	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	Any Input		5		pF
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0V$ $V_{CC} = 10V$		110 45	175 70	ns ns
t_H	Time after Clock Pulse that J and K must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$		−40 −20	0 0	ns ns
t_{PW}	Minimum Clock Pulse Width $t_{WL} = t_{WH}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 50	190 80	ns ns
t_{PW}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		90 40	130 60	ns ns
f_{MAX}	Maximum Toggle Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.5 7.0	4.0 11.0		MHz MHz
t_r, t_f	Clock Pulse Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$			15 5	μs μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Test Circuit



Truth Table

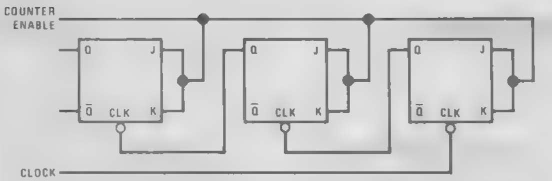
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

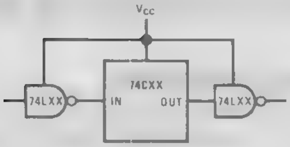
Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

*No change in output from previous state.

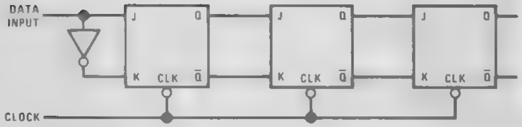
Ripple Binary Counters



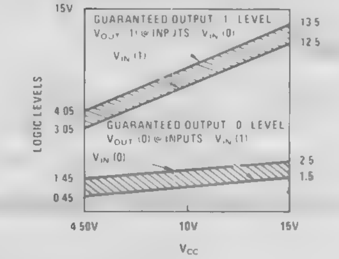
74C Compatibility



Shift Registers

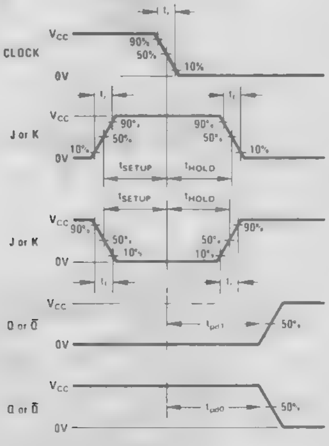


Guaranteed Noise Margin as a Function of V_{CC}



Switching Time Waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

National Semiconductor

MM54C74/MM74C74 Dual D Flip-Flop

General Description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

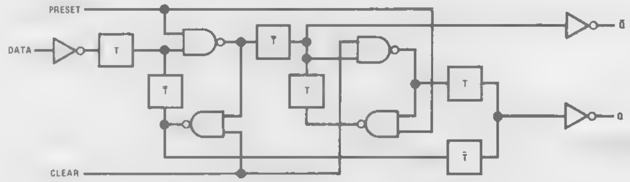
Features

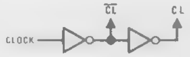
Supply voltage range	3V to 15V
Tenth power TTL compatible	drive 2LPT^{2}L loads
High noise immunity	0.45 V_{CC} (typ)
Low power	50 nW (typ)
Medium speed operation	10 MHz (typ) with 10V supply

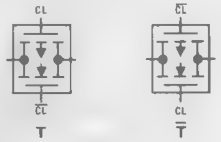
Applications

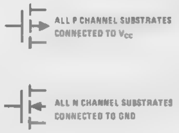
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

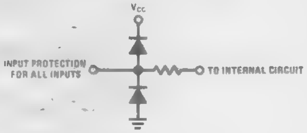
Logic and Connection Diagrams







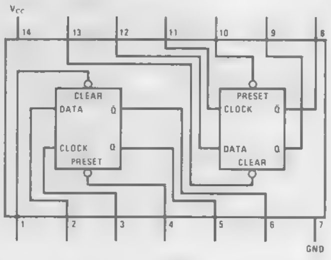

ALL P CHANNEL SUBSTRATES CONNECTED TO V_{CC}
ALL N CHANNEL SUBSTRATES CONNECTED TO GND



Truth Table

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

*No change in output from previous state.



TOP VIEW

Note: A logic "0" on clear sets Q to logic "0."
A logic "0" on preset sets Q to logic "1."

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C74	−55°C to 125°C
MM74C74	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating V_{CC} Range	+3V to +15V

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V	4.5			V
		V_{CC} = 10V	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V			0.5	V
		V_{CC} = 10V			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15.0V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15.0V	−1.0			μA
I_{CC}	Supply Current	V_{CC} = 15.0V		0.05	60	μA
	Low Power TTL/CMOS Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5			
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.75V 74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_D = −360μA 74C, V_{CC} = 4.75V, I_D = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_D = 360μA 74C, V_{CC} = 4.75V, I_D = 360μA			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	Any Input (See Note 2)		5.0		pF
t_{pd}	Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 100	400 150	ns ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data must be Present t_{SETUP}	$V_{CC} = 5.0V$ $V_{CC} = 10V$	100 40	50 20		ns ns
t_{H0}, t_{H1}	Time after Clock Pulse that Data must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$		−20 −8.0	0 0	ns ns
t_{PW1}	Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		100 40	250 100	ns ns
t_{PW2}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		100 40	160 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15.0 5.0			µs µs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	3.5 8.0		MHz MHz
C_{PD}	Power Dissipation Capacitance	See Note 3		40		pF

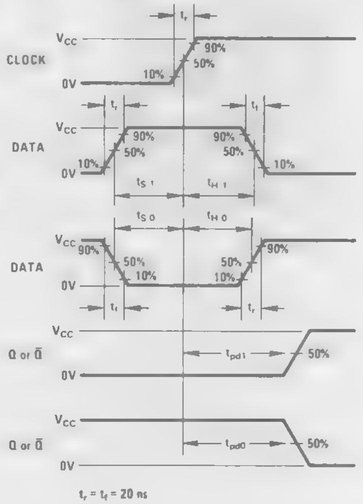
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

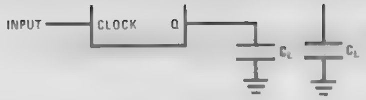
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Switching Time Waveforms

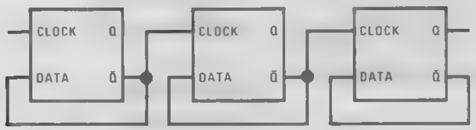
CMOS to CMOS



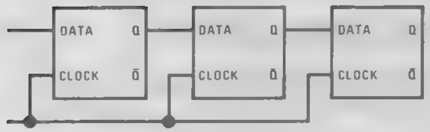


Typical Applications

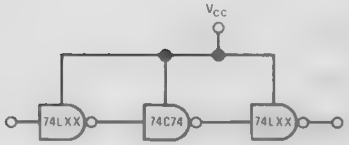
Ripple Counter (Divide by 2^n)



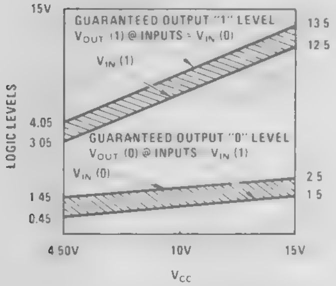
Shift Register



74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



National Semiconductor

MM54C83/MM74C83 4-Bit Binary Full Adder

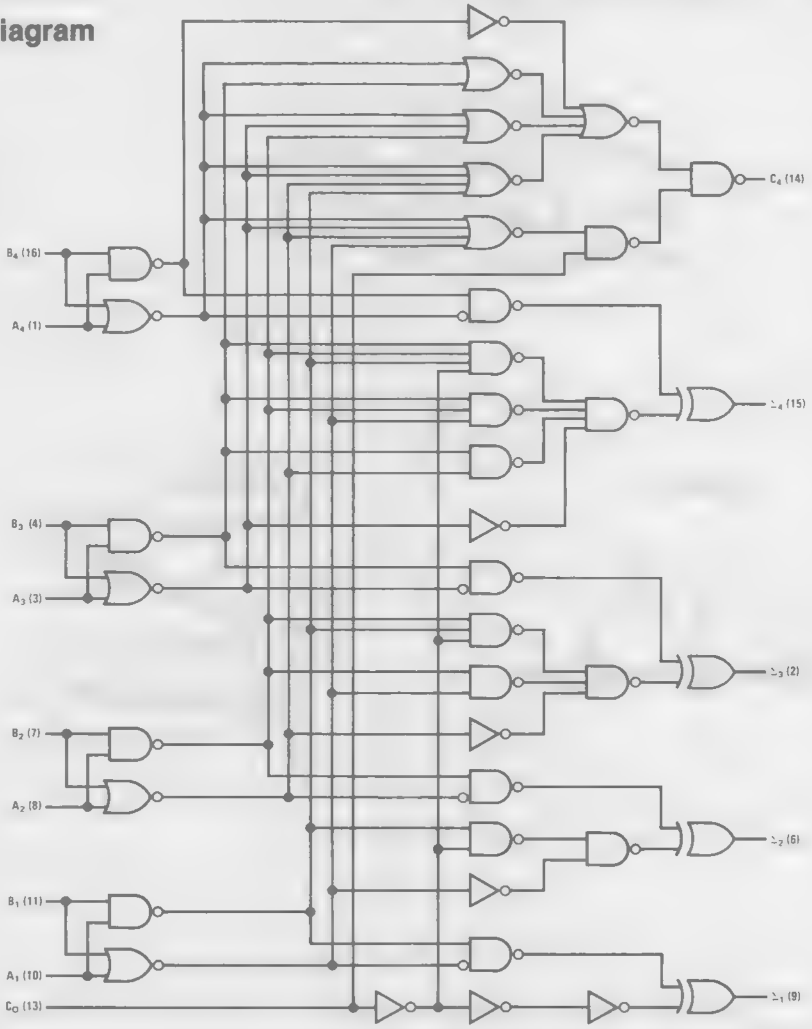
General Description

The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (C_O) is included and the sum (Σ) outputs are provided for each bit and the resultant carry C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Fast carry ripple (C_O to C_4)	50 ns (typ.) @ $V_{CC} = 10V$ and $C_L = 50\,pF$
■ Fast summing (Σ_{IN} to Σ_{OUT})	125 ns (typ.) @ $V_{CC} = 10V$ and $C_L = 50\,pF$

Logic Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C83	−55°C to 125°C
MM74C83	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

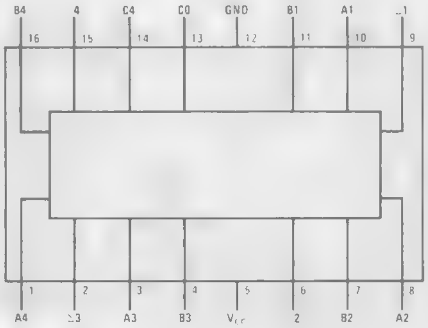
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

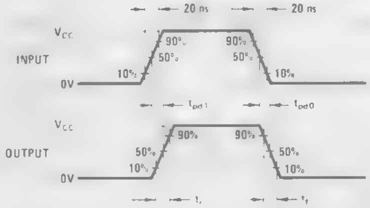
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd1}	Propagation Delay from C_0 to C_4	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 50	200 80	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to C_4	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 90	450 150	ns ns
t_{pd1}	Propagation Delay from C_0 to Sum Outputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		350 125	550 200	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to Sum Outputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		300 90	550 150	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		120		pF

Connection Diagram



Switching Time Waveforms



Inputs must be tied to appropriate logic level

Truth Table

INPUT				OUTPUT WHEN C0 = L / WHEN C2 = L			OUTPUT WHEN C0 = H / WHEN C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	H

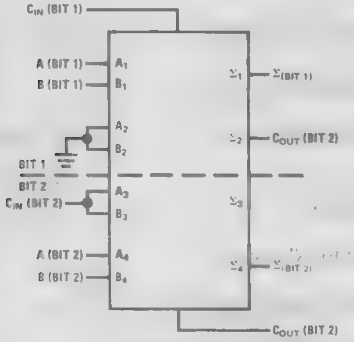
H = high level, L = low level

Note: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Typical Applications

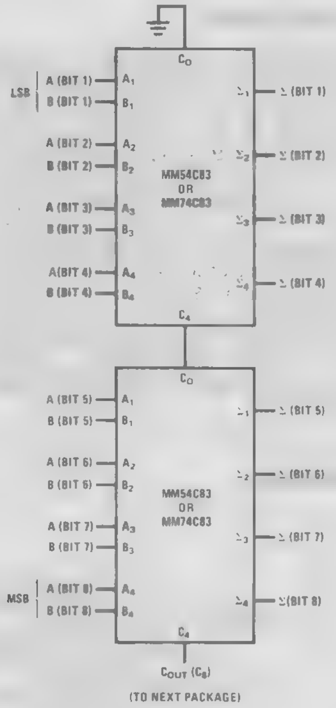
APPLICATION

Connect the MM54C83/MM74C83 in the following manner to implement a dual single bit full adder.



CASCADING

Connect the MM54C83/MM74C83 in the following manner to implement full adders with more than 4 bits.



National Semiconductor

MM54C85/MM74C85 4-Bit Magnitude Comparator

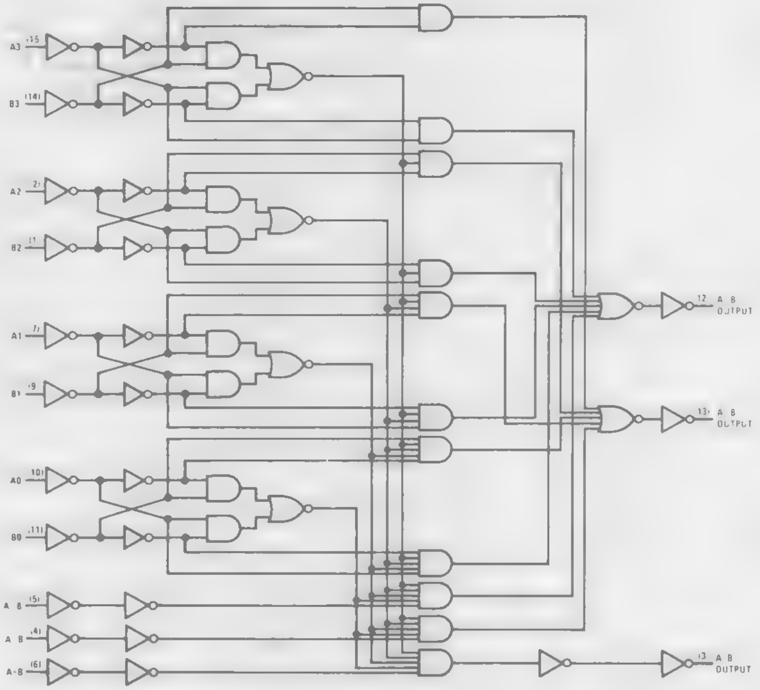
General Description

The MM54C85/MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A > B, A < B and A = B), and three outputs (A > B, A < B and A = B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A > B, A < B, and A = B) of the least significant stage to the cascade inputs (A > B, A < B and A = B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$ applied to the A = B input and low level voltages ($V_{IN(0)}$) applied to A > B and A < B inputs.

Features

Wide supply voltage range	3.0V to 15V
Guaranteed noise margin	1.0V
High noise immunity	0.45 V_{CC} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L
Expandable to 'N' stages	
Applicable to binary or BCD	
The MM54C85/MM74C85 follows the DM54LS85/DM74LS85 Pinout.	

Logic Diagrams



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C85	$-55°C$ to $+125°C$	V_{CC}	18V
MM74C85	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		µA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	µA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay from any A or B Data Input to any Data Output	$V_{CC}=5.0V$ $V_{CC}=10V$		250 100	600 300	ns ns
t_{pd}	Propagation Delay Time from any Cascade Input to any Output	$V_{CC}=5.0V$ $V_{CC}=10V$		200 100	500 250	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Package		45		pF

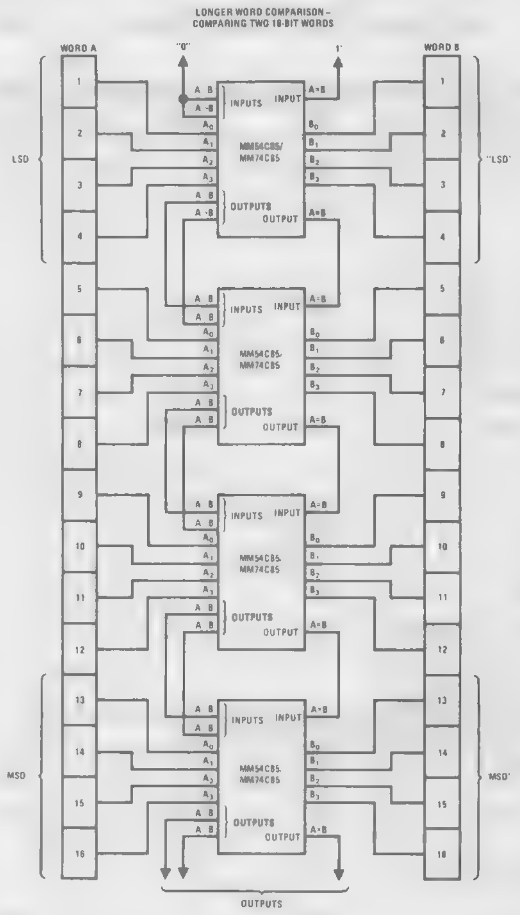
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

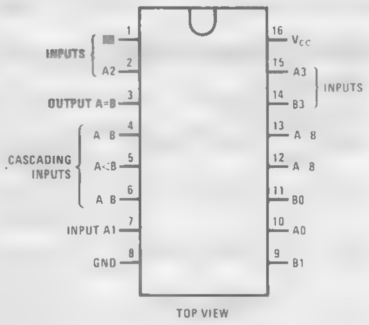
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Applications

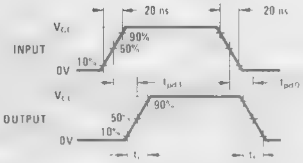
Four Digit Comparator



Connection Diagram



Switching Time Waveforms



Unused inputs must be tied to an appropriate logic level.

Truth Table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

National Semiconductor

MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

General Description

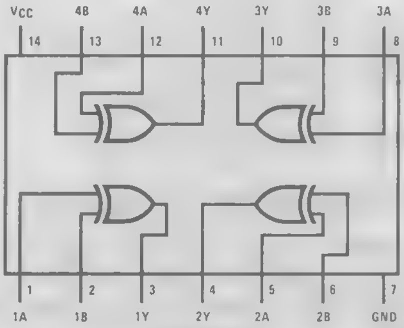
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	10 nW/package (typ.)

- The MM54C86/MM74C86 follows the MM54LS86/MM74LS86 Pinout.

Connection Diagram



TOP VIEW

Truth Table

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Level L= Low Level

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C86	−55°C to +125°C
MM74C86	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA			0.5	V
		V_{CC} = 10V, I_O = +10μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

AC Electrical Characteristics

(MM54C86/MM74C86) T_A = 25°C, C_L = 50 pF, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Time to Logical "1" or "0"	V_{CC} = 5.0V		110	185	ns
		V_{CC} = 10V		50	90	ns
C_{IN}	Input Capacitance	Note 2		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

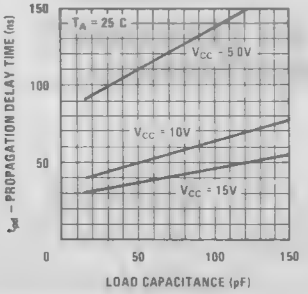
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

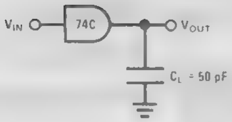
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C86/MM74C86

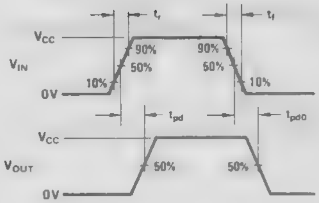


AC Test Circuits



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

Switching Time Waveforms



National
Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different that the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	100 nW/package (typ.)
■ Fast access time	130 ns (typ.) at V_{CC} = 10V
■ TRI-STATE output	

TRI-STATE is a registered trademark of National Semiconductor Corp.

See page 4-3
for Detailed
Specifications

National Semiconductor

MM54C90/MM74C90 4-Bit Decade Counter MM54C93/MM74C93 4-Bit Binary Counter

General Description

The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

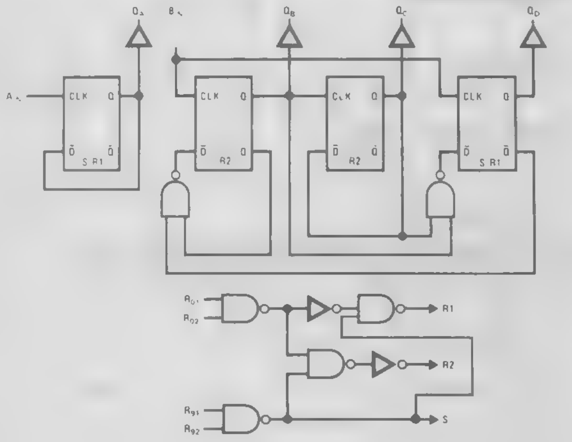
All inputs are protected against static discharge damage.

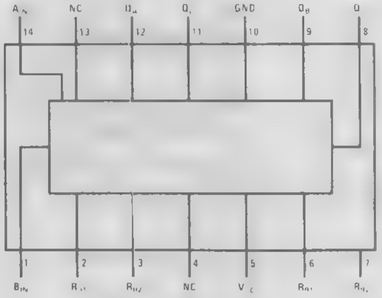
Features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ The MM54C93/MM74C93 follows the MM54L93/MM74L93 Pinout	

Logic and Connection Diagrams

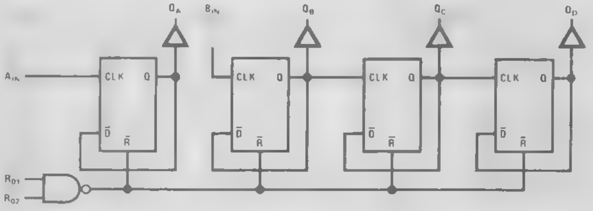
MM54C90/MM74C90

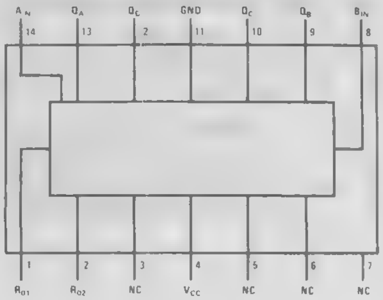




TOP VIEW

MM54C93/MM74C93





TOP VIEW

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C90, MM54C93	$-55°C$ to $+125°C$
MM74C90, MM74C93	$-40°C$ to $+85°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C90, MM54C93	$V_{CC}=4.5V$	$V_{CC}-1.5$			V
	MM74C90, MM74C93	$V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C90, MM54C93	$V_{CC}=4.5V$			0.8	V
	MM74C90, MM74C93	$V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage					
	MM54C90, MM54C93	$V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
	MM74C90, MM74C93	$V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C90, MM54C93	$V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
	MM74C90, MM74C93	$V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8	16		mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_A	$V_{CC}=5.0V$		200	400	ns
		$V_{CC}=10V$		80	150	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_B (MM54C93/MM74C93)	$V_{CC}=5.0V$		450	850	ns
		$V_{CC}=10V$		160	300	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_B (MM54C90/MM74C90)	$V_{CC}=5.0V$		450	800	ns
		$V_{CC}=10V$		160	300	ns

AC Electrical Characteristics (Cont'd.) $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

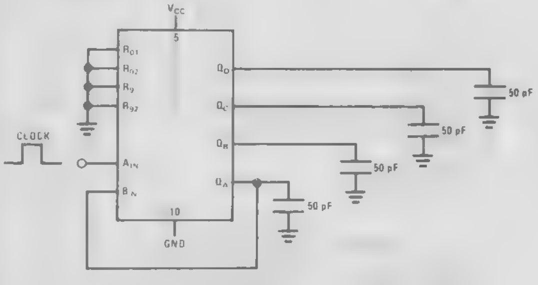
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C93/MM74C93)	$V_{CC} = 5.0V$		500	1050	ns
		$V_{CC} = 10V$		200	400	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C90/MM74C90)	$V_{CC} = 5.0V$		500	1000	ns
		$V_{CC} = 10V$		200	400	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C93/MM74C93)	$V_{CC} = 5.0V$		600	1200	ns
		$V_{CC} = 10V$		250	500	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0V$		450	800	ns
		$V_{CC} = 10V$		160	300	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C93/MM74C93)	$V_{CC} = 5.0V$		150	300	ns
		$V_{CC} = 10V$		75	150	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0V$		200	400	ns
		$V_{CC} = 10V$		75	150	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{91} or R_{92} to Q_A or Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0V$		250	500	ns
		$V_{CC} = 10V$		100	200	ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C93/MM74C93)	$V_{CC} = 5.0V$	600	250		ns
		$V_{CC} = 10V$	300	125		ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C90/MM74C90)	$V_{CC} = 5.0V$	600	250		ns
		$V_{CC} = 10V$	300	125		ns
t_{PW}	Min. R_{91} or R_{92} Pulse Width (MM54C90/MM74C90)	$V_{CC} = 5.0V$	500	200		ns
		$V_{CC} = 10V$	250	100		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 10V$			15	µs
		$V_{CC} = 10V$			5	µs
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$	250	100		ns
		$V_{CC} = 10V$	100	50		ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2			MHz
		$V_{CC} = 10V$	5			MHz
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		45		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

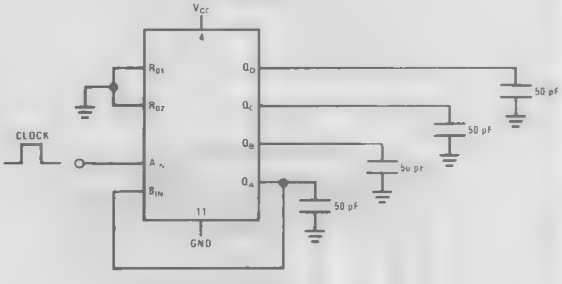
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Test Circuits



Clock rise and fall time $t_r = t_f = 20\,ns$

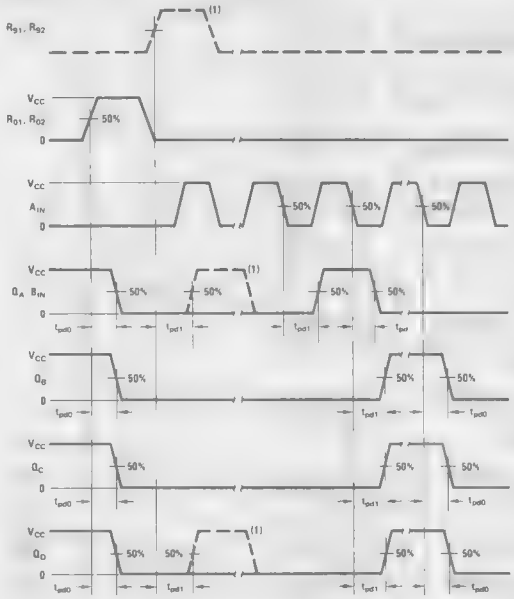
MM54C90/MM74C90



Clock rise and fall time $t_r = t_f = 20\,ns$

MM54C93/MM74C93

Switching Time Waveforms



Note 1 MM54C90, MM74C90 and MM54C93, MM74C93 are solid line waveforms. Dashed line waveforms are for MM54C90/MM74C90 only.

Truth Tables

MM54C90/MM74C90 4-Bit Decade Counter

BCD Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to input B for BCD count.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

MM54C93/MM74C93 4-Bit Binary Counter

Binary Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS		OUTPUT			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

National Semiconductor

MM54C95/MM74C95 4-Bit Right-Shift Left-Shift Register

General Description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

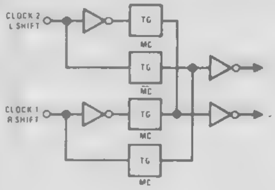
Features

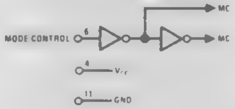
- Medium speed operation 10 MHz (typ.) $V_{CC} = 10\,V$, $C_L = 50\,pF$
- High noise immunity 0.45 V_{CC} (typ.)
- Low power 100 nW/ (typ.)
- Tenth power TTL compatible Drive 2 LTTL loads
- Wide supply voltage range 3 V to 15 V
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking
- The MM54C95/MM74C95 follows the MM54L95/MM74L95 Pinout.

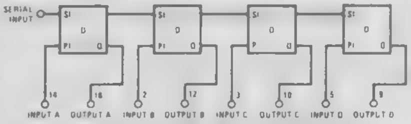
Applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Block and Connection Diagrams







Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Function Table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS		SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	[illegible]			
↓	H	L	X	X	X	X	X	Operating Conditions			

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D

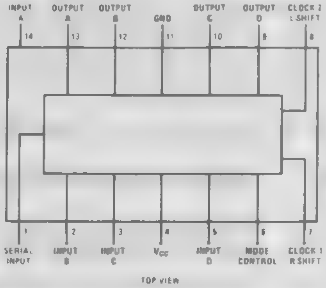
H = high level (steady state) L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level ↑ = transition from low to high level

a, b, c, d = the level of steady state input at inputs A, B, C or D, respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3 V to $V_{CC}+0.3\text{ V}$
Operating Temperature	
MM54C95	$-55°C$ to $+125°C$
MM74C95	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
Maximum V_{CC} Voltage	18V
Package Dissipation	500 mW
Operating V_{CC} Range	+3 V to +15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$	4.5 9			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\text{ V}$			1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\text{ V}$	−1			μA
I_{CC}	Supply Current	$V_{CC}=15\text{ V}$		0.050	300	μA
	Low Power TTL/CMOS Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5\text{ V}$ 74C, $V_{CC}=4.75\text{ V}$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5\text{ V}$ 74C, $V_{CC}=4.75\text{ V}$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5\text{ V}$, $I_O=360\,\mu A$ 74C, $V_{CC}=4.75\text{ V}$, $I_O=360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5\text{ V}$, $I_O=360\,\mu A$ 74C, $V_{CC}=4.75\text{ V}$, $I_O=360\,\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\text{ V}$, $V_{IN(0)}=0\text{ V}$ $T_A=25°C$, $V_{OUT}=0\text{ V}$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\text{ V}$, $V_{IN(0)}=0\text{ V}$ $T_A=25°C$, $V_{OUT}=0\text{ V}$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\text{ V}$, $V_{IN(1)}=5.0\text{ V}$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\text{ V}$, $V_{IN(1)}=10\text{ V}$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50\text{ pF}$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$		200 80	400 160	ns ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data must be Preset	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$	60 25	30 10		ns ns
t_{H0}, t_{H1}	Time After Clock Pulse that Data must be Held	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$	25 10	10 50		ns ns
t_{PW}	Minimum Clock Pulse Width ($t_{WL}=t_{WH}$)	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$		100 50		ns ns
t_{SM}	Time Prior to Clock Pulse that Mode Control must be Preset	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$	200 100	100 50		ns ns
f_{MAX}	Maximum Input Clock Frequency	$V_{CC}=5.0\text{ V}$ $V_{CC}=10\text{ V}$	3 6.5	5 10		MHz MHz
C_{IN}	Input Capacitance	Any Input. (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

National
Semiconductor

MM54C150/MM74C150 16-Line to 1-Line Multiplexer MM72C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

General Description

The MM54C150/MM74C150 and MM72C19/MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

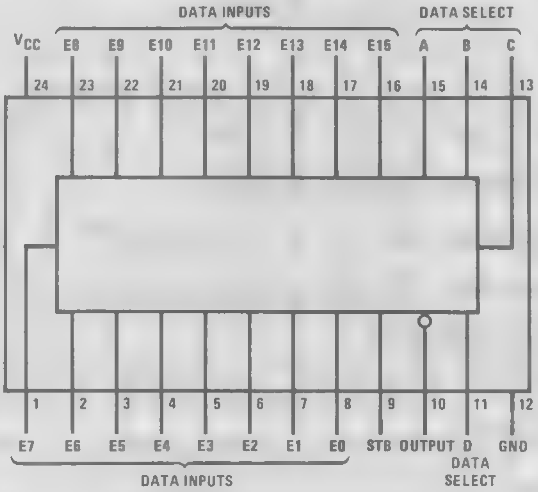
A strobe override places the output of MM54C150/MM74C150 in the logical "1" state and the output of MM72C19/MM82C19 in the high-impedance state.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Drive 1 TTL Load

Connection Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$
Operating Temperature Range	
MM54C150, MM72C19	−55°C to +125°C
MM74C150, MM82C19	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State MM73C19/MM82C19	$V_{CC}=15\,V$, $V_O=15\,V$ $V_{CC}=15\,V$, $V_O=0\,V$	 −1.0	0.005 −0.005	1.0 	μA μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
	TTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, 72C $V_{CC}=4.5\,V$ 74C, 82C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, 72C $V_{CC}=4.5\,V$ 74C, 82C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, 72C $V_{CC}=4.5\,V$, $I_O=-1.6\,mA$ 74C, 82C $V_{CC}=4.75\,V$, $I_O=-1.6\,mA$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C, 72C $V_{CC}=4.5\,V$, $I_O=1.6\,mA$ 74C, 82C $V_{CC}=4.75\,V$, $I_O=1.6\,mA$			0.4 0.4	V V
	Output Drive (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=0\,V$, $T_A=25°C$	−4.35	−8		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$, $V_{OUT}=0\,V$, $T_A=25°C$	−20	−40		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	20	40		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0\,V$		250	600	ns
		$V_{CC} = 10\,V$		110	300	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		290	650	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0\,V$		290	650	ns
		$V_{CC} = 10\,V$		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output MM54C150/MM74C150	$V_{CC} = 5.0\,V$		120	300	ns
		$V_{CC} = 10\,V$		55	150	ns
t_{1H}, t_{0H}	Delay from Strobe to High Impedance State MM72C19/MM82C19	$V_{CC} = 5.0\,V$, $R_L = 10k$, $C_L = 5\,pF$		80	200	ns
		$V_{CC} = 10\,V$, $R_L = 10k$, $C_L = 5\,pF$		60	150	ns
t_{H1}, t_{H0}	Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State) MM72C19/MM82C19	$V_{CC} = 5.0\,V$, $R_L = 10k$, $C_L = 5\,pF$		80	250	ns
		$V_{CC} = 10\,V$, $R_L = 10k$, $C_L = 5\,pF$		30	120	ns
C_{IN}	Input Capacitance	Any Input, (Note 2)		5.0		pF
C_{OUT}	Output Capacitance MM72C19/MM82C19	(Note 2)		11.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Truth Table

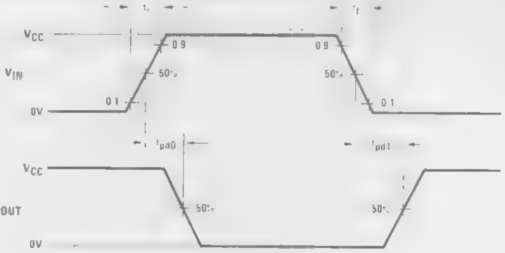
MM54C150/MM74C150

INPUTS																					OUTPUT
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1*
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

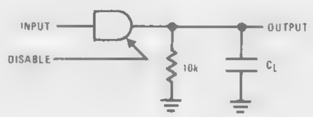
*For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

Switching Time Waveforms

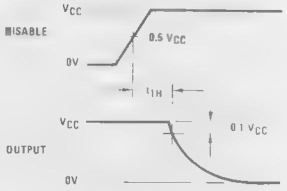
CMOS to CMOS



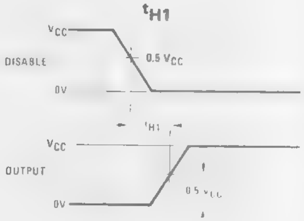
t_{1H} and t_{H1}



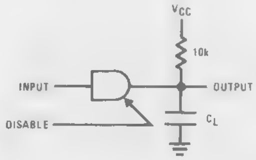
t_{1H}



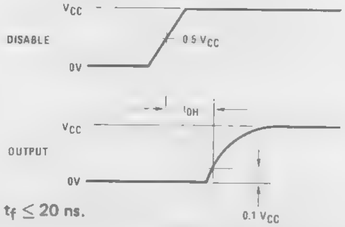
t_{H1}



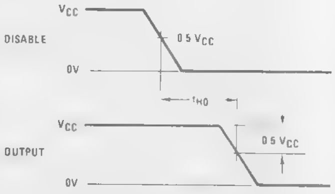
t_{0H} and t_{H0}



t_{0H}



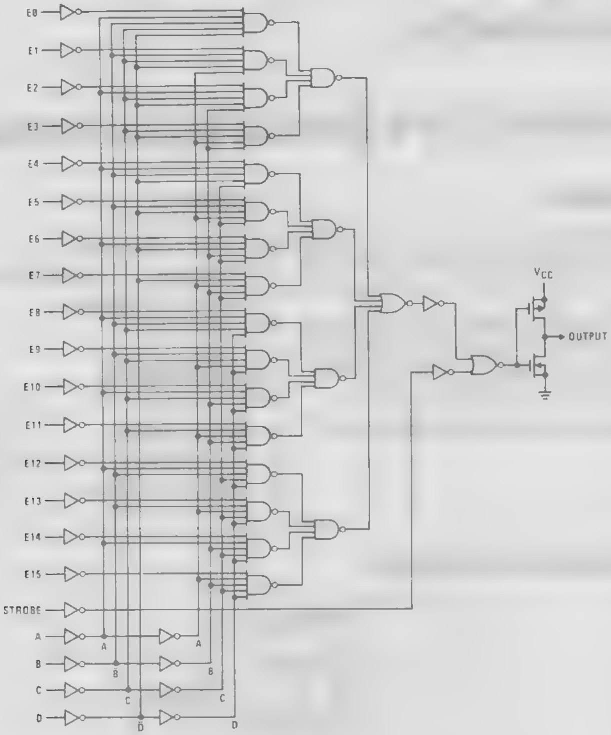
t_{H0}



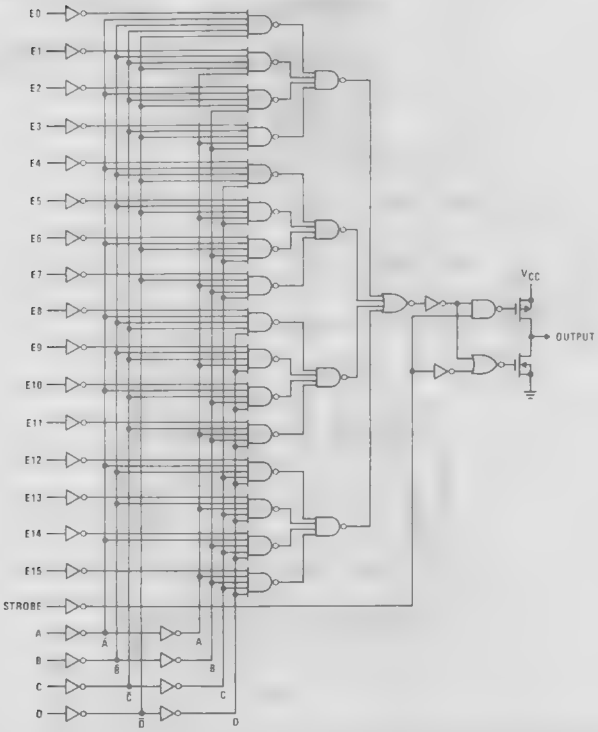
Note: Delays measured with input t_r, $t_f \leq 20$ ns.

Logic Diagram

MM54C150/MM74C150



MM72C19/MM82C19



National Semiconductor

MM54C151/MM74C151 8-Channel Digital Multiplexer

General Description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0".

All inputs are protected against electrostatic effects.

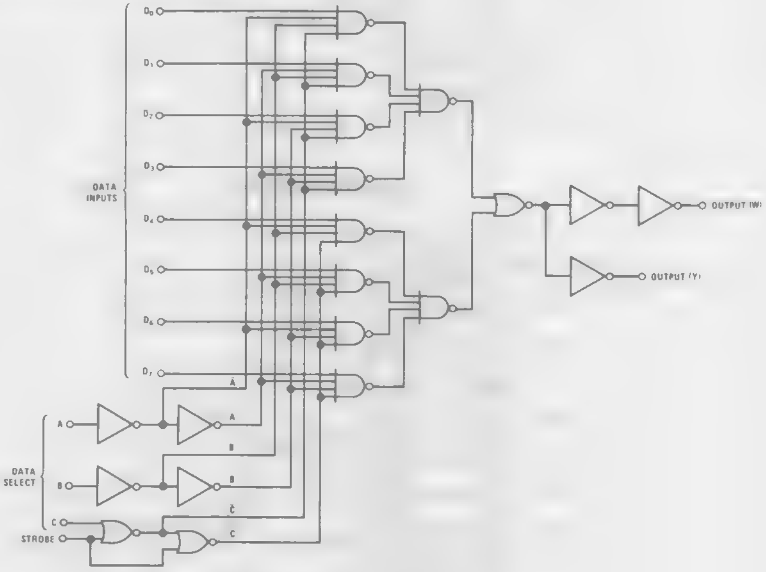
Features

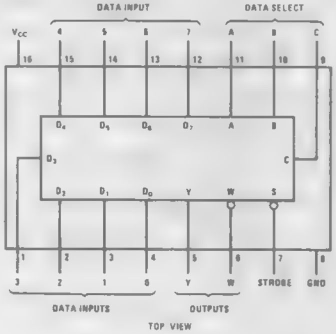
■ Supply voltage range	3 V to 15 V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams





MM74C151	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\,\mu A$ $V_{CC} = 10\,V$, $I_O = -10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = +10\,\mu A$ $V_{CC} = 10\,V$, $I_O = +10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0			μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	300	μA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V mA
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = -360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = 360\,\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0\,V$, $V_{IN(1)} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10\,V$, $V_{IN(1)} = 10\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y	$V_{CC} = 5.0V$, $V_{CC} = 10V$		170 80	270 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data to W	$V_{CC} = 5.0V$, $V_{CC} = 10V$		200 90	300 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y	$V_{CC} = 5.0V$, $V_{CC} = 10V$		240 110	360 170	ns ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		50		pF

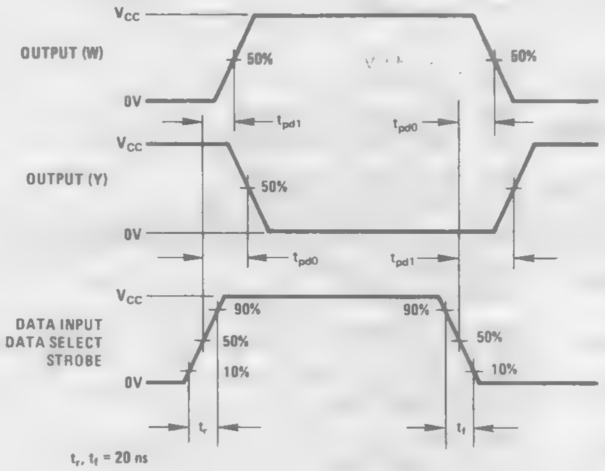
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

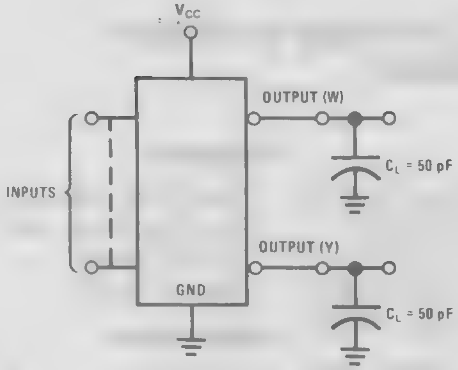
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms

CMOS to CMOS (t_{pd1} & t_{pd0})



AC Test Circuit



Truth Table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

National Semiconductor

MM54C154/MM74C154 4-Line to 16-Line Decoder/Demultiplexer

General Description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

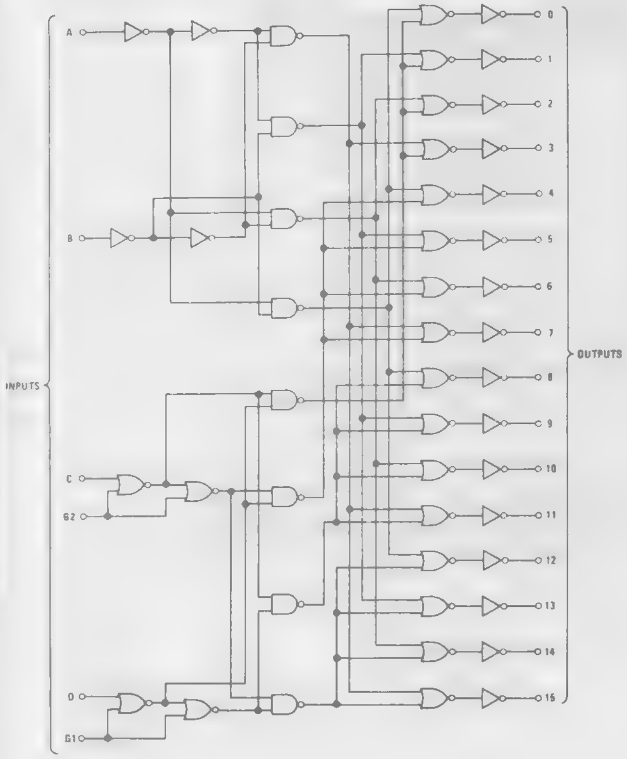
Features

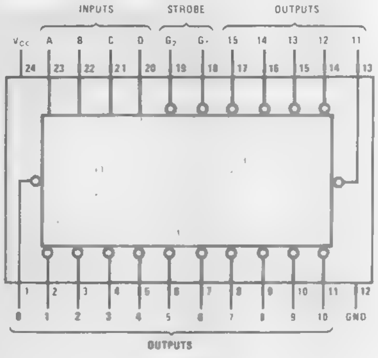
■ Supply voltage range	3 V to 15 V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise margin	1 V guaranteed
■ High noise immunity	$0.45\ V_{CC}$ (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams





TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$
Operating Temperature Range	
MM54C154	−55°C to +125°C
MM74C154	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\,\mu A$ $V_{CC} = 10\,V$, $I_O = -10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = +10\,\mu A$ $V_{CC} = 10\,V$, $I_O = +10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0	−0.005		µA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	300	µA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -100\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = -100\,\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = 360\,\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0\,V$, $V_{IN(1)} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10\,V$, $V_{IN(1)} = 10\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

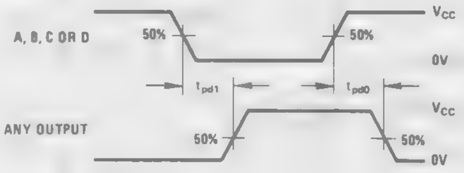
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}	Propagation Delay to a Logical "0" From Any Input to Any Output	$V_{CC} = 5.0V$, $V_{CC} = 10V$		275 100	400 200	ns ns
t_{pd0}	Propagation Delay to a Logical "0" from G1 or G2 to Any Output	$V_{CC} = 5.0V$, $V_{CC} = 10V$		275 100	400 200	ns ns
t_{pd1}	Propagation Delay to a Logical "1" from Any Input to Any Output	$V_{CC} = 5.0V$, $V_{CC} = 10V$		265 100	400 200	ns ns
t_{pd1}	Propagation Delay to a Logical "1" from G1 or G2 to Any Output	$V_{CC} = 5.0V$, $V_{CC} = 10V$		265 100	400 200	ns ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

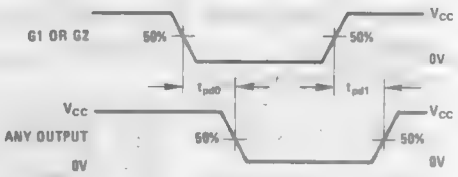
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms





$t_r = t_f = 20$ ns

Truth Table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

National Semiconductor

MM54C157/MM74C157 Quad 2-Input Multiplexers

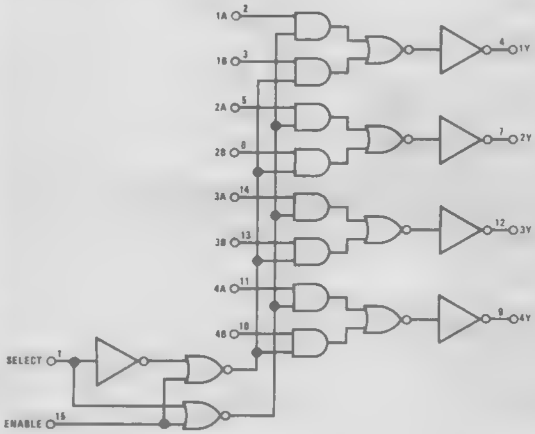
General Description

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

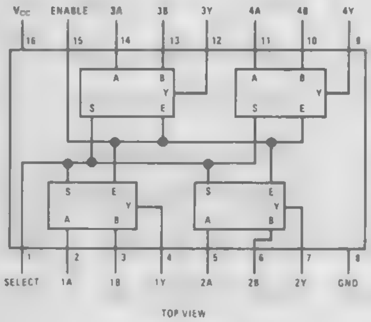
Features

■ Supply voltage range	3 V to 15 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Tenth power TTL compatible	drive 2 LPTTL loads

Logic Diagram

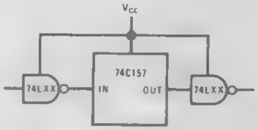


Connection Diagram



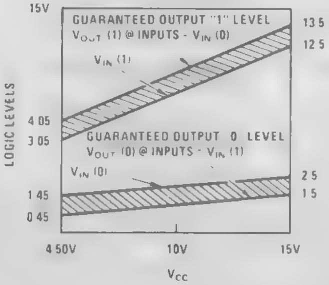
Truth Table

ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1



74L Compatibility

Guaranteed Noise Margin as a Function of V_{CC}



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Maximum V_{CC} Voltage	18V
Operating Temperature Range		Package Dissipation	500 mW
MM54C157	−55°C to +125°C	Operating V_{CC} Range	3V to 15V
MM74C157	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$,	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	60	μA
	CMOS to Tenth Power Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5V$ 74C $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5V$ 74C $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5V$, $I_O=360\mu A$ 74C $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay from Data to Output	$V_{CC}=5.0V$ $V_{CC}=10V$		150 70	250 110	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Select to Output	$V_{CC}=5.0V$ $V_{CC}=10V$		180 80	300 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Enable to Output	$V_{CC}=5.0V$ $V_{CC}=10V$		180 80	300 130	ns ns
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

National Semiconductor

MM54C160/MM74C160 Decade Counter with Asynchronous Clear
MM54C161/MM74C161 Binary Counter with Asynchronous Clear
MM54C162/MM74C162 Decade Counter with Synchronous Clear
MM54C163/MM74C163 Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

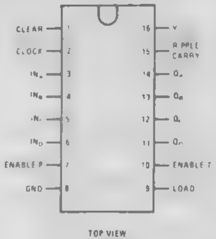
A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

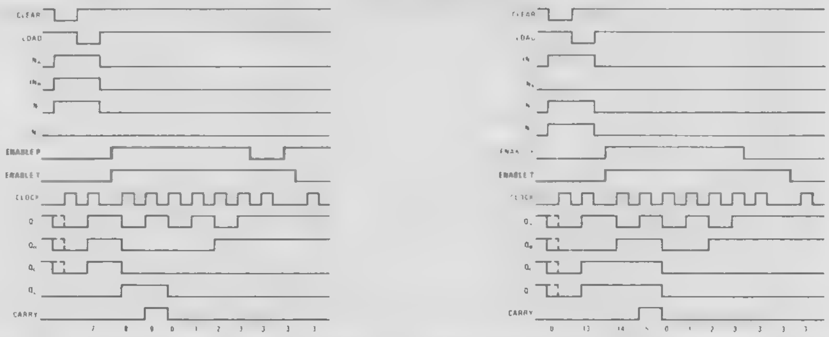
■ High noise margin	1 V guaranteed
■ High noise immunity	$0.45\ V_{CC}$ (typ.)
■ Tenth power TTL compatible	drives 2 LPTTL loads
■ Wide supply voltage range	3 V to 15 V
■ Internal look-ahead for fast counting schemes	
■ Carry output for N-bit cascading	
■ Load control line	
■ Synchronously programmable	

Connection Diagram



TOP VIEW

Logic Waveforms



C160, --- C162 Decade Counters

C161, --- C163 Binary Counters

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C160/1/2/3	−55°C to +125°C
MM74C160/1/2/3	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Package Dissipation	500mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = +10\mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = +10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$			0.8	V
		74C $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -360\mu A$	2.4			V
		74C $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4			V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = +360\mu A$			0.4	V
		74C $V_{CC} = 4.75V$, $I_O = +360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0V$, $V_{IN(1)} = 5.0V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8,0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time from Clock to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 100	400 160	ns ns
t_{pd}	Propagation Delay Time from Clock to Carry Out	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		290 120	450 190	ns ns
t_{pd}	Propagation Delay Time from T Enable to Carry Out	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		180 70	290 120	ns ns
t_{pd}	Propagation Time from Clear to Q (C160 and C161 only)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		190 80	300 150	ns ns
t_S	Time prior to Clock that Data or Load must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 30		ns ns
t_S	Time prior to Clock that Enable P or T must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		170 70	280 120	ns ns
t_S	Time prior to Clock that Clear must be Present (162, 163 only)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	190 80	ns ns
t_W	Minimum Clock Pulses Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		90 35	170 70	ns ns
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			15 5.0	µs µs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.5	3.0 8.5		MHz MHz
C_{PD}	Power Dissipation Capacitance	Note 3		95		pF
	Input Capacitance	Note 2		5.0		pF

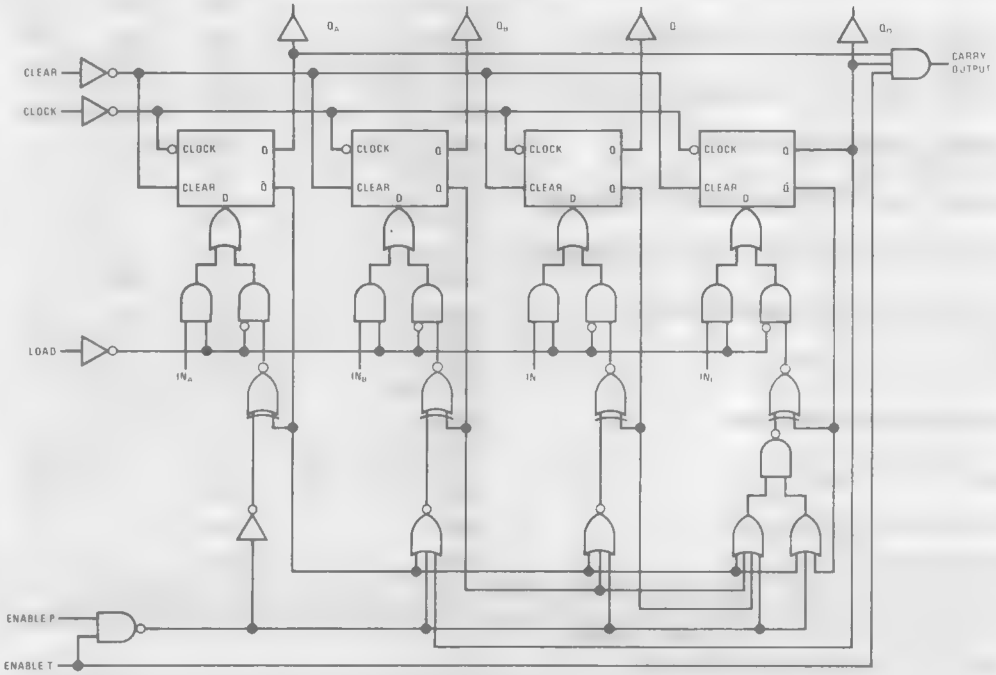
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

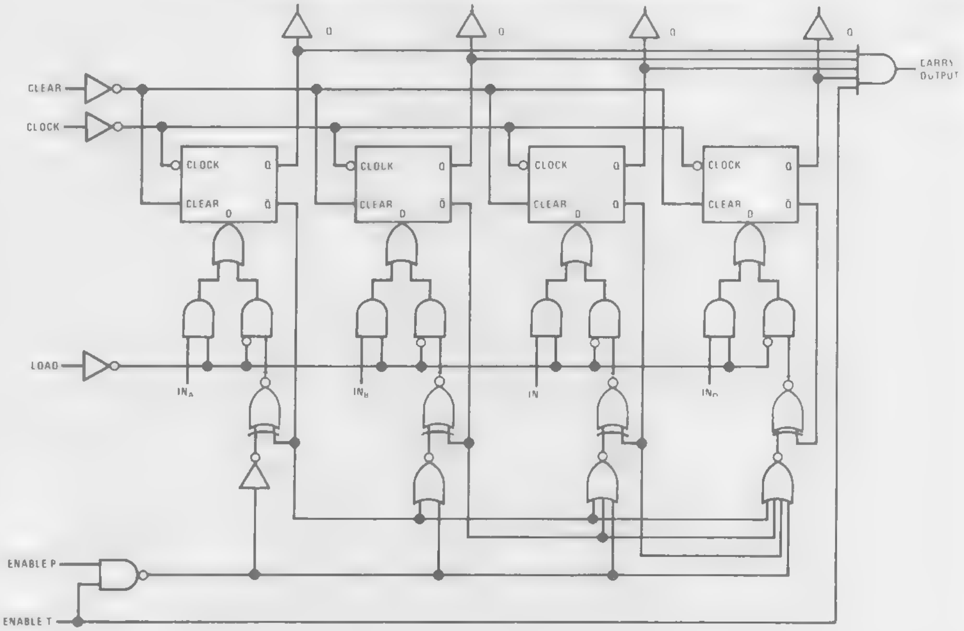
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Logic Diagrams

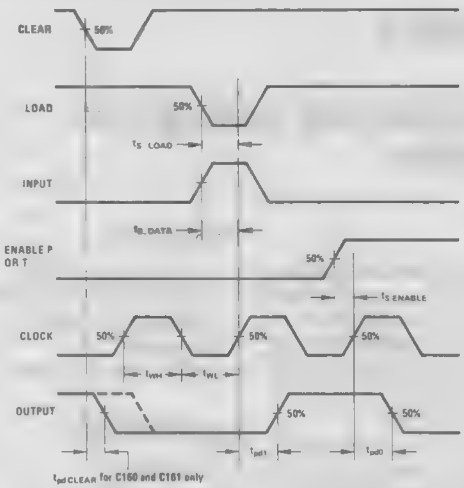
MM74C160, MM74C162; Clear is Synchronous for the MM74C162



MM74C161, MM74C163; Clear is Synchronous for the MM74C163



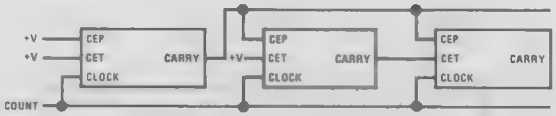
Switching Time Waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns PRR ≤ 1 MHz duty cycle $\leq 50\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



National Semiconductor

MM54C164/MM74C164 8-Bit Parallel-Out Serial Shift Register

General Description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. A high-level input enables the other input which will then determine the state of the flip flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

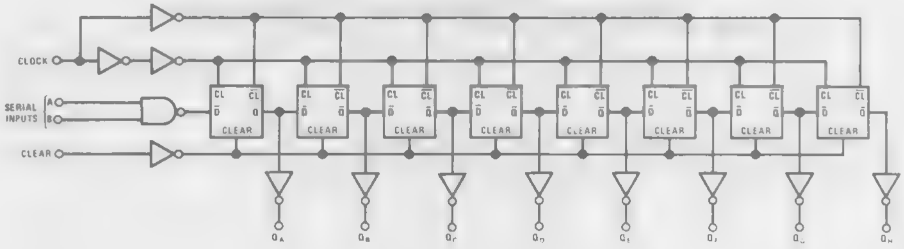
Features

■ Supply voltage range	3 V to 15 V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	8.0 MHz (typ.) with 10 V supply

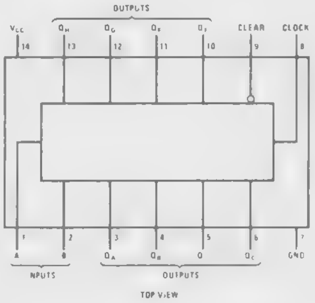
Applications

- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Block Diagram



Connection Diagram



Truth Tables

Serial Inputs A and B

INPUTS		OUTPUT
t_n		t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC}+0.3 V
Operating Temperature Range	
MM54C164	−55°C to +125°C
MM74C164	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Absolute Maximum V_{CC}	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V	3.5			V
		V_{CC} = 10 V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V			1.5	V
		V_{CC} = 10 V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V, I_O = −10 μA	4.5			V
		V_{CC} = 10 V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, I_O = +10 μA			0.5	V
		V_{CC} = 10 V, I_O = +10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V, V_{IN} = 0 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	μA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V	V_{CC} − 1.5			V
		74C V_{CC} = 4.75 V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V			0.8	V
		74C V_{CC} = 4.75 V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA	2.4			V
		74C V_{CC} = 4.75 V, I_O = −360 μA	2.4			V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 μA			0.4	V
		74C V_{CC} = 4.75 V, I_O = 360 μA			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

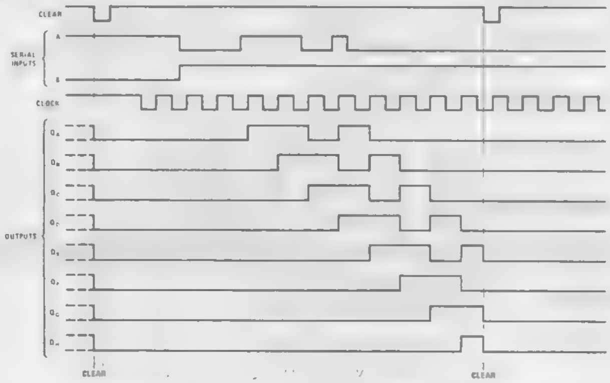
	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd1}	Propagation Delay Time to a Logical "0" or a Logical "1" from Clock to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		230 90	310 120	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		280 110	380 150	ns ns
t_S	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	200 80	110 30		ns ns
t_H	Time After Clock Pulse that Data Must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0 0	0 0		ns ns
t_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.5	3 8		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 55	250 90	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0			µs µs
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		140		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

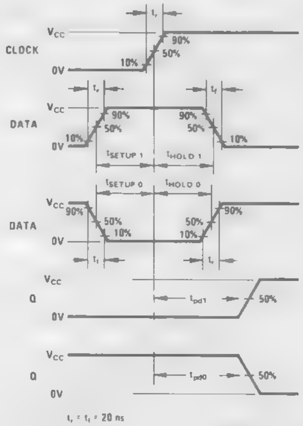
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

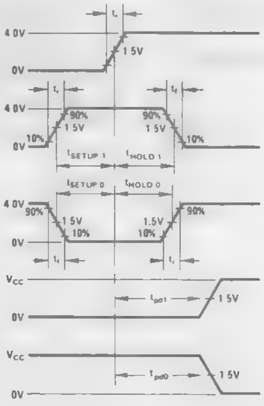
Switching Time Waveforms



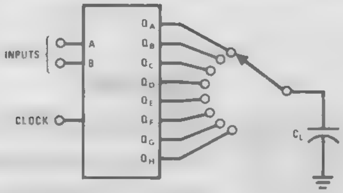
CMOS to CMOS



TTL to CMOS

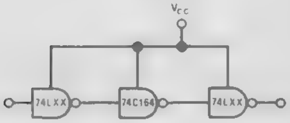


AC Test Circuit

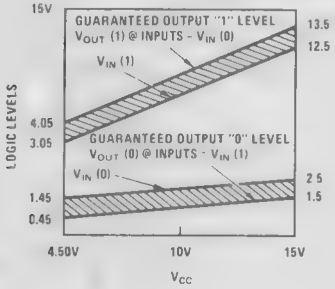


Typical Applications

74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



National Semiconductor

MM54C165/MM74C165 Parallel-Load 8-bit Shift Register

General Description

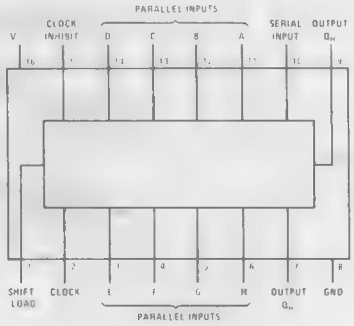
The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Features

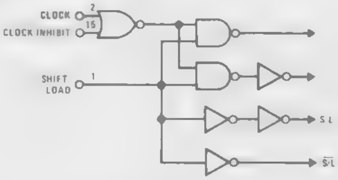
■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	$0.45\ V_{CC}$ (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Direct overriding load	
■ Gated clock inputs	
■ Fully static operation	

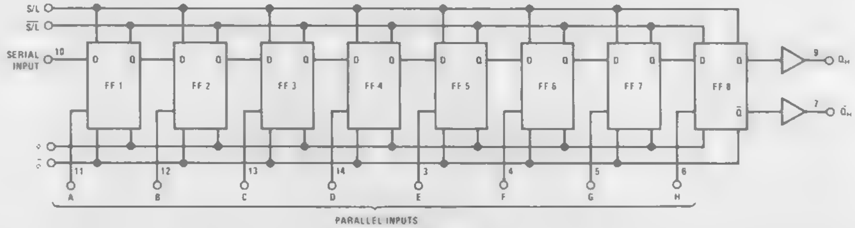
Connection Diagram



TOP VIEW

Block Diagrams





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C165	−55°C to +125°C
MM74C165	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Absolute Maximum V_{CC}	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5V$ 74C $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5V$ 74C $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5V$, $I_O=360\mu A$ 74C $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$ $T_A=25°C$, $V_{OUT}=0V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$ $T_A=25°C$, $V_{OUT}=0V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

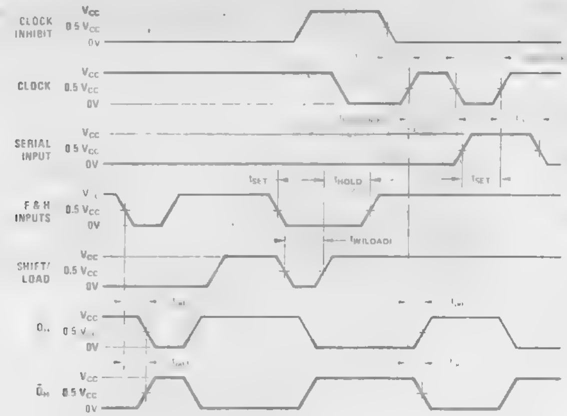
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		200 80	400 200	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		200 80	400 200	ns ns
t_S	Clock Inhibit Set-up Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	150 60	75 30		ns ns
t_S	Serial Input Set-up Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	50 30	25 15		ns ns
t_H	Serial Input Hold Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	50 30	0 0		ns ns
t_S	Parallel Input Set-up Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	150 60	75 30		ns ns
t_H	Parallel Input Hold Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	50 30	0 0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		70 30	200 100	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		85 30	180 90	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.5 5.0	6.0 12		MHz MHz
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	10 5.0			μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



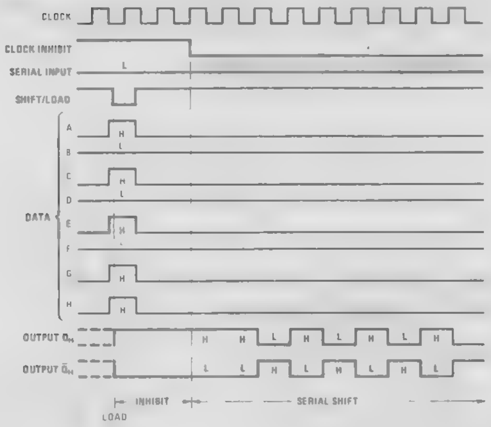
Note A The remaining six data and the serial input are low

Note B Prior to test high level data is loaded into H input

LOAD	INHIBIT	CLOCK	SERIAL					Q_H
				A	H	Q_A	Q_B	
L	X	X	X	a	h	a	b	h
H	L	L	X	X		Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X		H	Q_{An}	Q_{Gn}
H	L	↑	L	X		L	Q_{An}	Q_{Gn}
H	H	↑	X	X		Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$
X = irrelevant
↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$
a . . . h = the level at data inputs A thru H
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established
Q_{An}, Q_{6n} = the level of Q_A or Q_6 before the most recent ↑ transition of the clock

Logic Waveforms



National Semiconductor

MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The four D-type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus-organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flops to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive-going transition.

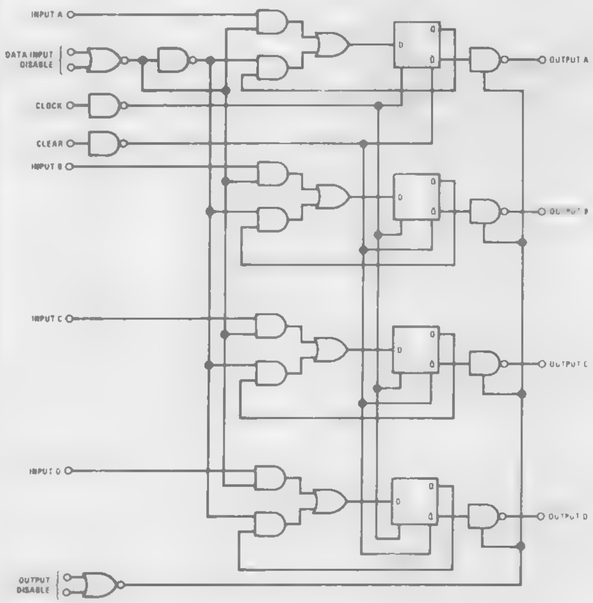
Features

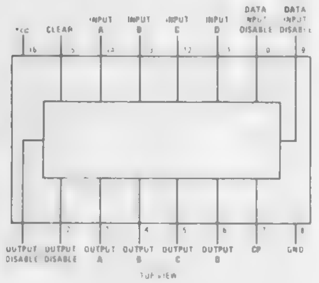
Supply voltage range	3V to 15V
Tenth power TTL compatible	Drive 2 LPTTL loads
High noise immunity	0.45 V_{CC} (typ.)
Low power	
Medium speed operation	
High impedance TRI-STATE	
Input disable without gating the clock	

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic Truth Table and Connection Diagrams





Truth Table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC} + 0.3\,V$
Operating Temperature Range	
MM54C173	−55°C to +125°C
MM74C173	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	−0.005		μA
	Output Current in High Impedance State	$V_{CC} = 15\,V$, $V_O = 15\,V$ $V_{CC} = 15\,V$, $V_O = 0\,V$	 −1.0	0.001 0.001	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	300	μA
	Low Power TTL/CMOS Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = -360\,\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = 360\,\mu A$			0.4 0.4	V V
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$, $T_A = 25°C$		500		ns
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0\,V$, $V_{IN(1)} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10\,V$, $V_{IN(1)} = 10\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

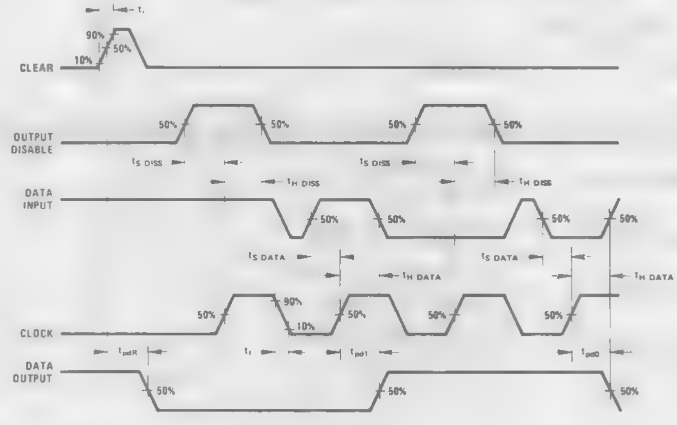
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Output	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		220 80	400 200	ns ns
t_S	Input Data Set-up Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		40 15	80 30	ns ns
t_H	Input Data Hold Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0	0 0	ns 0	 ns
t_S	Input Disable Set-up Time, $t_{S\ DISS}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 35	200 70	ns ns
t_H	Input Disable Hold Time, $t_{H\ DISS}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		0 0	0 0	ns ns
t_{1H}, t_{0H}	Delay from Output Disable to High Impedance State (from Logical "1" or Logical "0" Level)	$V_{CC} = 5.0\,V$, $R_L = 10\,k$ $V_{CC} = 10\,V$, $R_L = 10\,k$		170 70	340 140	ns ns
t_{H1}	Delay from Output Disable to Logical "1" Level (from High Impedance State)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		170 70	340 140	ns ns
t_{H0}	Delay from Output Disable to Logical "0" Level (from High Impedance State)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		170 70	340 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Clear to Output	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		240 90	490 180	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.0 7.0	4.0 12		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 70		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	10 5.0			μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)				

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



National Semiconductor

MM54C174/MM74C174 Hex D Flip-Flop

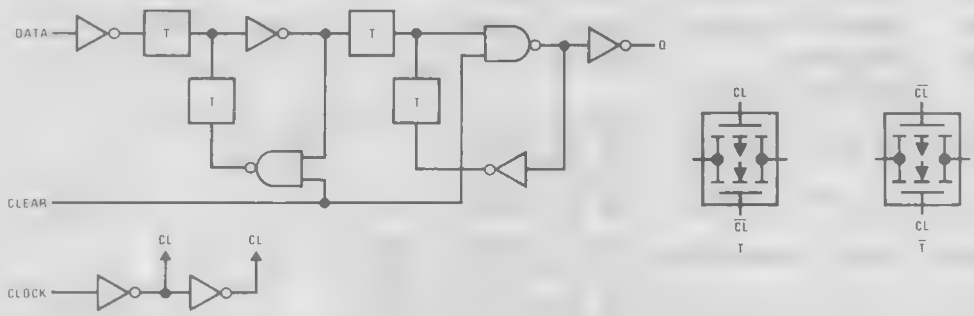
General Description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes To V_{CC} and GND.

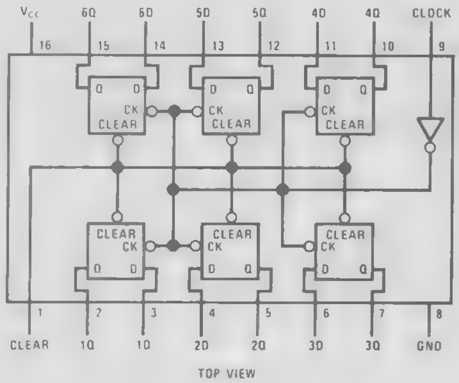
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Logic Diagrams



Connection Diagram



Truth Table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM54C174	−55°C to +125°C
MM74C174	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V, I_O = −10 μA V_{CC} = 10 V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, I_O = +10 μA V_{CC} = 10 V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V, V_{IN} = 0 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 μA 74C V_{CC} = 4.75 V, I_O = 360 μA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0 V T_A = 25°C, V_{OUT} = 0 V	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10 V T_A = 25°C, V_{OUT} = 0 V	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0	16		mA

t_{pd}	Propagation Delay Time to a Logical "0" from Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		110 50	300 110	ns ns
t_{S1}, t_{S0}	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0V$ $V_{CC} = 10V$	75 25			ns ns
t_{H1}, t_{H0}	Time after Clock Pulse that Data must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$	0 0	−10 −5.0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		50 35	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		65 35	140 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0	>1200 >1200		µs µs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	6.5 12		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		11 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		95		pF

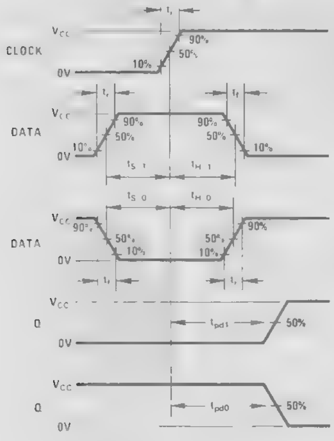
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

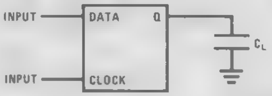
Switching Time Waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

AC Test Circuit



National Semiconductor

MM54C175/MM74C175 Quad D Flip-Flop

General Description

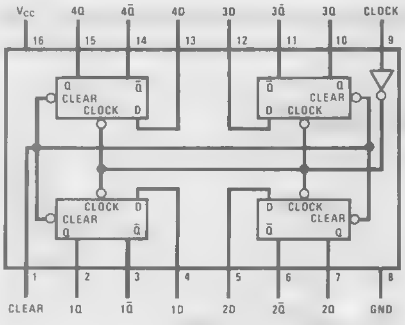
The MM54C175/MM74C175 consists of four positive-edge triggered D type flip-flops implemented with monolithic CMOS technology. Both are true and complemented outputs from each flip-flop are externally available. All four flip flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram and Truth Table



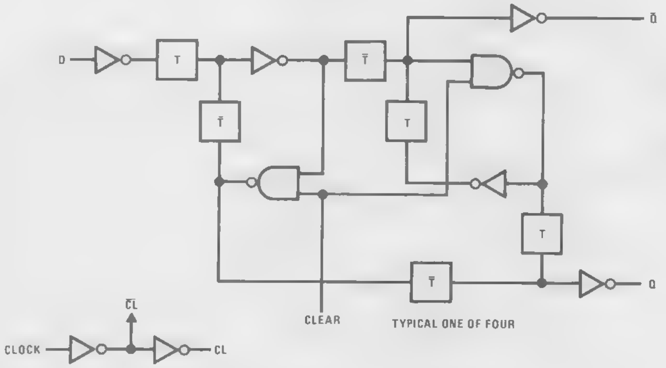
TOP VIEW

Each Flip-Flop

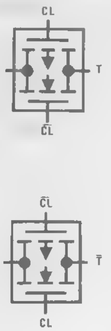
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

Logic Diagram



TYPICAL ONE OF FOUR



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C175	−55°C to +125°C
MM74C175	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\mu A$ $V_{CC} = 10V$, $I_O = -10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = +10\mu A$ $V_{CC} = 10V$, $I_O = +10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -360\mu A$ 74C $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = 360\mu A$ 74C $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$ $T_A = 25°C$, $V_{OUT} = 0V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$ $T_A = 25°C$, $V_{OUT} = 0V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		190 75	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay time to a Logical "1" from Clear to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		230 90	400 150	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	100 40	45 16		ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0 0	−11 −4		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		130 45	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 45	250 100	ns ns
t_r	Maximum Clock Rise Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0	450 125		μs μs
t_f	Maximum Clock Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0	50 50		μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.0	3.5 10		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		10 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		130		pF

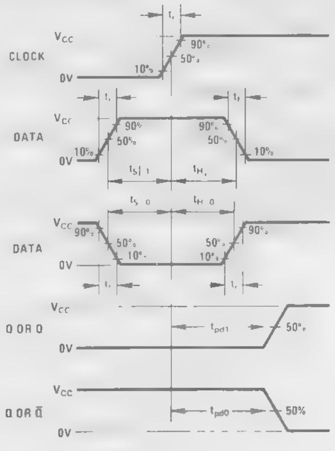
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

National Semiconductor

MM54C192/MM74C192 Synchronous 4-Bit Up/Down Decade Counter
MM54C193/MM74C193 Synchronous 4-Bit Up/Down Decade Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters, while the MM54C193 and MM74C193 are binary counters.

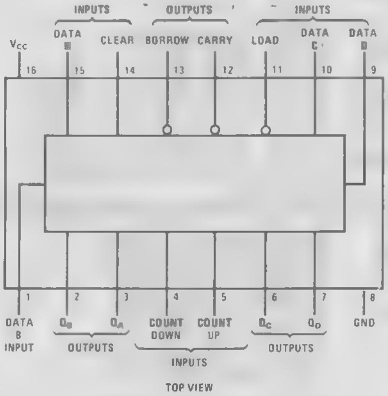
Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at a logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

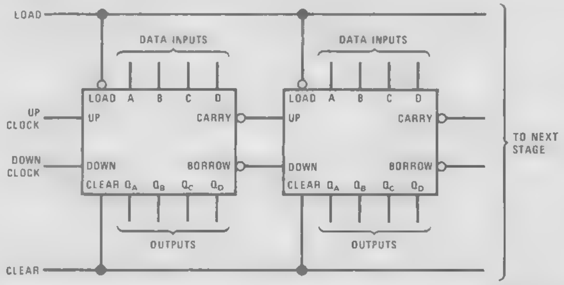
Features

■ High noise margin	1 V guaranteed
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ Wide supply range	3 V to 15 V
■ Carry and borrow outputs for N-bit cascading	
■ Asynchronous clear	
■ High noise immunity	0.45 V_{CC} (typ.)

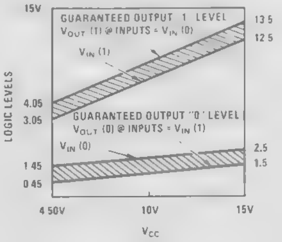
Connection Diagram



Cascading Packages



Guaranteed Noise Margin as A Function of V_{CC}



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM54C193	−55°C to +125°C
MM74C193	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V, I_O = −10 µA V_{CC} = 10 V, I_O = −10 µA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, I_O = +10 µA V_{CC} = 10 V, I_O = +10 µA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V, V_{IN} = 0 V	1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	µA
	CMOS to Tenth Power Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 µA 74C V_{CC} = 4.75 V, I_O = −360 µA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 µA 74C V_{CC} = 4.75 V, I_O = 360 µA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

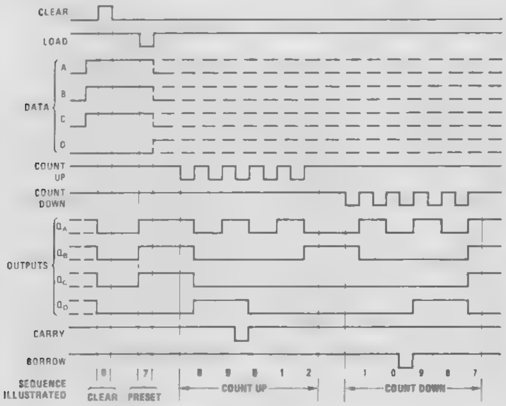
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to Q from Count Up or Down	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 100	400 160	ns ns
t_{pd}	Propagation Delay Time to Borrow from Count Down	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	200 80	ns ns
t_{pd}	Propagation Delay Time to Carry from Count Up	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	200 80	ns ns
t_S	Time Prior to Load that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 30	160 50	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		300 120	480 190	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 40	160 65	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to Q from Load	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		300 120	480 190	ns ns
t_W	Minimum Count Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 35	200 80	ns ns
f_{MAX}	Maximum Count Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.5 6	4 10		MHz MHz
t_r, t_f	Count Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			15 5	μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

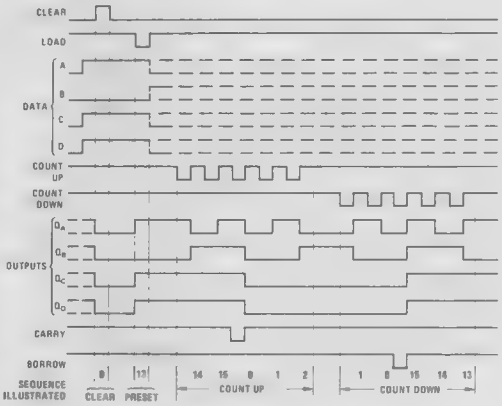
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Timing Diagrams



Note I: Clear outputs to zero.
Note II: Load (preset) to binary thirteen.
Note III: Count up to fourteen, fifteen, carry, zero, one and two.
Note IV: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

MM54C192/MM74C192

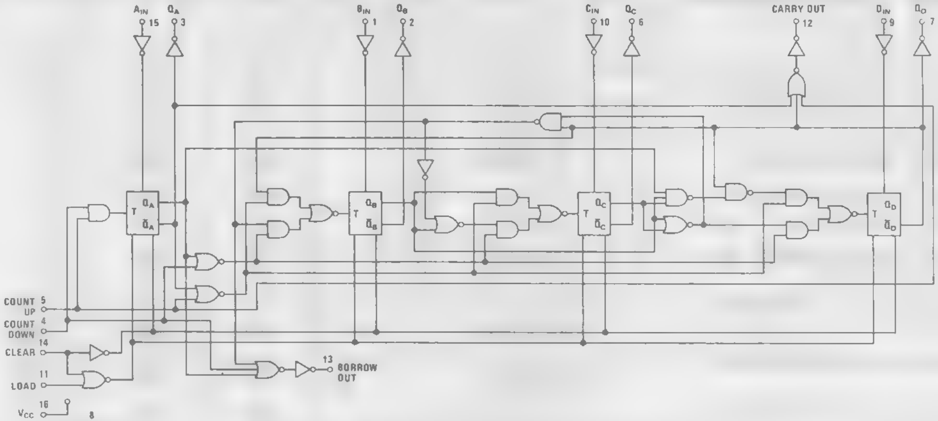


Note I: Clear outputs to zero.
Note II. Load (preset) to BCD seven.
Note III: Count up to eight, nine, carry, zero, one, and two.
Note IV: Count down to one, zero, borrow, nine, eight, and seven.

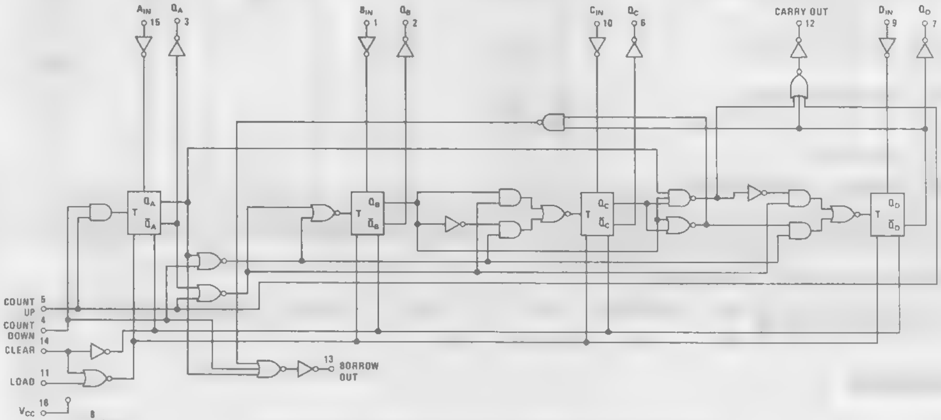
MM54C193/MM74C193

NOTE A. Clear overrides load, data, and count inputs.
NOTE B When counting up, count down input must be high; when counting down, count-up input must be high

Schematic Diagrams



MM54C192 Synchronous 4-Bit Up/Down Decade Counter



MM54C193 Synchronous 4-Bit Up/Down Binary Counter

National Semiconductor

MM54C195/MM74C195 4-bit Registers

General Description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible:

Parallel Load
Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control of input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D, or T-type flip flop as shown in the truth table.

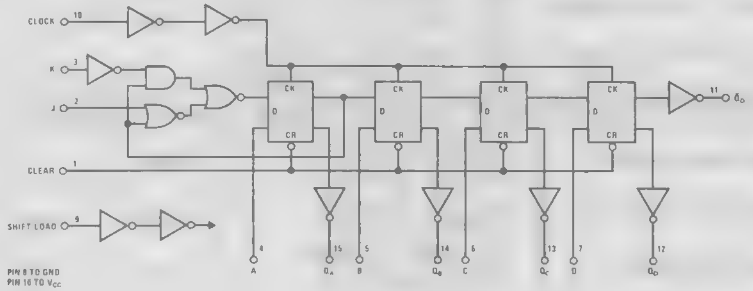
Features

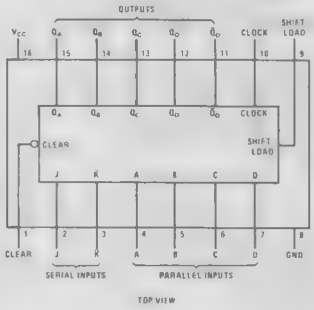
- Medium speed operation 8.5 MHz (typ.) with 10 V supply and 50 pF load
- High noise immunity 0.45 V_{CC} (typ.)
- Low power 100 nW (typ.)
- Tenth power TTL compatible drive 2 LPTTL loads
- Supply voltage range 3 V to 15 V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and K inputs to first stage
- Complementary outputs from last stage
- Positive-edge triggered clocking
- Diode clamped inputs to protect against static charge

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Schematic and Connection Diagrams





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM54C195	−55°C to +125°C
MM74C195	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

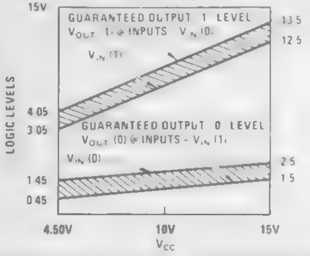
Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, V_{CC} = 10 V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5		 V	V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 μA 74C V_{CC} = 4.75 V, I_O = 360 μA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Truth Table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_A	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_A	Q_B	Q_C	Q_C
H	L	Q_{An}	Q_A	Q_B	Q_C	Q_C

Note: H HIGH LEVEL, L LOW LEVEL
t_n - bit time before clock pulse
t_{n+1} bit time after clock pulse
Q_{An} State of Q_A at t_n.

Guaranteed noise Margin as a Function of V_{CC}



AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

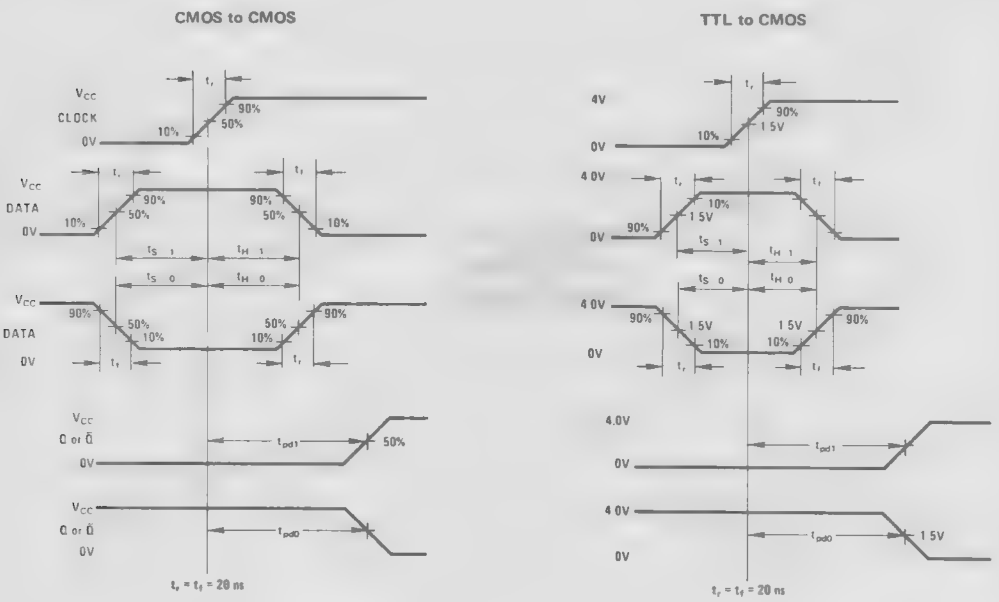
	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 75	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clear to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 50	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		80 35	200 70	ns ns
t_S	Time Prior to Clock Pulse that Shift/Load must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		110 60	150 90	ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		−10 −5.0	0 0	ns ns
t_W	Minimum Clear Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 50	200 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		90 40	130 60	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	5.0 2.0			µs µs
f_{MAX}	Maximum Input Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.5	3.0 8.5		MHz MHz
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



CMOS to CMOS

TTL to CMOS

National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW (typ.)
■ Internal address register	

See page 4-7
for detailed
specifications

National Semiconductor

MM54C221/MM74C221 Dual Monostable Multivibrator

General Description

The MM54C221/MM74C221 dual monostable multivibrator is a monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transtion-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}.

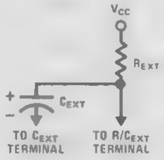
Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} R_{EXT}$. For further information and applications, see AN-138.

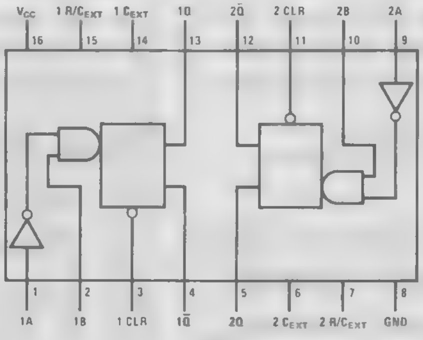
Features

■ Wide supply voltage range	4.5 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagrams

Timing Component





TOP VIEW

Truth Table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⊔ = One low level pulse
X = Irrelevant

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C221	−55°C to +125°C
MM74C221	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	4.5V to 15V
Absolute Maximum V_{CC}	18V
$R_{EXT} \geq 80 V_{CC}$ (Ω)	
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10 μA V_{CC} = 10V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current (Standby)	V_{CC} = 15V, R_{EXT} = ∞, Q1, Q2 = Logic "0" (Note 3)		0.05	300	μA
I_{CC}	Supply Current (During Output Pulse)	V_{CC} = 15V, Q1 = Logic "1", Q2 = Logic "0" (Figure 4)		15		mA
		V_{CC} = = 5.0V, Q1 = Logic "1", Q2 = Logic "0" (Figure 4)		2.0		mA
	Leakage Current at R/C_{EXT} Pin	V_{CC} = 15V, V_{CEXT} = 5.0V		0.01	3.0	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA 74C V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA 74C V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current (P-channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current (N-channel)	V_{CC} = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current (N-channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

$t_{pd\ A,B}$	Propagation Delay from Trigger Input (A,B) to Output Q, $\overline{Q}$	$V_{CC}=5.0V$		250	500	ns
		$V_{CC}=10V$		120	250	ns
$t_{pd\ CL}$	Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$	$V_{CC}=5.0V$		250	500	ns
		$V_{CC}=10V$		120	250	ns
t_S	Time Prior to Trigger Input (A,B) that Clear must be Set	$V_{CC}=5.0V$	150	50		ns
		$V_{CC}=10V$	60	20		ns
$t_{W(A,B)}$	Trigger Input (A,B) Pulse Width	$V_{CC}=5.0V$	150	50		ns
		$V_{CC}=10V$	70	30		ns
$t_{W(CL)}$	Clear Input (CL) Pulse Width	$V_{CC}=5.0V$	150	50		ns
		$V_{CC}=10V$	70	30		ns
$t_{W(OUT)}$	Q or $\overline{Q}$ Output Pulse Width	$V_{CC}=5.0V$, $R_{EXT}=10k$, $C_{EXT}=0pF$		900		ns
		$V_{CC}=10V$, $R_{EXT}=10k$, $C_{EXT}=0pF$		350		ns
		$V_{CC}=15V$, $R_{EXT}=10k$, $C_{EXT}=0pF$		320		ns
		$V_{CC}=5.0V$, $R_{EXT}=10k$, $C_{EXT}=1000pF$ (Fig. 1)	9.0	10.6	12.2	μs
		$V_{CC}=10V$, $R_{EXT}=10k$, $C_{EXT}=1000pF$ (Fig. 1)	9.0	10	11	μs
		$V_{CC}=15V$, $R_{EXT}=10k$, $C_{EXT}=1000pF$ (Fig. 1)	8.9	9.8	10.8	μs
		$V_{CC}=5.0V$, $R_{EXT}=10k$, $C_{EXT}=0.1\mu F$ (Fig. 2)	900	1020	1200	μs
		$V_{CC}=10V$, $R_{EXT}=10k$, $C_{EXT}=0.1\mu F$ (Fig. 2)	900	1000	1100	μs
		$V_{CC}=15V$, $R_{EXT}=10k$, $C_{EXT}=0.1\mu F$ (Fig. 2)	900	990	1100	μs
R_{ON}	ON Resistance of Transistor between R/C_{EXT} to C_{EXT}	$V_{CC}=5.0V$ (Note 4)		50	150	Ω
		$V_{CC}=10V$ (Note 4)		25	65	Ω
		$V_{CC}=15V$ (Note 4)		16.7	45	Ω
	Output Duty Cycle	$R=10k$, $C=1000pF$			90	%
		$R=10k$, $C=0.1\mu F$ (Note 5)			90	%
C_{IN}	Input Capacitance	R/C_{EXT} Input (Note 2)		15	25	pF
		Any Other Input (Note 2)		5.0		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: In Standby (Q = Logic "0") the power dissipated equals the leakage current plus V_{CC}/R_{EXT}.

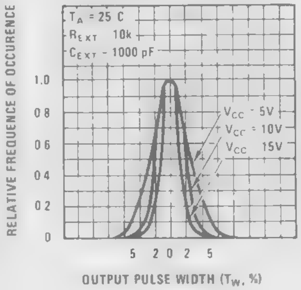
Note 4: See AN-138 for detailed explanation of R_{ON}.

Note 5: Maximum output duty cycle = $R_{EXT} / R_{EXT} + 1000$.

Typical Performance Characteristics

Figure 1

Typical Distribution of Units for Output Pulse Width



0% Point pulse width

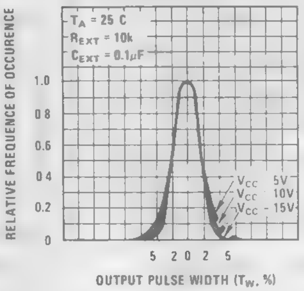
At V_{CC} = 5V, T_W = 10.6μs
At V_{CC} = 10V, T_W = 10μs
At V_{CC} = 15V, T_W = 9.8μs

Percentage of units within ±4%:

At V_{CC} = 5V, 90% of units
At V_{CC} = 10V, 95% of units
At V_{CC} = 15V, 98% of units

Figure 2

Typical Distribution of Units for Output Pulse Width



0% Point pulse width:

At V_{CC} = 5V, T_W = 1020μs
At V_{CC} = 10V, T_W = 1000μs
At V_{CC} = 15V, T_W = 982μs

Percentage of units within ±4%:

At V_{CC} = 5V, 95% of units
At V_{CC} = 10V, 97% of units
At V_{CC} = 15V, 98% of units

Figure 3

Typical Variation in Output Pulse Width vs Temperature

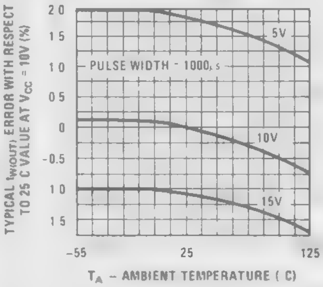
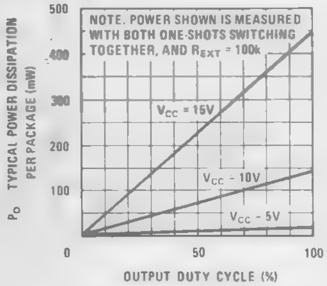
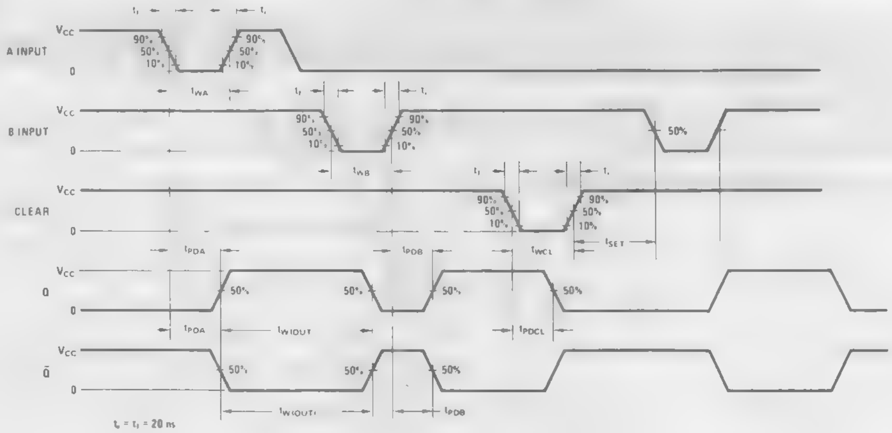


Figure 4

Typical Power Dissipation per Package



Switching Time Waveforms



National Semiconductor

MM54C240/MM74C240 Inverting MM54C244/MM74C244 Non-Inverting Octal Buffers and Line Drivers with TRI-STATE® Outputs

General Description

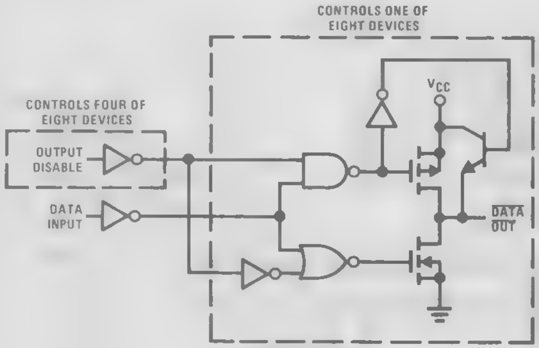
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state. For improved TTL input compatibility see MM74C941.

Features

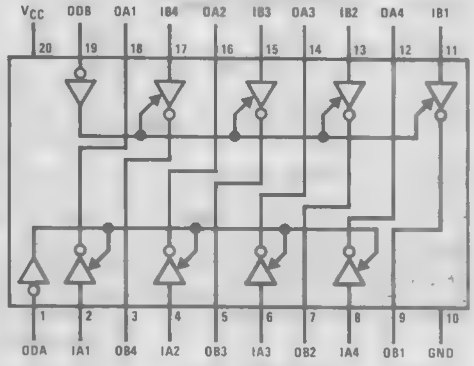
- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 V_{CC} typ)
- Low power consumption
- High capacitive load drive capability
- TRI-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

Logic and Connection Diagrams

MM54C240/MM74C240

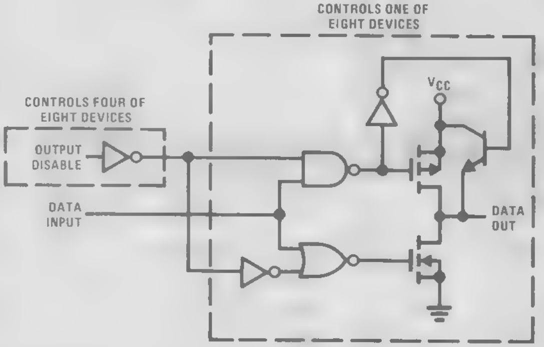

CONTROLS ONE OF EIGHT DEVICES
V_{CC}
CONTROLS FOUR OF EIGHT DEVICES
OUTPUT DISABLE
DATA INPUT
$\overline{\text{DATA OUT}}$

MM54C240/MM74C240
Dual-In-Line Package

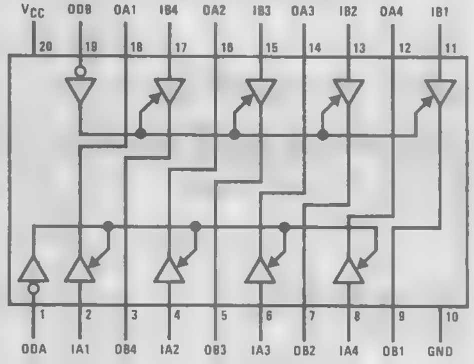


TOP VIEW

MM54C244/MM74C244



MM54C244/MM74C244
Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C240, MM54C244	$-55°C$ to $+125°C$
MM74C240, MM74C244	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC}=5.0V$	3.5			V
	$V_{CC}=10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC}=5.0V$			1.5	V
	$V_{CC}=10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC}=5.0V$, $I_O=-10\ \mu A$	4.5			V
	$V_{CC}=10V$, $I_O=-10\ \mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC}=5.0V$, $I_O=10\ \mu A$			0.5	V
	$V_{CC}=10V$, $I_O=10\ \mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
Supply Current (I_{CC})	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
	74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC}=4.5V$			0.8	V
	74C, $V_{CC}=4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC}=4.5V$, $I_O=-450\ \mu A$	$V_{CC}-0.4$			V
	74C, $V_{CC}=4.75V$, $I_O=-450\ \mu A$	$V_{CC}-0.4$			V
	54C, $V_{CC}=4.5V$, $I_O=-2.2$ mA	2.4			V
	74C, $V_{CC}=4.75V$, $I_O=-2.2$ mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC}=4.5V$, $I_O=2.2$ mA			0.4	V
	74C, $V_{CC}=4.75V$, $I_O=2.2$ mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−14.0	−30.0		mA
	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−36.0	−70.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	12.0	20.0		mA
	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	48.0	70.0		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

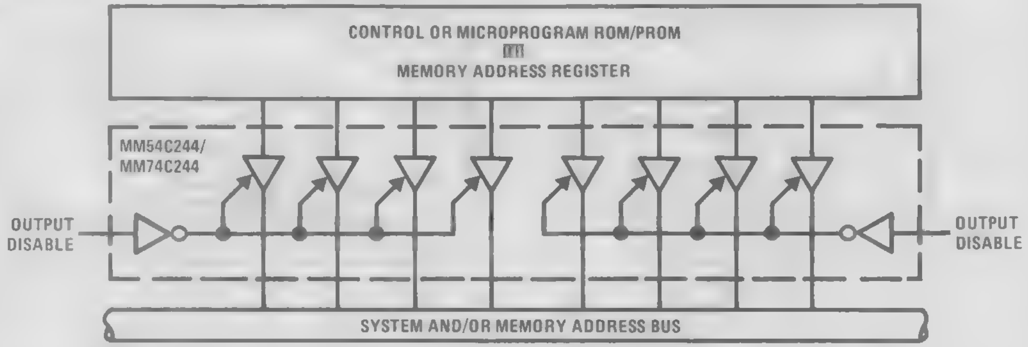
Parameter		Conditions	Min	Typ	Max	Units
$t_{Pd(1)}$, $t_{Pd(0)}$	Propagation Delay (Data In to Out)					
	MM54C240/MM74C240	$V_{CC} = 5V$, $C_L = 50$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		40	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		80	110	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		60	90	ns
	MM54C244/MM74C244	$V_{CC} = 5V$, $C_L = 50$ pF		45	70	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		25	50	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	70	ns
t_{1H}, t_{0H}	Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		45	80	ns
		$V_{CC} = 10V$		35	60	ns
t_H, t_H	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
$t_{T(HL)}$, $t_{T(LH)}$	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		45	80	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		30	60	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		75	140	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled Per Buffer)	(See Note 3)				
	MM54C240/MM74C240			100		pF
	MM54C244/MM74C244			100		pF
	(Output Disabled Per Buffer)					
	MM54C240/MM74C240			10		pF
	MM54C244/MM74C244			0		pF
C_{IN}	Input Capacitance (Any Input)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF
C_O	Output Capacitance (Output Disabled)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Typical Application



Truth Tables

MM54C240/MM74C240

ODA	IA	OA
1	X	Z
1	X	Z
0	0	1
0	1	0

ODB	IB	OB
1	X	Z
1	X	Z
0	0	1
0	1	0

MM54C244/MM74C244

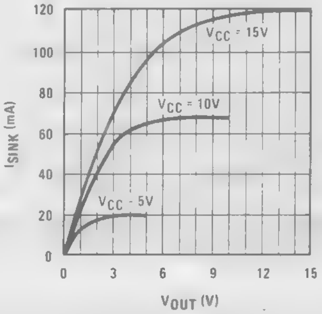
ODA	IA	OA
1	X	Z
1	X	Z
0	0	0
0	1	1

ODB	IB	OB
1	X	Z
1	X	Z
0	0	0
0	1	1

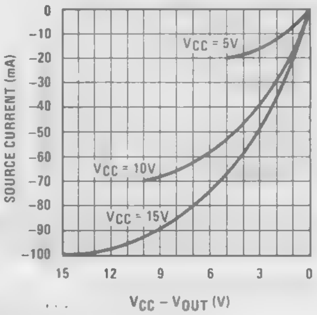
1 = High
0 = Low
X = Don't Care
Z = TRI-STATE

Typical Performance Characteristics

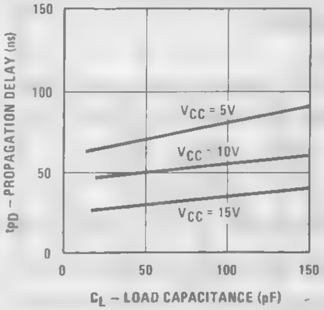
N-Channel Output Drive @ 25°C



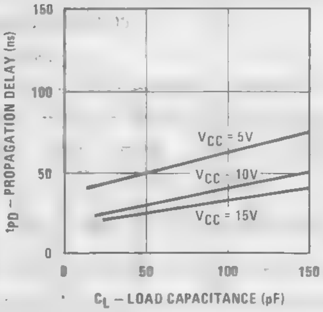
P-Channel Output Drive @ 25°C



MM54C240/MM74C240 Propagation Delay Vs. Load Capacitance

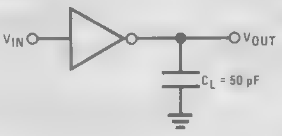


MM54C244/MM74C244 Propagation Delay Vs. Load Capacitance

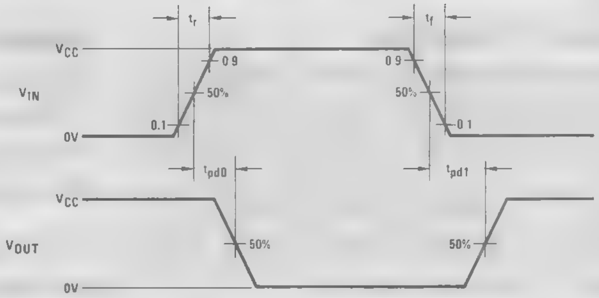


AC Test Circuits and Switching Time Waveforms

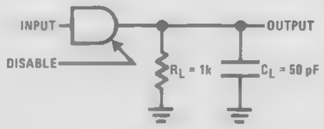
t_{pd0}, t_{pd1}



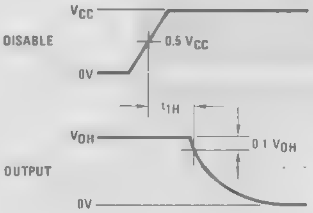
CMOS to CMOS



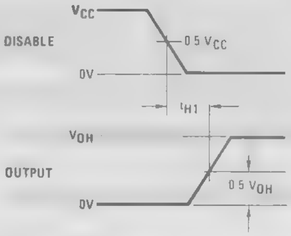
t_{1H} and t_{H1}



t_{1H}

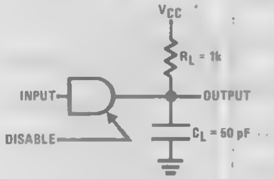


t_{H1}

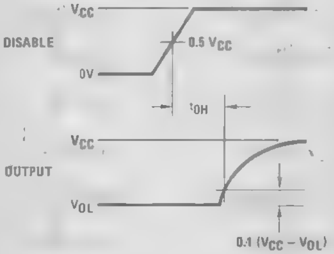


Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

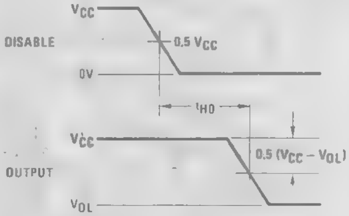
t_{0H} and t_{H0}



t_{0H}



t_{H0}



Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch MM54C374/MM74C374 TRI-STATE® Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

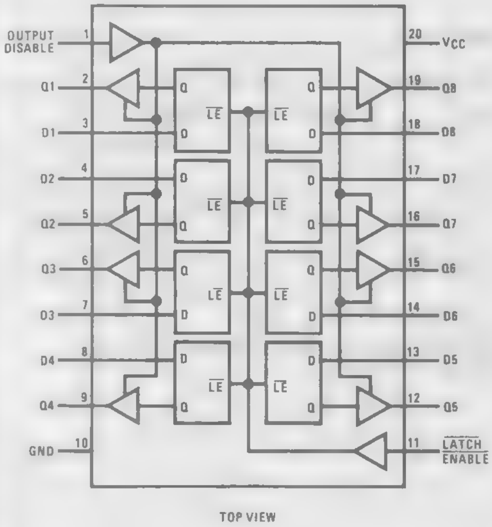
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300″ pin centers.

Features

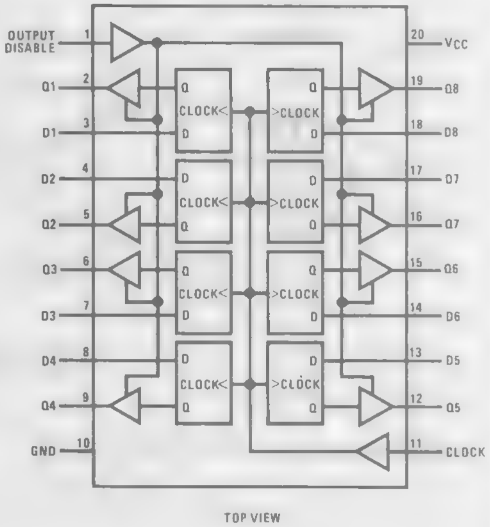
Wide supply voltage range	3.0 V to 15 V
High noise immunity	0.45 V_{CC} (typ.)
Low power consumption	
TTL compatibility	fan-out of 1 driving standard TTL
Bus driving capability	
TRI-STATE outputs	
Eight storage elements in one package	
Single CLOCK/$\overline{\text{LATCH ENABLE}}$ and OUTPUT DISABLE control inputs	
20-pin dual-in-line package with 0.300″ centers takes half the board space of a 24-pin package	

Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package



MM54C374/MM74C374
Dual-In-Line Package



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM54C373	−55°C to +125°C
MM74C373	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\,\mu A$ $V_{CC} = 10\,V$, $I_O = -10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = +10\,\mu A$ $V_{CC} = 10\,V$, $I_O = +10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0	−0.005		μA
I_{OZ}	TRI-STATE® Leakage Current	$V_{CC} = 15\,V$, $V_O = 15\,V$ $V_{CC} = 15\,V$, $V_O = 0\,V$	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$			0.8 0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = -360\,\mu A$	$V_{CC} - 0.4$ $V_{CC} - 0.4$			V
		54C $V_{CC} = 4.5\,V$, $I_O = -1.6\,mA$ 74C $V_{CC} = 4.75\,V$, $I_O -1.6\,mA$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 1.6\,mA$ 74C $V_{CC} = 4.75\,V$, $I_O = 1.6\,mA$			0.4 0.4	V V
	Output Drive (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0\,V$, $V_{OUT} = 0\,V$ $T_A = 25°C$ (Note 4)	−12	−24		mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10\,V$, $V_{OUT} = 0\,V$ $T_A = 25°C$ (Note 4)	−24	−48		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$ (Note 4)	6.0	12		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10\,V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$ (Note 4)	24	48		mA

AC Electrical Characteristics

MM54C373/MM74C373 $T_A = 25°C$, $C_L = 50\,pF$, $t_r = t_f = 20\,ns$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay, LATCH/ENABLE to Output	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		165	330	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		70	140	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		195	390	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		85	170	ns
t_{pd0}, t_{pd1}	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}} = V_{CC}$				
		$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		155	310	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		70	140	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		185	370	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		85	170	ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE	$t_{HOLD} = 0\,ns$				
		$V_{CC} = 5.0\,V$		70	140	ns
		$V_{CC} = 10\,V$		35	70	ns
f_{MAX}	Maximum $\overline{\text{LATCH ENABLE}}$ Frequency	$V_{CC} = 5.0\,V$	3.3	6.7		MHz
		$V_{CC} = 10\,V$	4.5	9.0		MHz
t_{PWH}	Minimum $\overline{\text{LATCH ENABLE}}$ Pulse Width	$V_{CC} = 5.0\,V$		75	150	ns
		$V_{CC} = 10\,V$		55	110	ns
t_r, t_f	Maximum $\overline{\text{LATCH ENABLE}}$ Rise and Fall Time	$V_{CC} = 5.0\,V$		NA		μs
		$V_{CC} = 10\,V$		NA		μs
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		65	130	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		35	70	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		110	220	ns
		$V_{CC} = 10\,V$, $C_L 150\,pF$		70	140	ns
C_{LE}	Input Capacitance	$\overline{\text{LE}}$ Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		200		pF

AC Electrical Characteristics

MM54C374/MM74C374 $T_A = 25°C$, $C_L = 50\,pF$, $t_r = t_f = 20\,ns$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay, CLOCK to Output	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		150	300	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		65	130	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		180	360	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		80	160	ns
$t_{SET\text{-}UP}$	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0\,ns$				
		$V_{CC} = 5.0\,V$		70	140	ns
		$V_{CC} = 10\,V$		35	70	ns
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	$V_{CC} = 5.0\,V$		70	140	ns
		$V_{CC} = 10\,V$		50	100	ns
f_{MAX}	Maximum CLOCK Frequency	$V_{CC} = 5.0\,V$	3.5	7.0		MHz
		$V_{CC} = 10\,V$	5.0	10		MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		65	130	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		35	70	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		110	220	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		70	140	ns
t_r, t_f	Maximum CLOCK Rise and Fall Time	$V_{CC} = 5.0\,V$	15	>2000		μs
		$V_{CC} = 10\,V$	5.0	>2000		μs
C_{CLK}	Input Capacitance	CLOCK Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		250		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

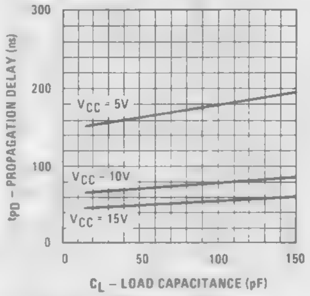
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

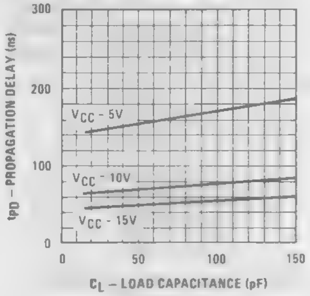
Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

Typical Performance Characteristics $T_A = 25°C$

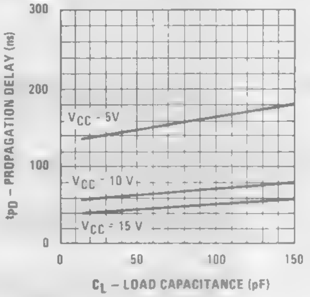
MM54C373/MM74C373 Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output vs Load Capacitance



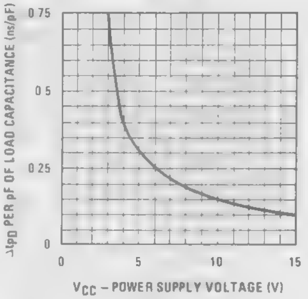
MM54C373/MM74C373 Propagation Delay, Data In to Output vs Load Capacitance



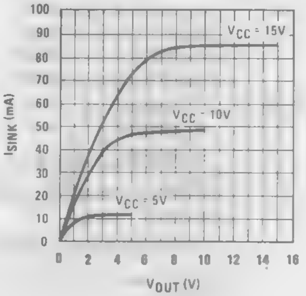
MM54C374/MM74C374 Propagation Delay, CLOCK to Output vs Load Capacitance



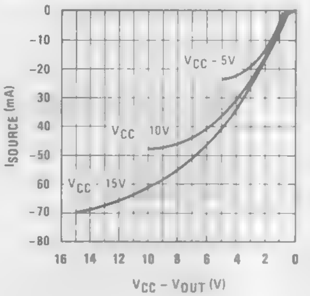
MM54C373/MM74C373, MM54C374/MM74C374 Change in Propagation Delay per pF of Load Capacitance (Δt_{PD}/pF) vs Power Supply Voltage



MM54C373/MM74C373, MM54C374/MM74C374 Output Sink Current vs V_{OUT}



MM54C373/MM74C373, MM54C374/MM74C374 Output Source Current vs $V_{CC} - V_{OUT}$



Truth Tables

MM54C373/MM74C373

OUTPUT DISABLE	$\overline{\text{LATCH ENABLE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

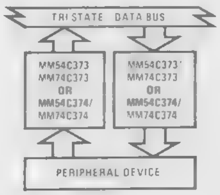
MM54C374/MM74C374

OUTPUT DISABLE	CLOCK	D	Q
L	_/‾	H	H
L	_/‾	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

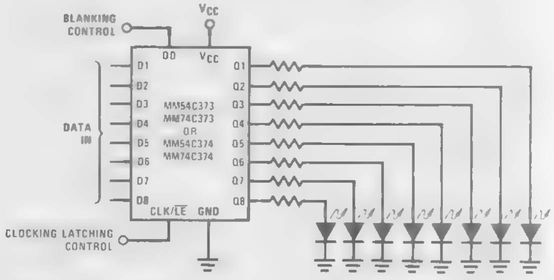
L = low logic level
H = high logic level
X = irrelevant
_/‾ = low to high logic level transition
Q = preexisting output level
Hi-Z = high impedance output state

Typical Applications

Data Bus Interfacing Element

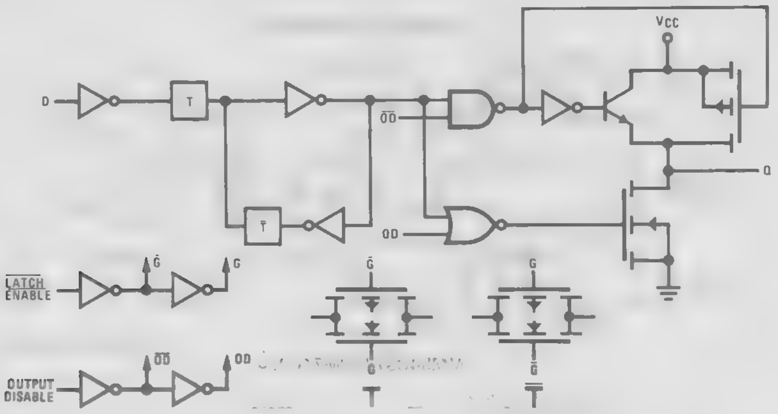


Simple, Latching, Octal, LED Indicator Driver with Blanking For Use As Data Display, Bus Monitor, μP Front Panel Display, Etc.

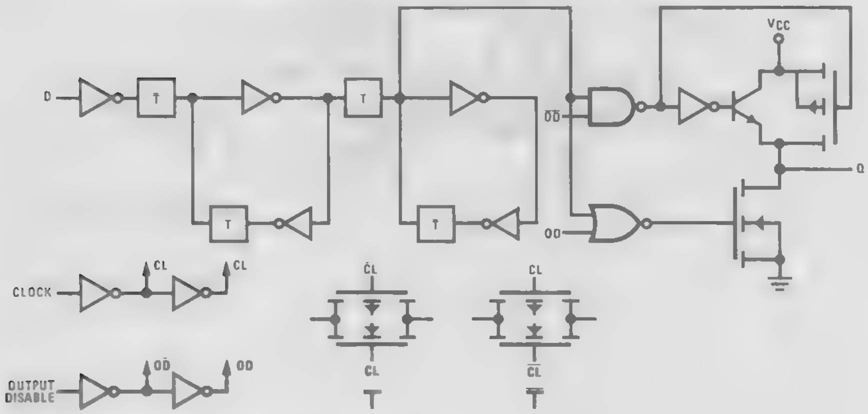


Logic Diagrams

MM54C373/MM74C373 (1 of 8 Latches)

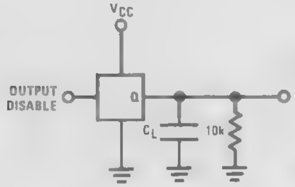


MM54C374/MM74C374 (1 of 8 Flip-Flops)

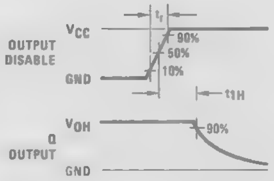


TRI-STATE® Test Circuits and Timing Diagrams

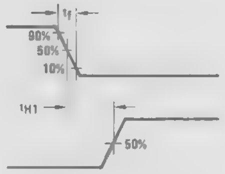
t_{1H}, t_{H1}



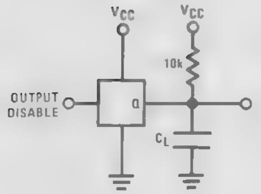
t_{1H}, $C_L = 5$ pF



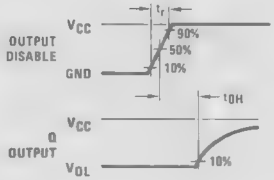
t_{H1}, $C_L = 50$ pF



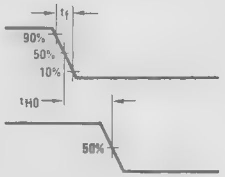
t_{0H}, t_{H0}



t_{0H}, $C_L = 5$ pF

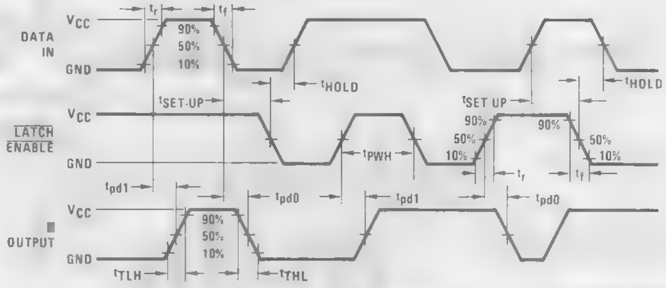


t_{H0}, $C_L = 50$ pF



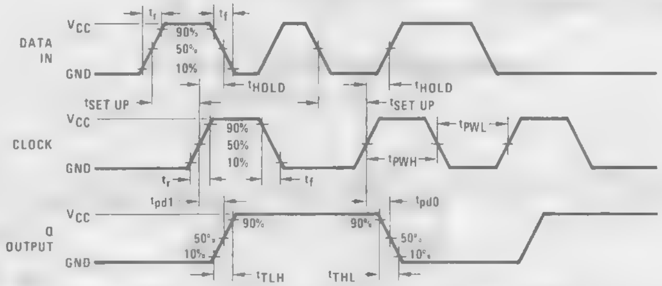
Switching Time Waveforms

MM54C373/MM74C373



OUTPUT DISABLE = GND

MM54C374/MM74C374



OUTPUT DISABLE = GND

National Semiconductor

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers
MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE® Hex Inverters

General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

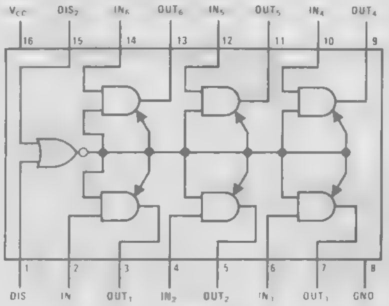
■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	$0.45 V_{CC}$ (typ.)
■ TTL compatible	drive 1 TTL Load

Applications

■ Bus drivers	Typical propagation delay into 150 pF load is 40 ns.

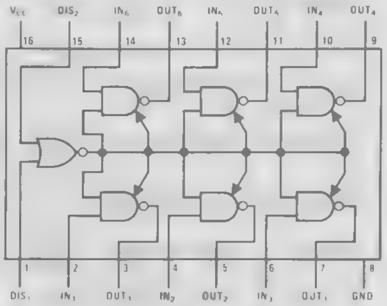
Connection Diagrams (Dual-In-Line and Flat Packages)

MM70C95/MM80C95



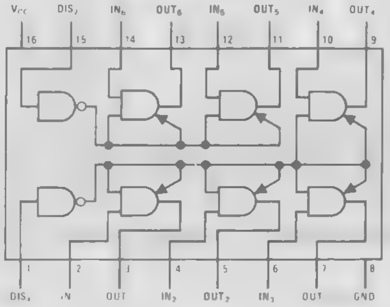
TOP VIEW

MM70C96/MM80C96



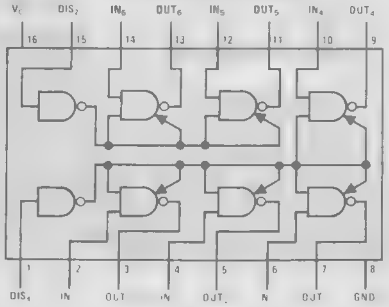
TOP VIEW

MM70C97/MM80C97



TOP VIEW

MM70C98/MM80C98



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM70CXX	−55°C to +125°C
MM80CXX	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Power Supply Voltage (V_{CC})	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	−0.005		μA
I_{OUT}	Output Current in High Impedance State	$V_{CC} = 15\,V$, $V_O = 15\,V$ $V_{CC} = 15\,V$, $V_O = 0\,V$	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.01	15	μA
	TTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	70C $V_{CC} = 4.5\,V$ 80C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	70C $V_{CC} = 4.5\,V$ 80C $V_{CC} = 4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	70C $V_{CC} = 4.5\,V$, $I_O = -1.6\,mA$ 80C $V_{CC} = 4.75\,V$, $I_O = -1.6\,mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	70C $V_{CC} = 4.5\,V$, $I_O = 1.6\,mA$ 80C $V_{CC} = 4.75\,V$, $I_O = 1.6\,mA$			0.4 0.4	V V
	Output Drive (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0\,V$, $V_{IN(1)} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−4.35			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10\,V$, $V_{IN(1)} = 10\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−20			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	4.35			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10\,V$, $V_{IN(0)} = 0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	20			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5.0\,V$		60	100	ns
		$V_{CC} = 10\,V$		25	40	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5.0\,V$		70	150	ns
		$V_{CC} = 10\,V$		35	75	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		85	160	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		40	80	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		95	210	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		45	110	ns
t_{1H}, t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5.0\,pF$				
	MM70C95/MM80C95	$V_{CC} = 5.0\,V$		80	135	ns
		$V_{CC} = 10\,V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5.0\,V$		100	180	ns
		$V_{CC} = 10\,V$		70	125	ns
	MM70C97/MM80C97	$V_{CC} = 5.0\,V$		70	125	ns
		$V_{CC} = 10\,V$		50	90	ns
	MM70C98/MM80C98	$V_{CC} = 5.0\,V$		90	170	ns
		$V_{CC} = 10\,V$		70	125	
t_{H1}, t_{H0}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$R_L = 10k$, $C_L = 50\,pF$				
	MM70C95/MM80C95	$V_{CC} = 5.0\,V$		120	200	ns
		$V_{CC} = 10\,V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5.0\,V$		130	225	ns
		$V_{CC} = 10\,V$		60	110	ns
	MM70C97/MM80C97	$V_{CC} = 5.0\,V$		95	175	ns
		$V_{CC} = 10\,V$		40	80	ns
	MM70C98/MM80C98	$V_{CC} = 5.0\,V$		120	200	ns
		$V_{CC} = 10\,V$		50	90	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE	Any Output (Note 2)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

Truth Table

MM70C95/MM80C95

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

MM70C98/MM80C98

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

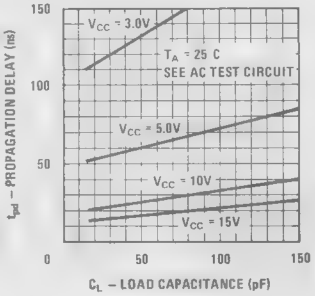
*Output 5-6 only

**Output 1-4 only

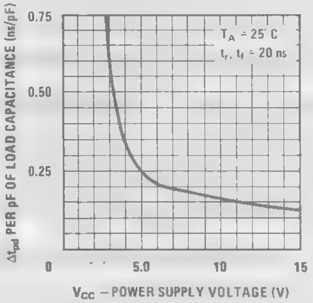
X = Irrelevant

Typical Performance Characteristics

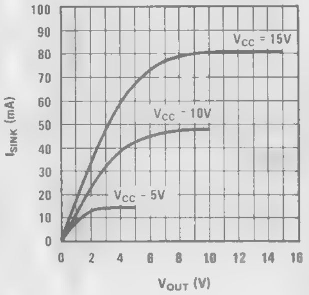
Propagation Delay vs Load Capacitance



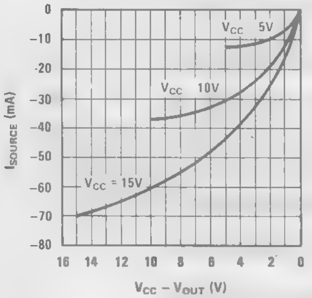
Δt_{pd}/pF vs Power Supply Voltage



N-Channel Output Drive @ 25°C

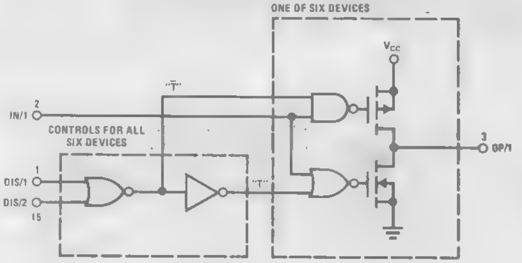


P-Channel Output Drive @ 25°C

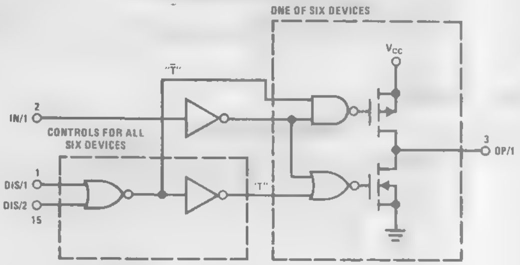


Schematic Diagram

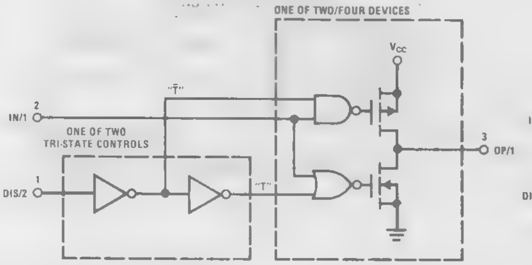
MM70C95/MM80C95 TRI-STATE



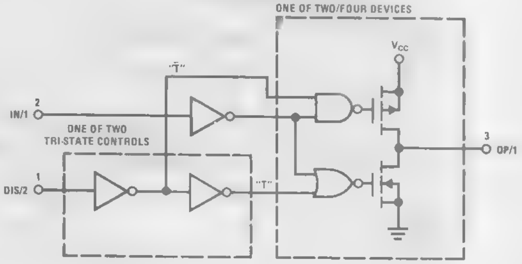
MM70C96/MM80C96 TRI-STATE



MM70C97/MM80C97 TRI-STATE

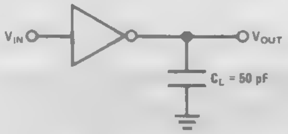


MM70C98/MM80C98 TRI-STATE

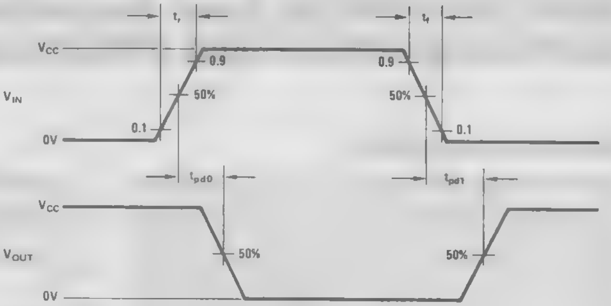


AC Test Circuit and Switching Time Waveforms

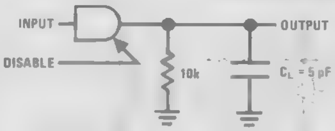
t_{pd0}, t_{pd1}



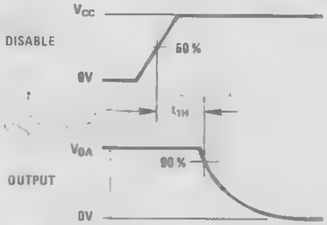
CMOS to CMOS



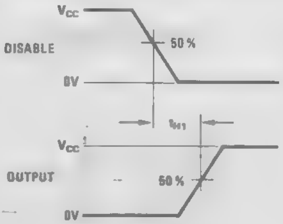
t_{1H} and t_{H1}



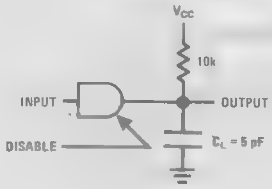
t_{1H}



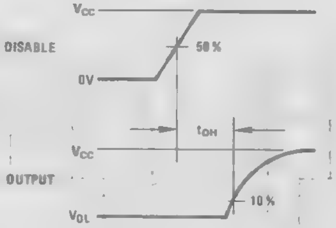
t_{H1}



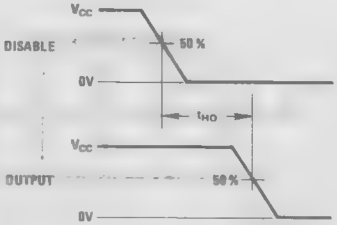
t_{0H} and t_{H0}



t_{0H}



t_{H0}



Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

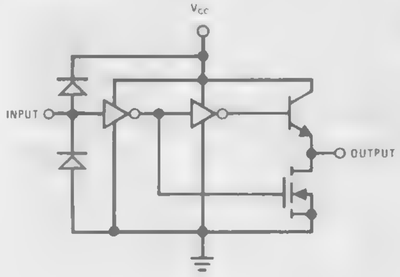
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

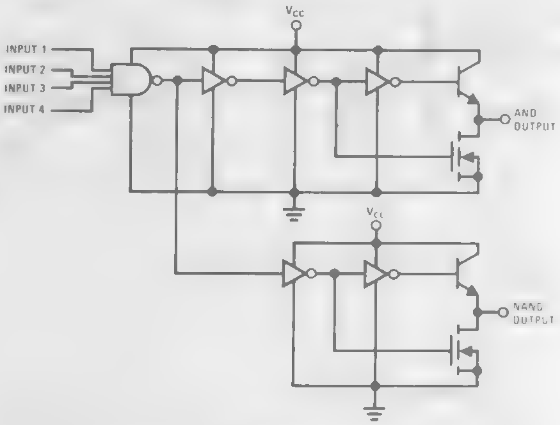
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low output ON resistance	20Ω (typ.)

Logic and Connection Diagrams

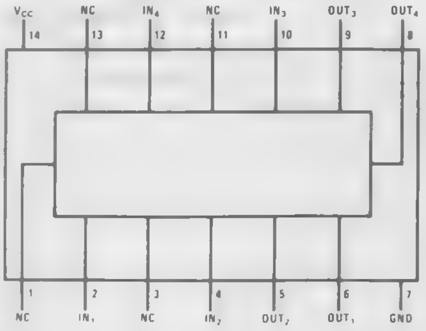
1/4 MM78C29/MM88C29



1/2 MM78C30/MM88C30

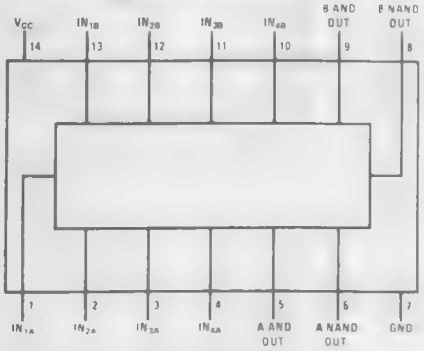


MM78C29/MM88C29



TOP VIEW

MM78C30/MM88C30



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin (Note 1)	−0.3 V to V_{CC} + 16 V
Operating Temperature Range	
MM78C29/MM78C30	−55°C to +125°C
MM88C29/MM88C30	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Average Current at Output	
MM78C30/MM88C30	50 mA
MM78C29/MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS					
$V_{IN(1)}$ Logical "1" Input Voltage	$V_{CC} = 5.0$ V	3.5			V
	$V_{CC} = 10$ V	8.0			V
$V_{IN(0)}$ Logical "0" Input Voltage	$V_{CC} = 5.0$ V			1.5	V
	$V_{CC} = 10$ V			2.0	V
$I_{IN(1)}$ Logical "1" Input Current	$V_{CC} = 15$ V, $V_{IN} = 15$ V		0.005	1.0	μA
$I_{IN(0)}$ Logical "0" Input Current	$V_{CC} = 15$ V, $V_{IN} = 0$ V	−1.0	−0.005		μA
I_{CC} Supply Current	$V_{CC} = 15$ V		0.05	100	μA
Output Drive					
Output Source Current MM78C29/MM78C30	$V_{OUT} = V_{CC} - 1.6$ V, $V_{CC} \geqslant 4.5$ V, $T_j = 25$°C	−57	−80		mA
	$T_j = 125$°C	−32	−50		mA
MM88C29/MM88C30	$V_{OUT} = V_{CC} - 1.6$ V, $V_{CC} \geqslant 4.75$ V, $T_j = 25$°C	−47	−80		mA
	$T_j = 85$°C	−32	−60		mA
MM78C29/MM88C29 MM78C30/MM88C30	$V_{OUT} = V_{CC} - 0.8$ V $V_{CC} \geqslant 4.5$ V	−2.0	−20		mA
Output Sink Current MM78C29/MM78C30	$V_{OUT} = 0.4$ V, $V_{CC} = 4.50$ V, $T_j = 25$°C	11	20		mA
	$T_j = 125$°C	8.0	14		mA
	$V_{OUT} = 0.4$ V, $V_{CC} = 10$ V, $T_j = 25$°C	22	40		mA
	$T_j = 125$°C	16	28		mA
MM88C29/MM88C30	$V_{OUT} = 0.4$ V, $V_{CC} = 4.75$ V, $T_j = 25$°C	9.5	22		mA
	$T_j = 85$°C	8.0	18		mA
	$V_{OUT} = 0.4$ V, $V_{CC} = 10$ V, $T_j = 25$°C	19	40		mA
	$T_j = 125$°C	15.5	33		mA
Output Source Resistance MM78C29/MM78C30	$V_{OUT} = V_{CC} - 1.6$ V, $V_{CC} \geqslant 4.5$ V, $T_j = 25$°C		20	28	Ω
	$T_j = 125$°C		32	50	Ω
MM88C29/MM88C30	$V_{OUT} = V_{CC} - 1.6$ V, $V_{CC} \geqslant 4.75$ V, $T_j = 25$°C		20	34	Ω
	$T_j = 85$°C		27	50	Ω

DC Electrical Characteristics (cont'd)

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Sink Resistance					
MM78C29/MM78C30	$V_{OUT} = 0.4\,V$, $V_{CC} = 4.50\,V$,				
	$T_j = 25°C$		20	36	Ω
	$T_j = 125°C$		28	50	Ω
	$V_{OUT} = 0.4\,V$, $V_{CC} = 10\,V$,				
	$T_j = 25°C$		10	18	Ω
	$T_j = 125°C$		14	25	Ω
MM88C29/MM88C30	$V_{OUT} = 0.4\,V$, $V_{CC} = 4.75\,V$,				
	$T_j = 25°C$		18	41	Ω
	$T_j = 85°C$		22	50	Ω
	$V_{OUT} = 0.4\,V$, $V_{CC} = 10\,V$,				
	$T_j = 25°C$		10	21	Ω
	$T_j = 85°C$		12	26	Ω
Output Resistance Temperature Coefficient					
Source			0.55		%/°C
Sink			0.40		%/°C
θ_{JA} Thermal Resistance					
MM78C29/MM78C30 (D-Package)			100		°C/W
MM88C29/MM88C30 (N-Package)			150		°C/W

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$

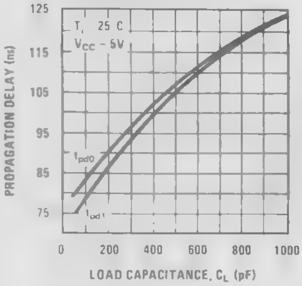
Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd} Propagation Delay Time to Logical "1" or "0"	*(See Figure 2)*				
MM78C29/MM88C29	$V_{CC} = 5.0\,V$		80	200	ns
	$V_{CC} = 10\,V$		35	100	ns
MM78C30/MM88C30	$V_{CC} = 5.0\,V$		110	350	ns
	$V_{CC} = 10\,V$		50	150	ns
t_{pd} Differential Propagation Delay Time to Logical "1" or "0"	$R_L = 100\,\Omega$, $C_L = 5000\,pF$ *(See Figure 1)*				
MM78C30/MM88C30	$V_{CC} = 5.0\,V$			400	ns
	$V_{CC} = 10\,V$			150	ns
C_{IN} Input Capacitance					
MM78C29/MM88C29	(Note 3)		5.0		pF
MM78C30/MM88C30	(Note 3)		5.0		pF
C_{PD} Power Dissipation Capacitance					
MM78C29/MM88C29	(Note 3)		150		pF
MM78C30/MM88C30	(Note 3)		200		pF

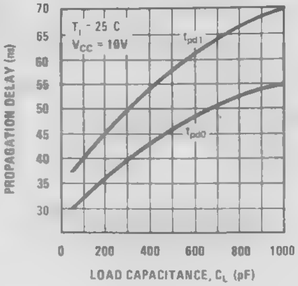
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

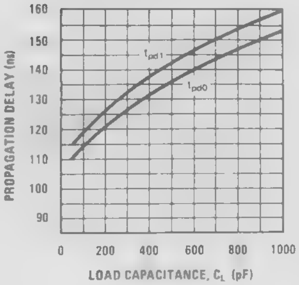
Note 2: Capacitance is guaranteed by periodic testing.

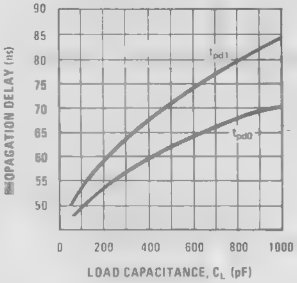
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

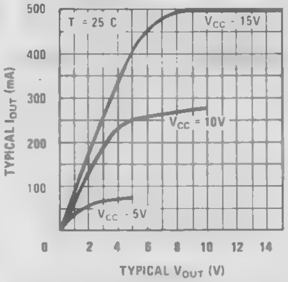
Typical Performance Characteristics

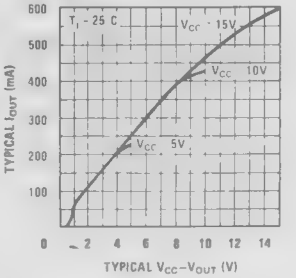

MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance


MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance


MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance


MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance


Typical Sink Current vs Output Voltage


Typical Source Current vs Output Voltage

AC Test Circuits

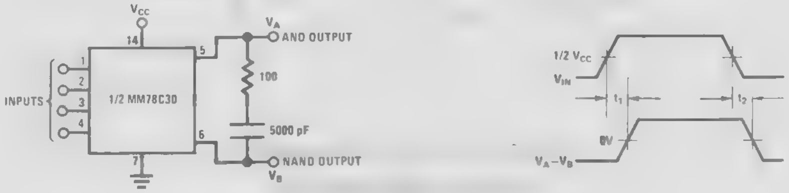


FIGURE 1.

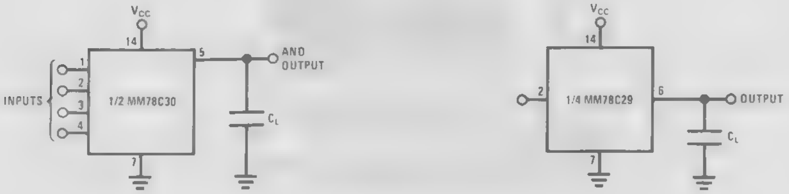
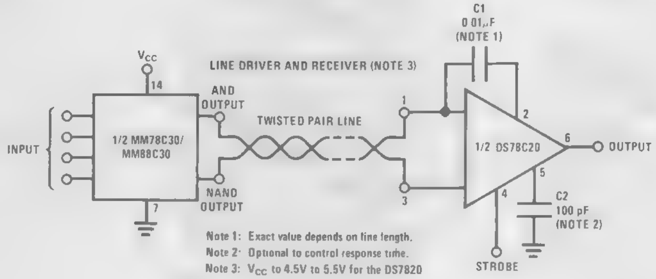


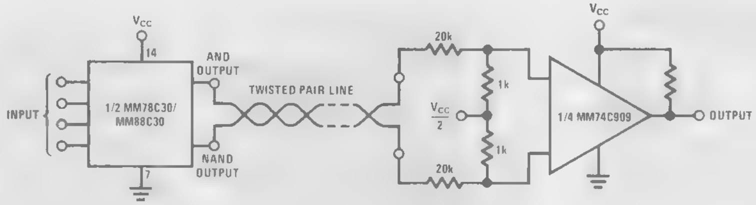
FIGURE 2.

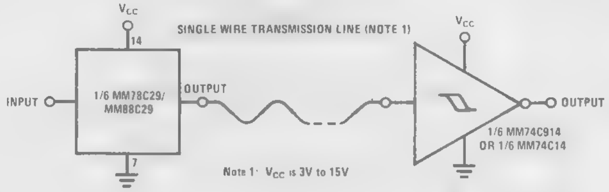
Typical Applications

Digital Data Transmission



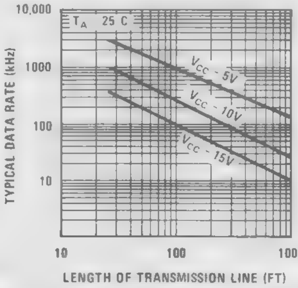
Note 1: Exact value depends on line length.
Note 2: Optional to control response time.
Note 3: V_{CC} to 4.5V to 5.5V for the DS7820





Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

Section 2

MM54C9XX/MM74C9XX Special Function/LSI Devices

National Semiconductor

MM54C901/MM74C901 Hex Inverting TTL Buffer
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer
MM54C903/MM74C903 Hex Inverting CMOS Buffer
MM54C904/MM74C904 Hex Non-Inverting CMOS Buffer

General Description

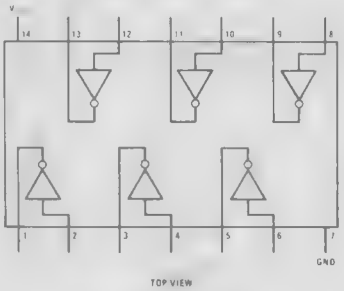
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply. For specific applications see MOS Brief 18 in the back of this catalog.

Features

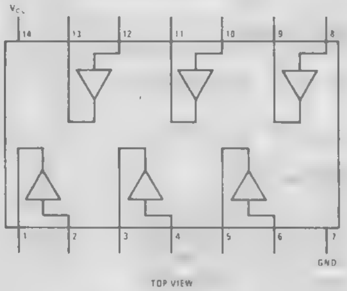
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	fan out of 2 driving standard TTL

Connection and Logic Diagrams

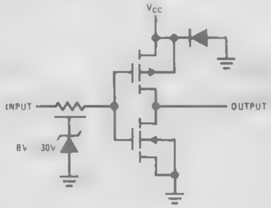
MM54C901/MM74C901
MM54C903/MM74C903



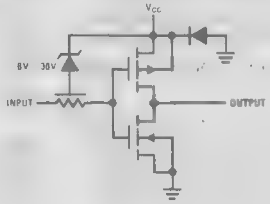
MM54C902/MM74C902
MM54C904/MM74C904



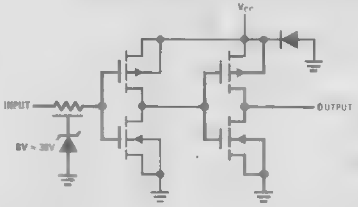
MM54C901/MM74C901
CMOS to TTL Inverting Buffer



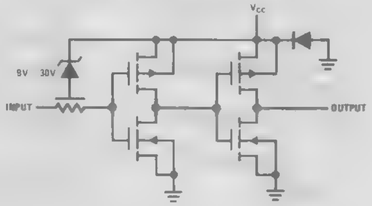
MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



MM54C902/MM74C902
CMOS to TTL Buffer



MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC} + 0.3\,V$
Voltage at any Input Pin	
MM54C901/MM74C901	$-0.3\,V$ to $+15\,V$
MM54C902/MM74C902	$-0.3\,V$ to $+15\,V$
MM54C903/MM74C903	$V_{CC} - 17\,V$ to $V_{CC} + 0.3\,V$
MM54C904/MM74C904	$V_{CC} - 17\,V$ to $V_{CC} + 0.3\,V$
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW

Operating Temperature Range	
MM54C901, MM54C902, MM54C903, MM54C904	−55°C to +125°C
MM74C901, MM74C902, MM74C903, MM74C904	−40°C to +85°C
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$	3.5			V
		$V_{CC} = 10\,V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$			1.5	V
		$V_{CC} = 10\,V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\,\mu A$	4.5			V
		$V_{CC} = 10\,V$, $I_O = -10\,\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$,			0.5	V
		$V_{CC} = 10\,V$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0	−0.005		µA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	15	µA
	TTL to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$	$V_{CC} - 1.5$			V
		74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$			0.8	V
		74C $V_{CC} = 4.75\,V$			0.8	V
	CMOS to TTL					
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5\,V$	4.0			V
	MM54C902, MM54C904	$V_{CC} = 4.5\,V$	$V_{CC} - 1.5$			V
	MM74C901, MM74C903	$V_{CC} = 4.75\,V$	4.25			V
	MM74C902, MM74C904	$V_{CC} = 4.75\,V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5\,V$			1.0	V
	MM54C902, MM54C904	$V_{CC} = 4.5\,V$			1.5	V
	MM74C901, MM74C903	$V_{CC} = 4.75\,V$			1.0	V
	MM74C902, MM74C904	$V_{CC} = 4.75\,V$			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -800\,\mu A$	2.4			V
		74C $V_{CC} = 4.75\,V$, $I_O = -800\,\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5\,V$, $I_O = 2.6\,mA$			0.4	V
	MM54C902, MM54C904	$V_{CC} = 4.5\,V$, $I_O = 3.2\,mA$			0.4	V
	MM74C901, MM74C903	$V_{CC} = 4.75\,V$, $I_O = 2.6\,mA$			0.4	V
	MM74C902, MM74C904	$V_{CC} = 4.75\,V$, $I_O = 3.2\,mA$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current) (MM54C901/MM74C901, MM54C903/MM74C903)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = 0\,V$ $T_A = 25°C$, $V_{IN} = 0\,V$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10\,V$, $V_{OUT} = 0\,V$ $T_A = 25°C$, $V_{IN} = 0\,V$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = V_{CC}$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = 0.4\,V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	3.8			mA

DC Electrical Characteristics (cont'd)

	Parameter	Conditions	Min.	Typ.	Max.	Units
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current) (MM54C902/MM74C902, MM54C902/MM74C902)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = 0V$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$ $T_A = 25°C$, $V_{IN} = 0V$	3.8			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	MM54C901/MM74C901, MM54C903/MM74C903					
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$		38	70	ns
		$V_{CC} = 10V$		22	30	ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$		21	35	ns
		$V_{CC} = 10V$		13	20	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		14		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF
	MM54C902/MM74C902, MM54C904/MM74C904					
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$		57	90	ns
		$V_{CC} = 10V$		27	40	ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$		54	90	ns
		$V_{CC} = 10V$		25	40	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		50		pF

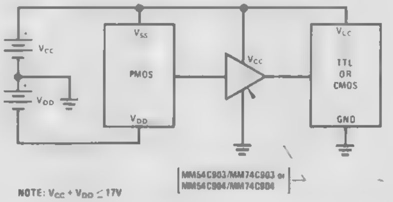
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

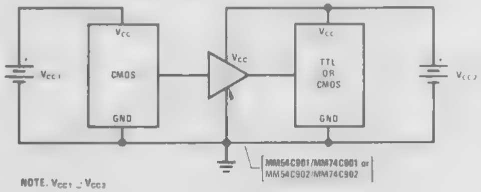
Typical Applications

PMOS to CMOS or TTL Interface



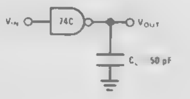
NOTE: $V_{CC} + V_{DD} \leq 17V$
$V_{CC} \leq 15V$

CMOS to TTL or CMOS at a Lower V_{CC}



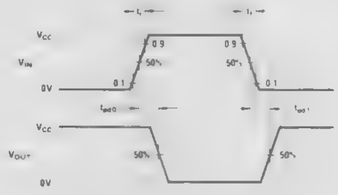
NOTE: $V_{CC1} \geq V_{CC2}$

AC Test Circuit and Switching Time Waveform



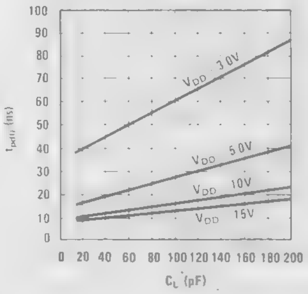
Note. Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS

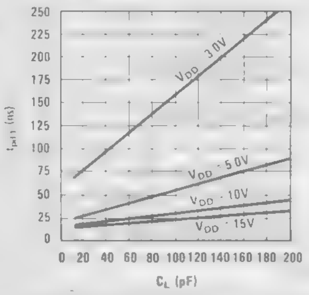


Typical Performance Characteristics

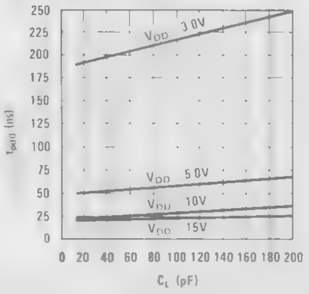
Typical Propagation Delay to a Logical "0" for the MM54C901/MM74C901 and MM54C903/MM74C903



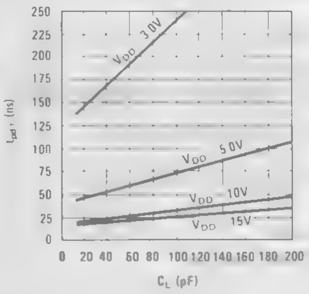
Typical Propagation Delay to a Logical "1" for the MM54C901/MM74C901 and MM54C903/MM74C903



Typical Propagation Delay to a Logical "0" for the MM54C902/MM74C902 and MM54C904/MM74C904



Typical Propagation Delay to a Logical "1" for the MM54C902/MM74C902 and MM54C904/MM74C904



National Semiconductor

MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

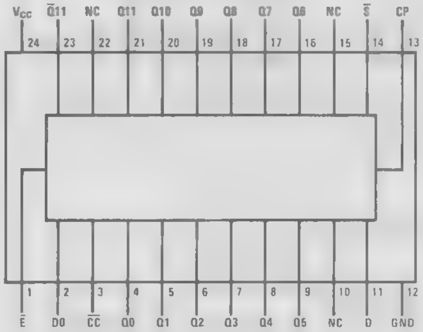
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



Truth Table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	CC
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\mu A$ $V_{CC} = 10V$, $I_O = -10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\mu A$ $V_{CC} = 10V$, $I_O = 10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C905	$V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
	MM74C905	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C905	$V_{CC} = 4.5V$			0.8	V
	MM74C905	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage					
	MM54C905	$V_{CC} = 4.5V$, $I_O = -360\mu A$	2.4			V
	MM74C905	$V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C905	$V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
	MM74C905	$V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$ $V_{CC} = 10V \pm 5\%$	8.0	16		mA
R_{SOURCE}	Q11–Q0 Outputs	$V_{OUT} = V_{CC} - 0.3V$ $T_A = 25°C$	150		350	Ω
R_{SINK}		$V_{CC} = 10V \pm 5\%$ $V_{OUT} = 0.3V$ $T_A = 25°C$	80		230	Ω

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50 pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time from Clock Input to Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
		$V_{CC} = 10V$		80	150	ns
t_{pd}	Propagation Delay Time from Clock Input to D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
		$V_{CC} = 10V$		70	125	ns
t_{pd}	Propagation Delay Time from Register Enable (E) to Output (Q11) ($t_{pd(E)}$)	$V_{CC} = 5.0V$		190	350	ns
		$V_{CC} = 10V$		75	150	ns
t_{pd}	Propagation Delay Time from Clock to CC ($t_{pd(CC)}$)	$V_{CC} = 5.0V$		190	350	ns
		$V_{CC} = 10V$		75	0.50	ns
t_S	Data Input Set-Up Time	$V_{CC} = 5.0V$	80			ns
		$V_{CC} = 10V$	30			ns
t_S	Start Input Set-Up Time	$V_{CC} = 5.0V$	80			ns
		$V_{CC} = 10V$	30			ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$	250	125		ns
		$V_{CC} = 10V$	100	50		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$			15	μs
		$V_{CC} = 10V$			5.0	μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2.0	4.0		MHz
		$V_{CC} = 10V$	5.0	10		MHz
C_{CK}	Clock Input Capacitance	Clock Input (Note 2)		10		pF
C_{IN}	Input Capacitance	Any other Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

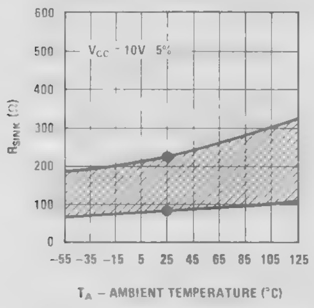
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

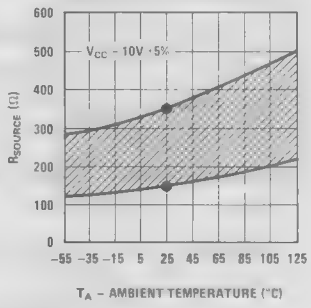
Typical Performance Characteristics

R_{SINK} vs Temperature



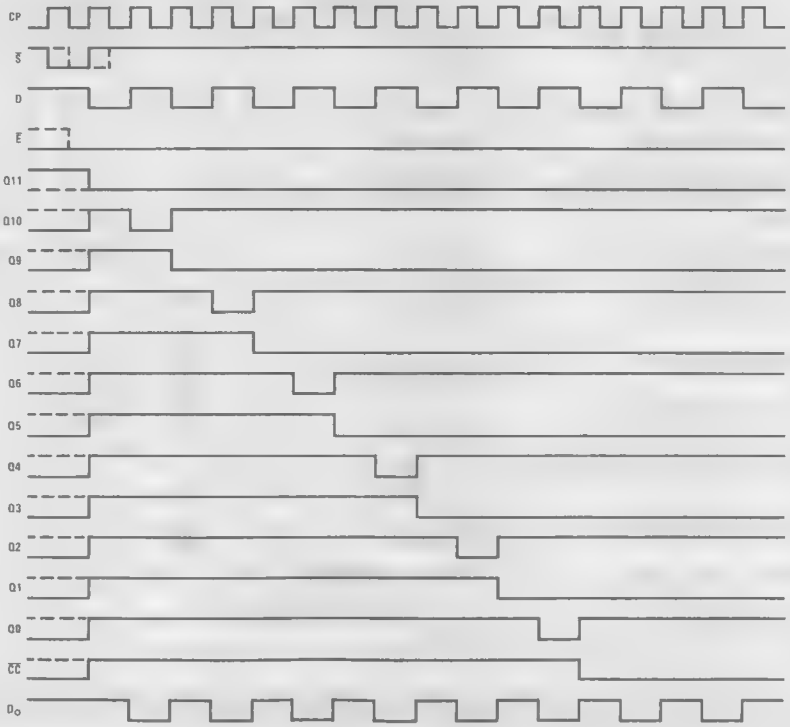
● These points are guaranteed by automatic testing.

R_{SOURCE} vs Temperature

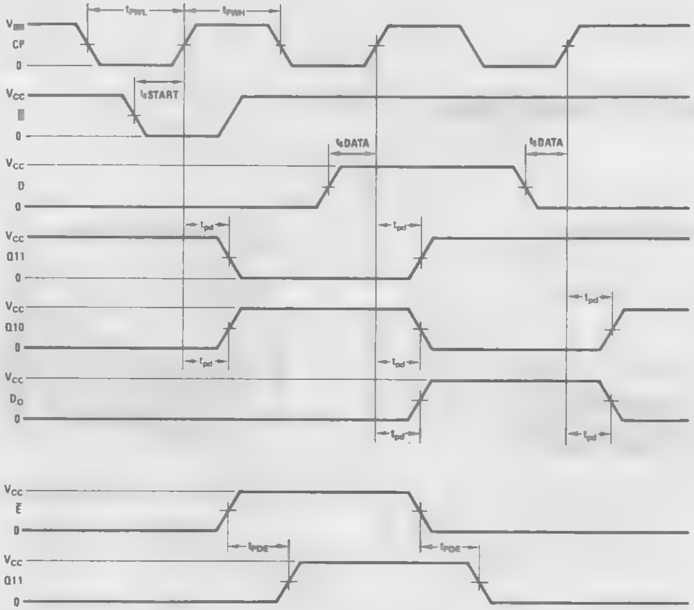


● These points are guaranteed by automatic testing.

Timing Diagram



Switching Time Waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

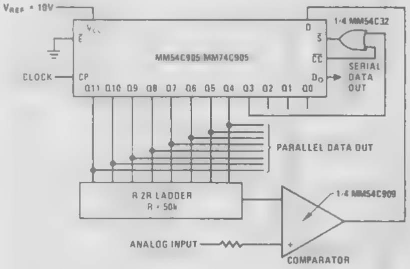
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

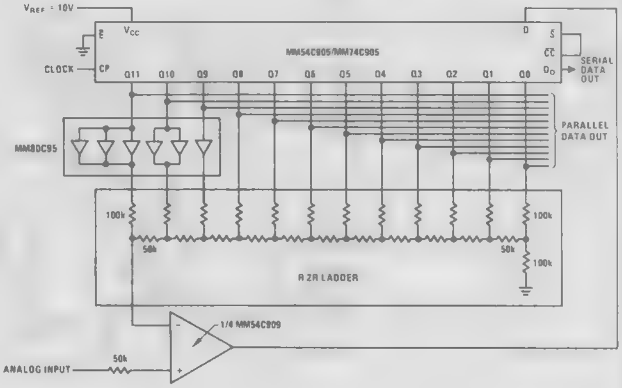
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



Definition of Terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q}11$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

National Semiconductor

MM54C906/MM74C906 Hex Open Drain N-Channel Buffers
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers

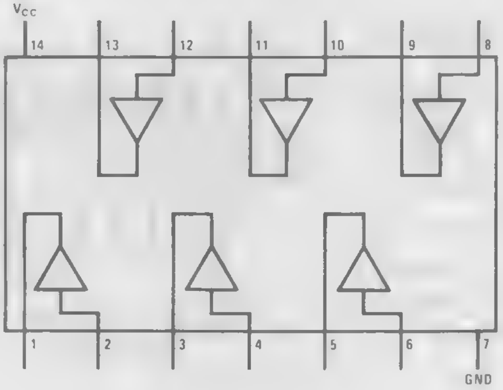
General Description

These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

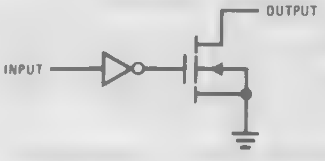
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ High current sourcing and sinking open drain outputs	

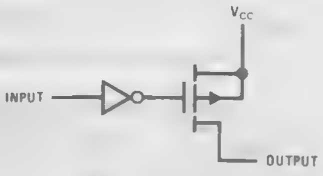
Connection Diagram



Logic Diagrams



MM54C906/MM74C906



MM54C907/MM74C907

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} + 0.3V
Voltage at any Output Pin	
MM54C906/MM74C906	−0.3V to +18V
MM54C907/MM74C907	V_{CC} − 18 to V_{CC} + 0.3V
Operating Temperature Range	
MM54C906/MM54C907	−55°C to +125°C
MM74C906/MM74C907	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V, Output Open		0.05	15	μA
	Output Leakage					
	MM54C906	V_{CC} = 4.5V, V_{IN} = V_{CC} − 1.5		0.005	5	μA
		V_{CC} = 4.5V, V_{OUT} = 18V				
	MM74C906	V_{CC} = 4.75V, V_{IN} = V_{CC} − 1.5		0.005	5	μA
		V_{CC} = 4.75V, V_{OUT} = 18V				
	MM54C907	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
		V_{CC} = 4.5V, V_{OUT} = V_{CC} − 18V				
	MM74C907	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
		V_{CC} = 4.75V, V_{OUT} = V_{CC} − 18V				
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
	Output Drive Current					
	MM54C906	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}				
		V_{CC} = 4.5V, V_{OUT} = 0.5V	2.1	8.0		mA
		V_{CC} = 4.5V, V_{OUT} = 1.0V	4.2	12		mA
	MM74C906	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}				
		V_{CC} = 4.75V, V_{OUT} = 0.5V	2.1	8.0		mA
		V_{CC} = 4.75V, V_{OUT} = 1.0V	4.2	12		mA
	MM74C907	V_{CC} = 4.5V, V_{IN} = V_{CC} − 1.5V				
		V_{CC} = 4.5V, V_{OUT} = V_{CC} − 0.5V	−1.05	−1.5		mA
		V_{CC} = 4.5V, V_{OUT} = V_{CC} − 1.0V	−2.1	−3.0		mA
	MM74C907	V_{CC} = 4.75V, V_{IN} = V_{CC} − 1.5V				
		V_{CC} = 4.75V, V_{OUT} = V_{CC} − 0.5V	−1.05	−1.5		mA
		V_{CC} = 4.75V, V_{OUT} = V_{CC} − 1.0V	−2.1	−3.0		mA
	MM54C906/MM74C906	V_{CC} = 10V, V_{IN} = 2.0V				
		V_{CC} = 10V, V_{OUT} = 0.5V	4.2	−20		mA
		V_{CC} = 10V, V_{OUT} = 1.0V	8.4	−30		mA
	MM54C907/MM74C907	V_{CC} = 10V, V_{IN} = 8.0V				
		V_{CC} = 10V, V_{OUT} = 9.5V	−2.1	−4.0		mA
		V_{CC} = 10V, V_{OUT} = 9.0V	−4.2	−8.0		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, $R = 10k$			150	ns
		$V_{CC} = 10V$, $R = 10k$			75	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$, (Note 4)			75 + 0.7 RC	ns
t_{pd}	Propagation Delay Time to a Logical "1"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$, (Note 4)			75 + 0.7 RC	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, $R = 10k$			150	ns
		$V_{CC} = 10V$, $R = 10k$			75	ns
C_{IN}	Input Capacity	(Note 2)		5.0		pF
C_{OUT}	Output Capacity	(Note 2)		20		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

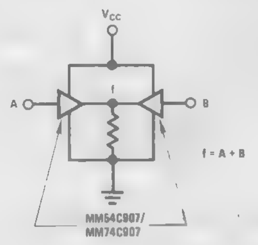
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes outputs are open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capactiy (C_{OUT}).

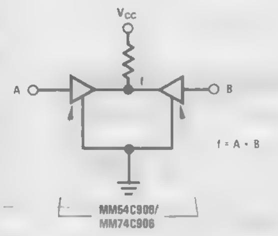
Typical Applications

Wire OR Gate



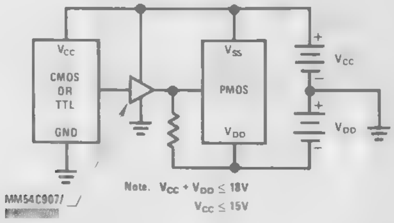
Note Can be extended to more than 2 inputs.

Wire AND Gate



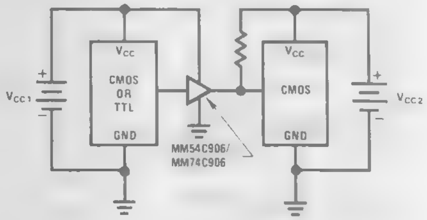
Note Can be extended to more than 2 inputs

CMOS or TTL to PMOS Interface



Note. $V_{CC} + V_{DD} \leq 18V$
$V_{CC} \leq 15V$

CMOS or TTL to CMOS at a Higher V_{CC}



National Semiconductor

MM74C908/MM74C918 Dual CMOS 30-Volt Relay Driver

General Description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_J = +65°C$.

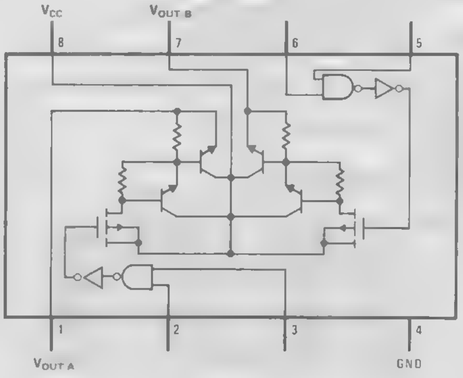
The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of −30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

Features

■ Wide supply voltage range	3V to 18V
■ High noise immunity	$0.45V_{CC}$ (typ.)
■ Low output "ON" resistance	8Ω (typ.)
■ High voltage	−30V
■ High current	250 mA

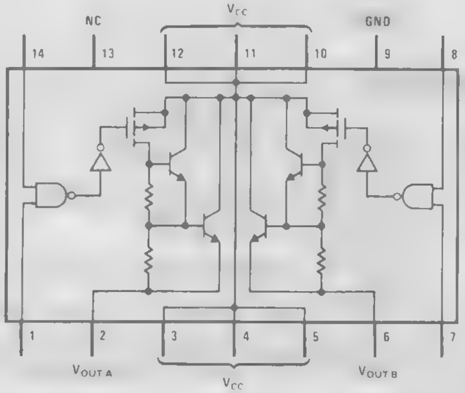
Connection Diagrams

MM74C908



TOP VIEW

MM74C918



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} + 0.3V
Voltage at Any Output Pin	32V
Operating Temperature Range MM74C908/MM74C918	−40°C to +85°C
Operating V_{CC} Range	3V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, Outputs Open Circuit		0.05	15	μA
	Output "OFF" Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -200\mu A$		−30		V
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage MM74C908/MM74C918	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage MM74C908/MM74C918	$V_{CC} = 4.75V$			0.8	V
	Output Drive					
V_{OUT}	Output Voltage	$I_{OUT} = -300 mA$, $V_{CC} \geq 5.0V$, $T_J = 25°C$	$V_{CC} - 2.7$	$V_{CC} - 1.8$		V
		$I_{OUT} = -250 mA$, $V_{CC} \geq 5.0V$, $T_J = 65°C$	$V_{CC} - 3.0$	$V_{CC} - 1.9$		V
		$I_{OUT} = -175 mA$, $V_{CC} \geq 5.0V$, $T_J = 150°C$	$V_{CC} - 3.15$	$V_{CC} - 2.0$		V
R_{ON}	Output Resistance	$I_{OUT} = -300 mA$, $V_{CC} \geq 5.0V$, $T_J = 25°C$		6.0	9.0	Ω
		$I_{OUT} = -250 mA$, $V_{CC} \geq 5.0V$, $T_J = 65°C$		7.5	12	Ω
		$I_{OUT} = -175 mA$, $V_{CC} \geq 5.0V$, $T_J = 150°C$		10	18	Ω
	Output Resistance Coefficient			0.55	0.80	%/°C
θ_{JA}	Thermal Resistance					
	MM74C908	(Note 3)		100	110	°C/W
	MM74C918	(Note 3)		45	55	°C/W

AC Electrical Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd1}	Propagation Delay to a Logic "1"	$V_{CC} = 5.0V$, $R_L = 50\Omega$, $C_L = 50 pF$, $T_A = 25°C$		150	300	ns
		$V_{CC} = 10V$, $R_L = 50\Omega$, $C_L = 50 pF$, $T_A = 25°C$		65	120	ns
t_{pd0}	Propagation Delay to a Logic "0"	$V_{CC} = 5.0V$, $R_L = 50\Omega$, $C_L = 50 pF$, $T_A = 25°C$		2.0	10	μs
		$V_{CC} = 10V$, $R_L = 50\Omega$, $C_L = 50 pF$, $T_A = 25°C$		4.0	20	μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF

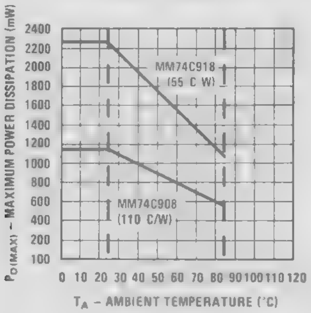
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

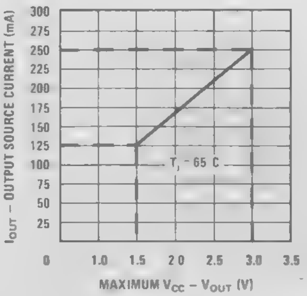
Note 3: θ_{JA} measured in free air with device soldered into printed circuit board.

Typical Performance Characteristics

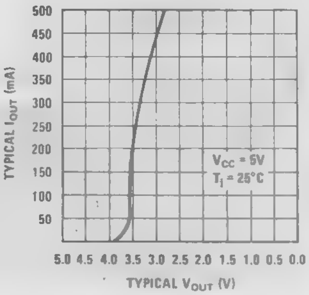
Maximum Power Dissipation vs Ambient Temperature



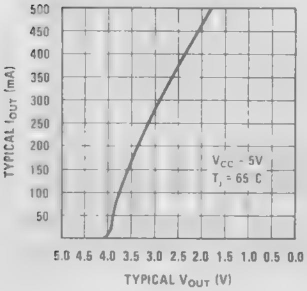
Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



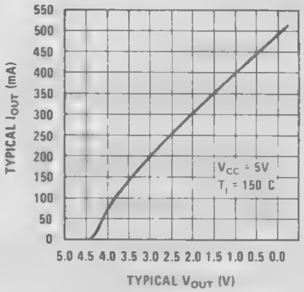
Typical I_{OUT} vs Typical V_{OUT}



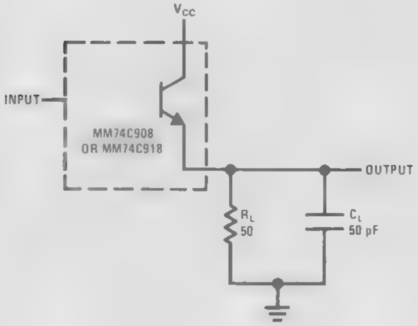
Typical I_{OUT} vs Typical V_{OUT}



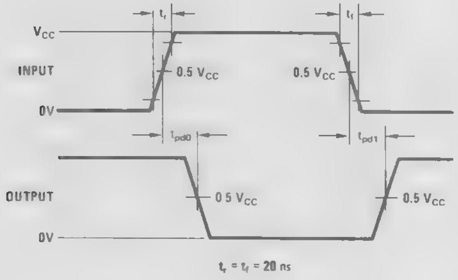
Typical I_{OUT} vs Typical V_{OUT}



AC Test Circuit



Switching Time Waveforms



Power Considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_j, and is given by:

$$R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 \tag{1}$$

and T_j is given by:

$$T_j = T_A + P_{DAV}\ \theta_{jA}, \tag{2}$$

where T_A = ambient temperature, θ_{jA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$$P_D = I_{OA}^2\ R_{ON} + I_{OB}^2\ R_{ON}, \tag{3}$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \tag{4}$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}^2\ R_{ON}\ (\text{Duty Cycle}_A) + I_{OB}^2\ R_{ON}\ (\text{Duty Cycle}_B) \tag{5}$$

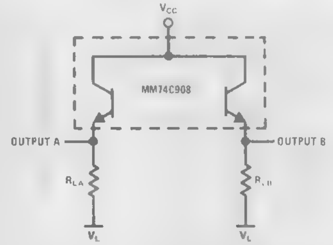
where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_j = T_A + \theta_{jA}\ [9\ (T_j - 25)\ (0.008) + 9]\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)] \tag{6a}$$

simplifying:

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]} \tag{6b}$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.



For example, let V_{CC} = 15V, R_{LA} = 100Ω, R_{LB} = 100Ω, V_L = 0V, T_A = 25°C, θ_{jA} = 110°C/W, Duty Cycle_A = 50%, Duty Cycle_B = 75%.
Assuming R_{ON} = 11Ω, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\text{ mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\text{ mA}$$

and

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}$$

$$T_j = \frac{25 + (7.2)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}{1 - (0.072)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}$$

$$T_j = 52.6^\circ\text{C}$$

and $R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 =$
$9\ (52.6 - 25)\ (0.008) + 9 = 11\Omega$

Applications

(See AN-177 for applications.)

National Semiconductor

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{\text{WE}}$, and a $\overline{\text{ME}}$ line. The six address lines are internally decoded to select one of 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{\text{ME}}$. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{\text{ME}}$, and (t_{HA}) after the positive to negative transition of $\overline{\text{ME}}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{\text{WE}}$ goes low while $\overline{\text{ME}}$ is low. $\overline{\text{WE}}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{\text{WE}}$ returns high.

Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{\text{WE}}$ held high.

TRI-STATE is a registered trademark of National Semiconductor Corp.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

Features

■ Supply voltage range	3.0V to 5.5V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatible fan out	1 TTL load
■ Input address register	
■ Low power consumption	250 nW/package (typ.) (chip enabled or disabled)
■ Fast access time	250 ns (typ.) at 5.0V
■ TRI-STATE outputs	
■ High voltage inputs	

See page 4-11 for Detailed Specifications

National Semiconductor

MM74C911 4-Digit Expandable Segment Display Controller

General Description

The MM74C911 display controller is an interface element with memory that drives a 4-digit, 8-segment LED display. The MM74C911 allows individual control of any segment in the 4-digit display. The number of segments per digit can be expanded without any external components. For example, two MM74C911's can be cascaded to drive a 16-segment alpha-numeric display.

The display controllers receive data information through 8 data lines a, b . . . DP, and digit information through 2 address inputs K1 and K2. The input data is written into the register selected by the address information when Chip Enable, $\overline{CE}$, and Write Enable, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required.

A self-contained internal oscillator sequentially presents the stored data to high drive (100 mA typ) TRI-STATABLE output drivers which directly drive the LED display. The drivers are active when the control pin labeled Segment Output Enable, $\overline{SOE}$, is low and go into TRI-STATE® when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control, or for disabling the output drive for power conservation.

The digit outputs directly drive the base of the digit transistor when the control pin labeled Digit Input Output, $\overline{DIO}$, is low. When $\overline{DIO}$ is high, the digit lines turn into inputs and the internal scanning multiplexer is disabled.

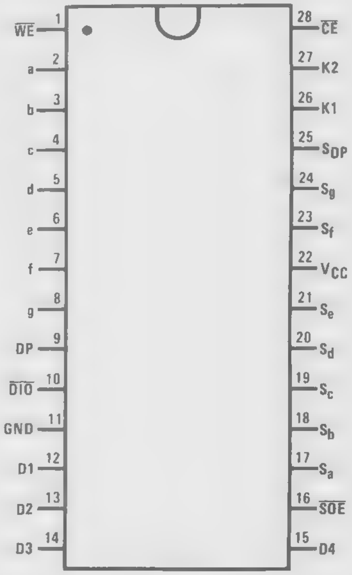
When any digit line is forced high by an external device, usually another MM74C911, the data information for that digit is presented to the output. In this manner, 16-segment alpha-numeric displays, 24 or 32-segment displays, or an array of discrete LED's can be controlled by the simple cascading of expandable segment display controllers. All inputs except digit inputs are TTL compatible and do not clamp input voltages above V_{CC}.

Features

- Direct segment drive (100 mA typ) TRI-STATABLE
- 4 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor
- Segment expandability without external components
- TTL compatible inputs
- Power saver mode—5 μW (typ.)

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Tables

Input Control

$\overline{CE}$	DIGIT ADDRESS		$\overline{WE}$	OPERATION
	K2	K1		
0	0	0	0	Write digit 1
0	0	0	1	Latch digit 1
0	0	1	0	Write digit 2
0	0	1	1	Latch digit 2
0	1	0	0	Write digit 3
0	1	0	1	Latch digit 3
0	1	1	0	Write digit 4
0	1	1	1	Latch digit 4
1	X	X	X	Disable writing

Output Control

$\overline{DIO}$	$\overline{SOE}$	DIGIT LINES				OPERATION
		D4	D3	D2	D1	
0	0	R	R	R	R	Refresh display
0	1	R	R	R	R	Disable segment outputs
1	0	0	0	0	0	Digits are now inputs
1	0	0	0	0	1	Display digit 1
1	0	0	0	1	0	Display digit 2
1	0	0	1	0	0	Display digit 3
1	0	1	0	0	0	Display digit 4
1	1	0	0	0	0	Power saver mode

R = Refresh (digit lines sequentially pulsed)
X = Don't care

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Any Input Except Digits	−0.3V to +15V
Operating Temperature Range, T_A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply at −40°C ≤ T_J ≤ +85°C, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current (Normal)	V_{CC} = 5V, Outputs Open		0.50	2.5	mA
I_{CC}	Supply Current (Power Saver)	V_{CC} = 5V, $\overline{SOE}$, $\overline{DIO}$ = "1", D1, D2, D3, D4 = "0"		1	600	μA
I_{OUT}	TRI-STATE Output Current	V_O = 5V		0.03	10	μA
		V_O = 0V	−10	−0.03		
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	V_{CC} = 5V, V_O = 3.4V				
		T_J = 25°C	−60	−100		mA
		T_J = 100°C	−40	60		mA
I_{DH}	High Level Digit Current	V_{CC} = 5V, V_O = 3V				
		T_J = 25°C	−10	−20		mA
		T_J = 100°C	−7	−10		mA
		V_{CC} = 5V, V_O = 1V				
		T_J = 25°C	15	−40		mA
		T_J = 100°C	−10	−15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage, Any Digit	V_{CC} = 5V, I_O = −360 μA	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage, Any Output	V_{CC} = 5V, I_O = 360 μA			0.4	V
θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltage reference to ground.

Note 3: θ_{JA} measured in free-air with device soldered into printed circuit board.

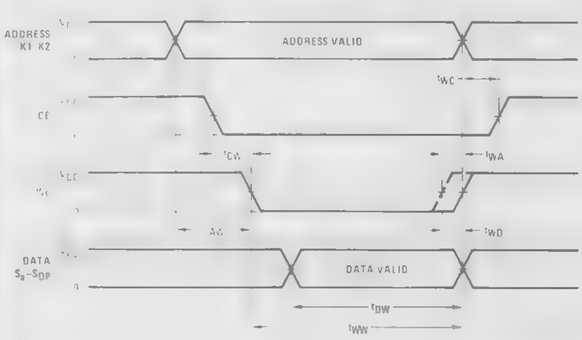
AC Electrical Characteristics $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable Set-Up Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{AW}	Address to Write Enable Set-Up Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{WW}	Write Enable Width	$T_J = 25°C$	400	225		ns
		$T_J = 125°C$	450	250		ns
t_{DW}	Data to Write Enable Set-Up Time	$T_J = 25°C$	390	225		ns
		$T_J = 125°C$	430	250		ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	$T_J = 25°C$	55	30		ns
		$T_J = 125°C$	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels into TRI-STATE	$R_L = 10k$, $C_L = 10$ pF				
		$T_J = 25°C$		275	500	ns
		$T_J = 125°C$		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" or Logical "0" Levels	$R_L = 10k$, $C_L = 50$ pF				
		$T_J = 25°C$		325	600	ns
		$T_J = 125°C$		375	700	ns
t_{D1}, t_{D0}	Propagation Delay From Digit Input to Segment Output	$T_J = 25°C$		500	1000	ns
		$T_J = 125°C$		700	1400	ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$	5	10		μs
		$T_J = 125°C$	10	20		μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$		525		Hz
		$T_J = 125°C$		375		Hz
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		30	50	pF

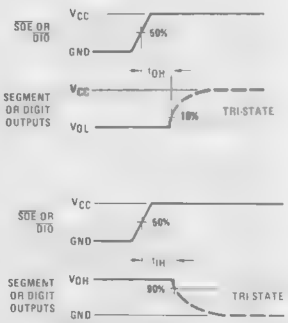
Note 4: Capacitance guaranteed by periodic testing.

Switching Time Waveforms

Write Data Waveforms

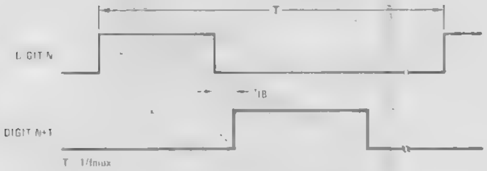


TRI-STATE Waveforms

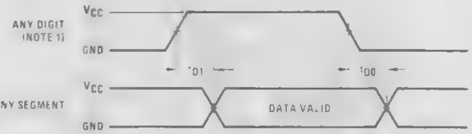


Switching Time Waveforms (Continued)

Multiplexing Output Waveforms



Read Data Waveforms



Note 1: All other digit lines are at a low level. $\overline{\text{DIO}}$ at a high level.

Functional Description

The MM74C911 display controller is manufactured on standard metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin to suppress current transients.

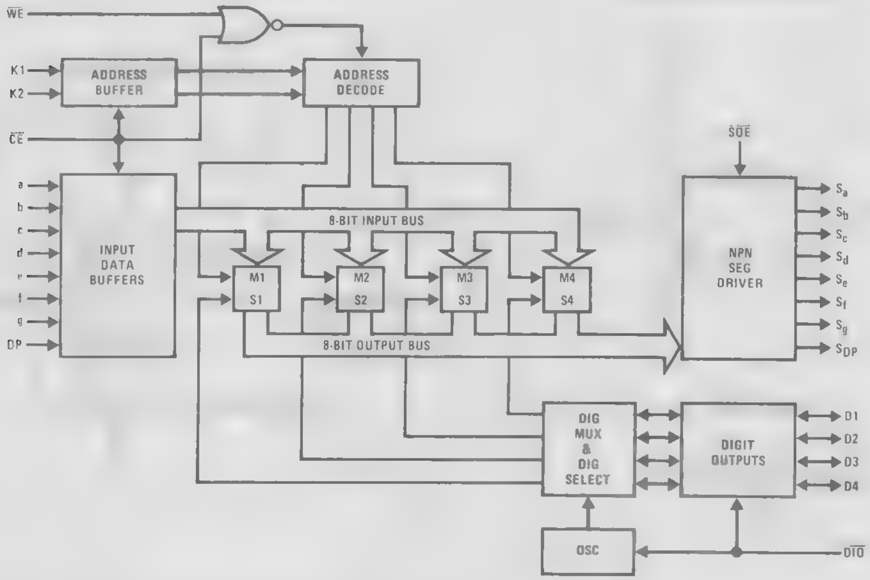
The digit outputs directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration. If an MM74C911 is driving a digit transistor and also supplying digit information to a cascaded MM74C911, base resistors are needed in the digit transistors to provide an adequate high level to the digit inputs of the cascaded MM74C911.

As seen in the block diagram, these display controllers contain four 8-bit registers; any one may be randomly written into. In normal operation, the internal multiplexer scans the registers and refreshes the display. In cascaded operation, 1 MM74C911 serves as a master refresh device and cascaded MM74C911's are slaved to it through digit lines operating as inputs.

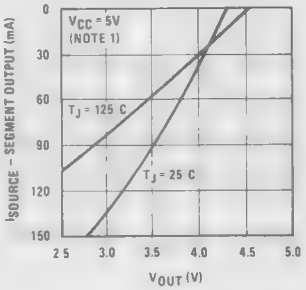
The MM74C911 appears to a microprocessor as memory and to the user as a self-scan display. Since every segment is under microprocessor control, great versatility is obtained.

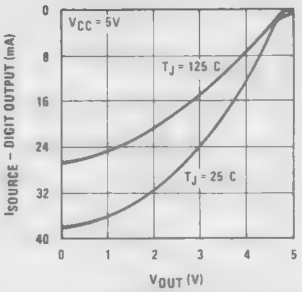
Low power standby operation occurs with both $\overline{\text{SOE}}$ and $\overline{\text{DIO}}$ inputs high. This condition forces the MM74C911 to a quiescent state typically drawing less than 1 μA of supply current with a standby supply voltage as low as 3V.

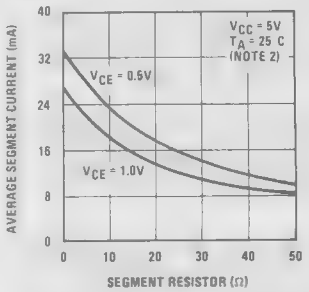
Block Diagram



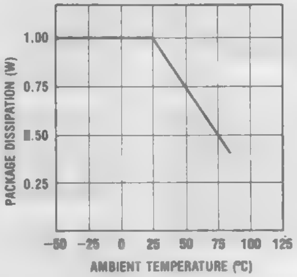
Typical Performance Characteristics



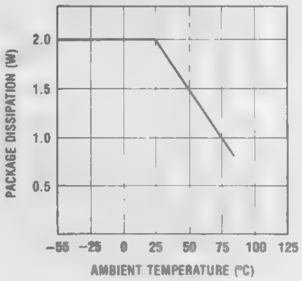




Power Dissipation vs. Temperature for Plastic Packages



Power Dissipation vs. Temperature for Ceramic Packages

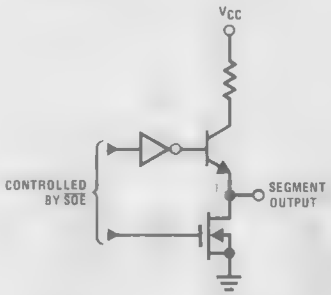


Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

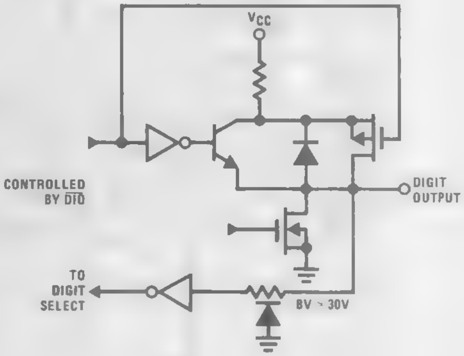
Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

Applications

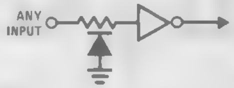
Segment Output Structure



Digit Output Structure

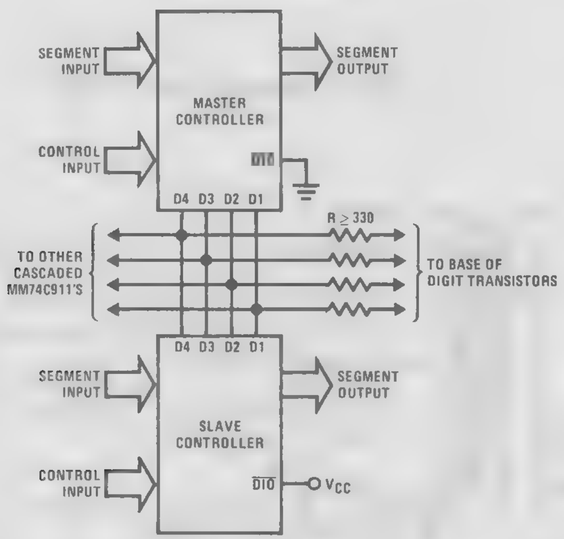


Input Protection

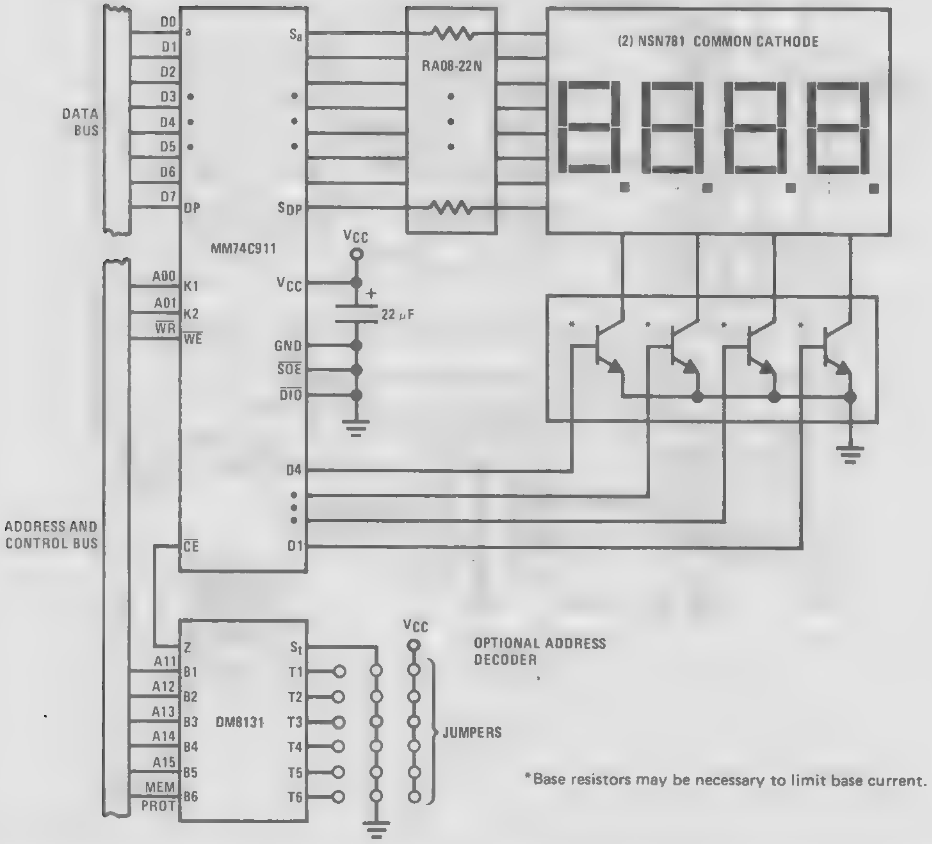


Applications (Continued)

Segment Expansion



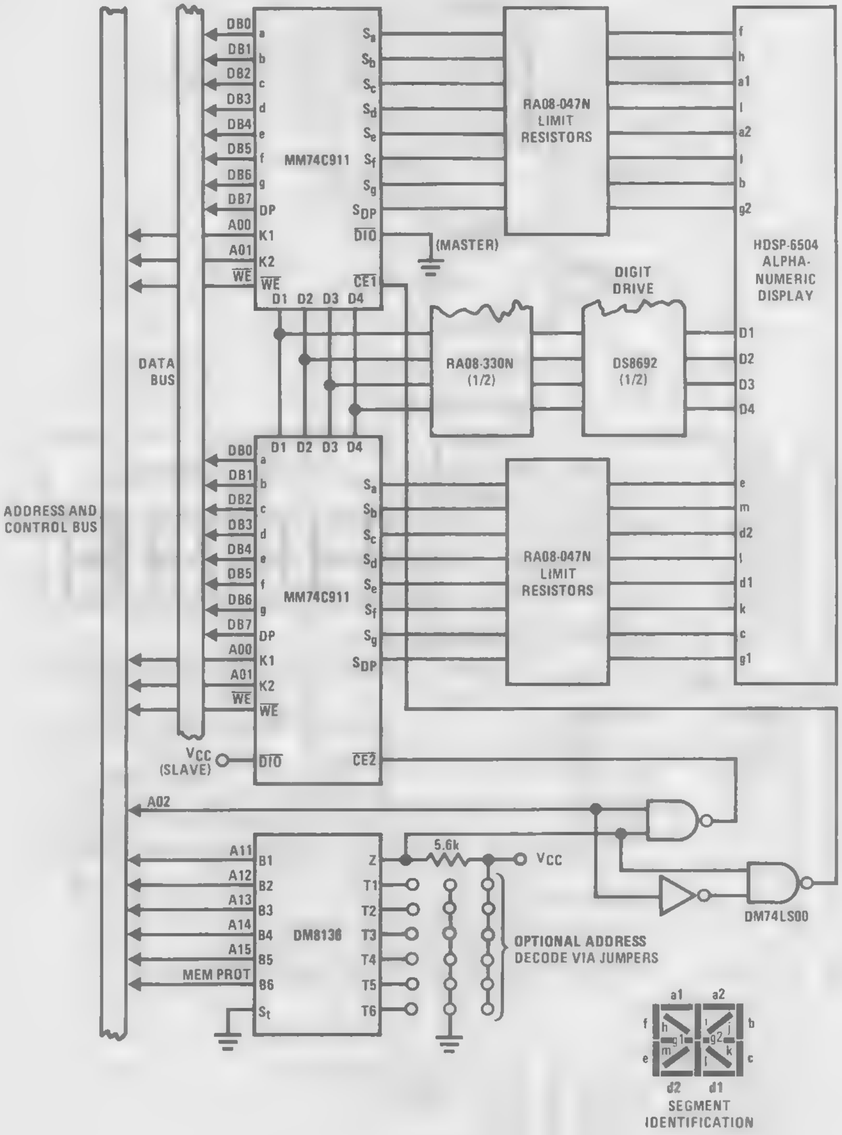
Typical Application



*Base resistors may be necessary to limit base current.

Applications (Continued)

4-Digit, 16-Segment Alpha-Numeric Display



National Semiconductor

MM74C912 6-Digit BCD Display Controller/Driver
MM74C917 6-Digit Hex Display Controller/Driver

General Description

The MM74C912, MM74C917 display controllers are interface elements, with memory, that drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when $\overline{\text{CHIP ENABLE}}$, $\overline{\text{CE}}$, and $\overline{\text{WRITE ENABLE}}$, $\overline{\text{WE}}$, are low and is latched when either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ return high. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled $\overline{\text{OSCILLATOR ENABLE}}$, $\overline{\text{OSE}}$, which is tied low in normal operation. A high level at $\overline{\text{OSE}}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives a LED display through high drive (100 mA typ) output drivers. The drivers are active when the control pin labeled $\overline{\text{SEGMENT OUTPUT ENABLE}}$, $\overline{\text{SOE}}$, is low and go into TRI-STATE® when $\overline{\text{SOE}}$ is high. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format. The MM74C917 converts binary data into hex format.

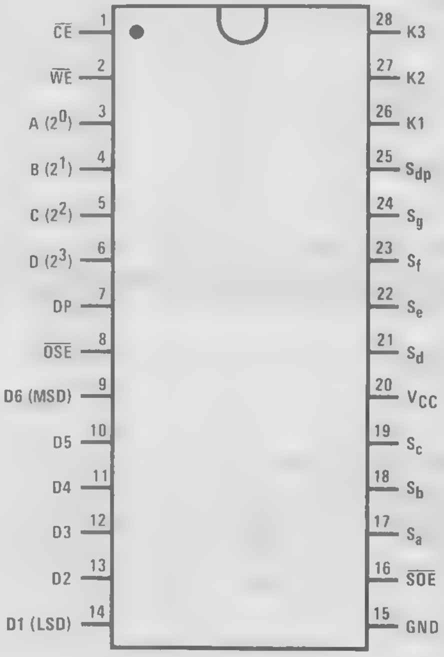
All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

- Direct segment drive (100 mA typ) TRI-STATEABLE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ)
- Internal segment decoder
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Tables

Input Control

$\overline{\text{CE}}$	DIGIT ADDRESS			$\overline{\text{WE}}$	OPERATION
	K3	K2	K1		
0	0	0	0	0	Write Digit 1
0	0	0	0	1	Latch Digit 1
0	0	0	1	0	Write Digit 2
0	0	0	1	1	Latch Digit 2
0	0	1	0	0	Write Digit 3
0	0	1	0	1	Latch Digit 3
0	0	1	1	0	Write Digit 4
0	0	1	1	1	Latch Digit 4
0	1	0	0	0	Write Digit 5
0	1	0	0	1	Latch Digit 5
0	1	0	1	0	Write Digit 6
0	1	0	1	1	Latch Digit 6
0	1	1	0	0	Write Null Digit
0	1	1	0	1	Latch Null Digit
0	1	1	1	0	Write Null Digit
0	1	1	1	1	Latch Null Digit
1	X	X	X	X	Disable Writing

X = don't care

Output Control

$\overline{\text{SOE}}$	$\overline{\text{OSE}}$	OPERATION
0	0	Refresh Display
0	1	Stop Oscillator*
1	0	Disable Segment Outputs
1	1	Standby Mode

*Segment drive may exceed maximum display dissipation.

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	Refer to $P_{D\,MAX}$ vs T_A Graph
Voltage at Any Input	$-0.3V$ to $+15V$	Operating V_{CC} Range	3V to 6V
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply at $40°C \leq T_J \leq 85°C$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5V$, Outputs Open		0.5	2	mA
I_{OUT}	TRI-STATE Output Current	$V_{CC} = 5V$, $V_O = 5V$		0.03	10	μA
		$V_{CC} = 5V$, $V_O = 0V$	−10	−0.03		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC}-2.0$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V$, $V_O = 3.4V$,				mA
		$T_J = 25°C$	−60	−100		
		$T_J = 100°C$	−40	−60		mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V$, $V_O = 1V$,				
		$T_J = 25°C$	−10	−20		mA
		$T_J = 100°C$	−7	−15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage Any Digit	$V_{CC} = 5V$, $I_O = -360\,\mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Output	$V_{CC} = 5V$, $I_O = 360\,\mu A$			0.4	V
Θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages reference to ground.

Note 3: Θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

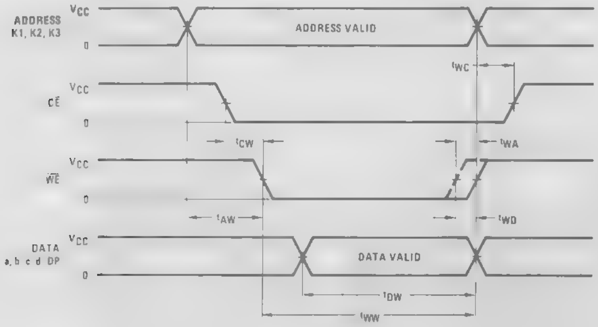
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable Setup Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{AW}	Address to Write Enable Setup Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{WW}	Write Enable Width	$T_J = 25°C$	400	225		ns
		$T_J = 125°C$	450	250		ns

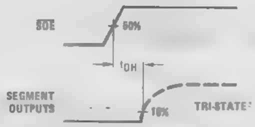
AC Electrical Characteristics (Continued) $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

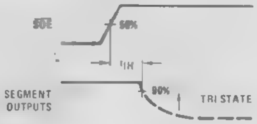
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DW}	Data to Write Enable Setup Time	$T_J = 25°C$	390	225		ns
		$T_J = 125°C$	430	250		ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	$T_J = 25°C$	0	-10		ns
		$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	$T_J = 25°C$	50	30		ns
		$T_J = 125°C$	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels Into TRI-STATE	$R_L = 10k$, $T_J = 25°C$		275	500	ns
		$C_L = 10$ pF, $T_J = 125°C$		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" to Logical "0" Level	$R_L = 10k$, $T_J = 25°C$		325	600	ns
		$C_L = 50$ pF, $T_J = 125°C$		375	700	ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$	5	10		μs
		$T_J = 125°C$	10	20		μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$		350		Hz
		$T_J = 125°C$		250		Hz
C_{IN}	Input Capacitance	Note 4		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Note 4		30	50	pF

Note 4: Capacitance is guranteed by periodic testing.

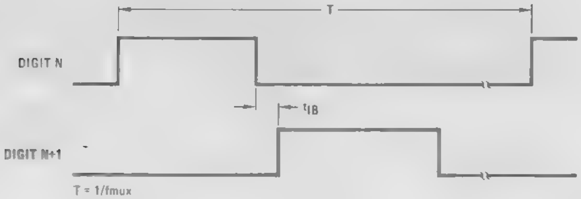
Switching Time Waveforms







Multiplexing Output Waveforms

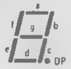


Functional Description

Character Font

MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	F.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	o	°	‾	-	_		.
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Segment Identification

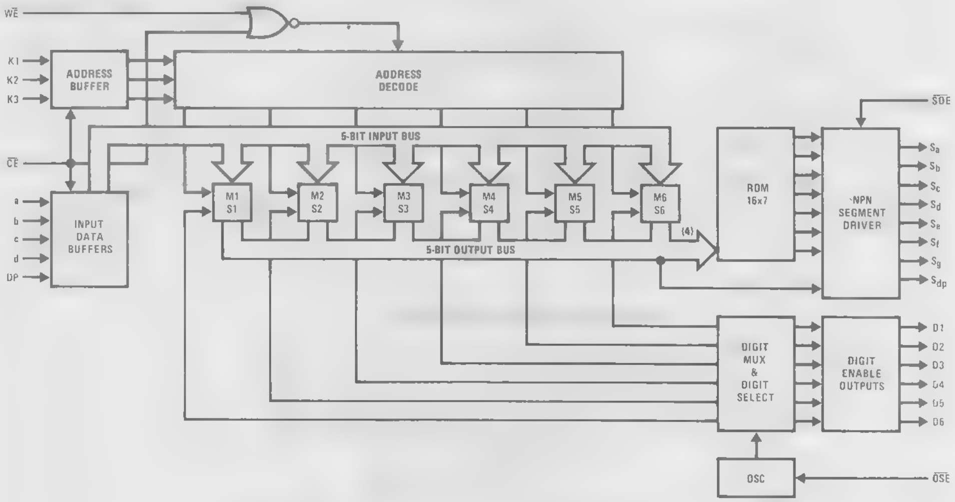


The MM74C912, MM74C917 display controllers are manufactured using metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin.

All inputs are TTL compatible; the segment outputs drive the LED display directly through current limiting resistors. The digit outputs are designed to directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration.

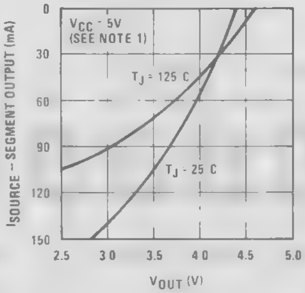
As seen in the block diagram, these display controllers contain six 5-bit registers; any one of which may be randomly written. The internal multiplexer scans the registers and refreshes the display. This combination of write only memory and self-scan display makes the display controller a "refreshing experience" for an overburdened microprocessor.

Block Diagram

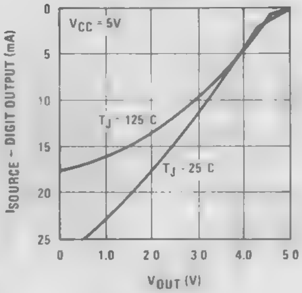


Typical Performance Characteristics

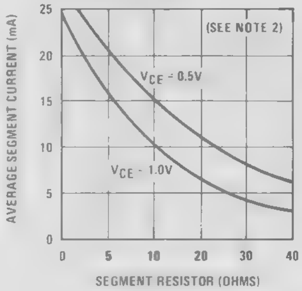
I_{SH} vs V_{OUT}



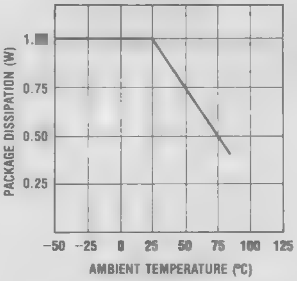
I_{DH} vs V_{OUT}



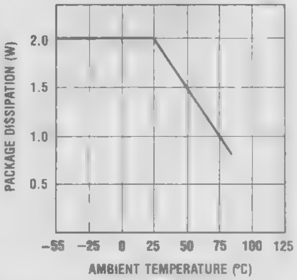
I_{AVG} vs R_{LIM}



Power Dissipation vs. Temperature for Plastic Packages



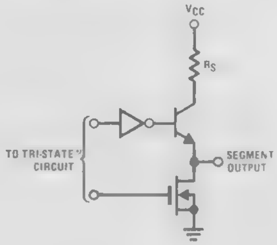
Power Dissipation vs. Temperature for Ceramic Packages



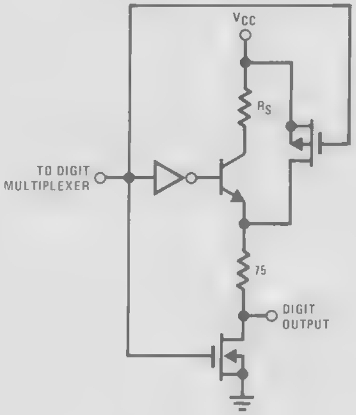
Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

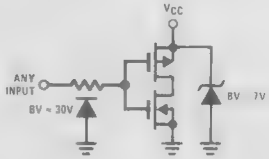
Segment Output Structure



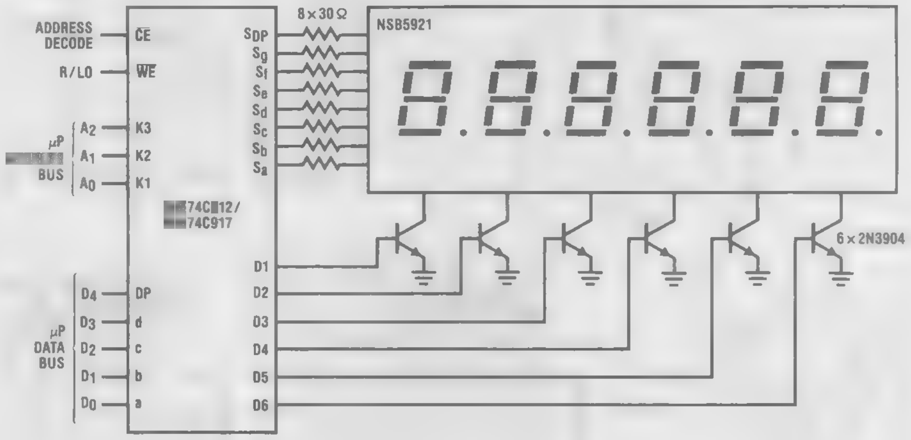
Digit Output Structure



Input Protection



Typical Applications



National Semiconductor

MM54C914/MM74C914 Hex Schmitt Trigger with Extended Input Voltage

General Description

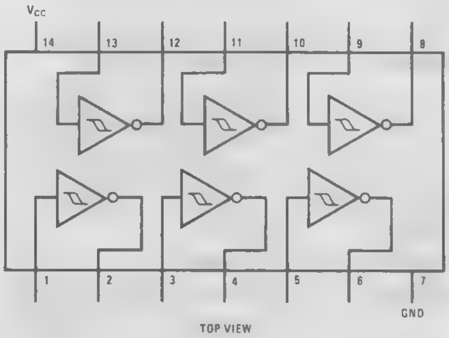
The MM54C914/MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 10V (V_{CC} − 25V to GND + 25V), and is valuable for applications involving voltage level shifting or mismatched power supplies.

The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005 V/°C at V_{CC} = 10V). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

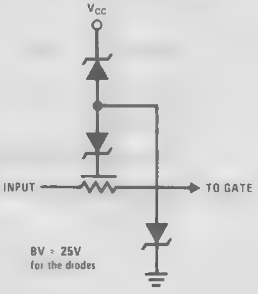
Features

■ Hysteresis	0.45 V_{CC} (typ.) 0.2 V_{CC} guaranteed
■ Special input protection	Extended Input Voltage Range
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram



Special Input Protection



Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{CC}-25V$ to $GND+25V$
Voltage at Any Other Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C914	−55°C to +125°C
MM74C914	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
V_{T+}	Positive Going Threshold Voltage	$V_{CC}=5.0V$	3.0	3.6	4.3	V
		$V_{CC}=10V$	6.0	6.8	8.6	V
		$V_{CC}=15V$	9.0	10	12.9	
V_{T-}	Negative Going Threshold Voltage	$V_{CC}=5.0V$	0.7	1.4	2.0	V
		$V_{CC}=10V$	1.4	3.2	4.0	V
		$V_{CC}=15V$	2.1	5.0	6.0	
$V_{T+}-V_{T-}$	Hysteresis	$V_{CC}=5.0V$	1.0	2.2	3.6	V
		$V_{CC}=10V$	2.0	3.6	7.2	V
		$V_{CC}=15V$	3.0	5.0	10.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=25V$		0.005	5.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=-10V$	−100	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, $V_{IN}=-10V/25V$		0.05	300	μA
		$V_{CC}=5.0V$, $V_{IN}=-2.5V$ (Note 4)		20		μA
		$V_{CC}=10V$, $V_{IN}=5.0V$ (Note 4)		200		μA
		$V_{CC}=15V$, $V_{IN}=7.5V$ (Note 4)		600		μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$, $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50 pF$, unless otherwise specified.

	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{pd}	Propagation Delay from Input to Output	$V_{CC} = 5.0V$		220	400	ns
		$V_{CC} = 10V$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

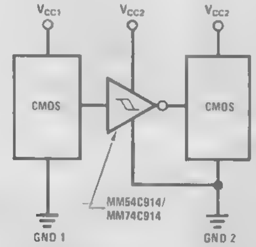
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: Only one input is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

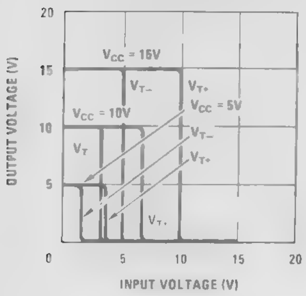
Typical Application



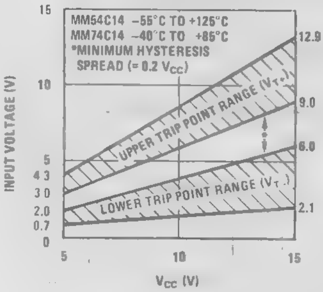
Note. $V_{CC1} > V_{CC2}$
GND 1 ≈ GND 2

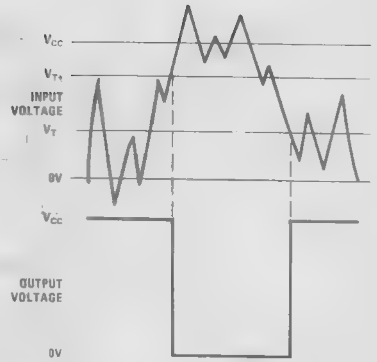
Typical Performance Characteristics

Typical Transfer Characteristics



Guaranteed Trip Point Range





National Semiconductor

MM54C915/MM74C915 7-Segment-to-BCD Converter

General Description

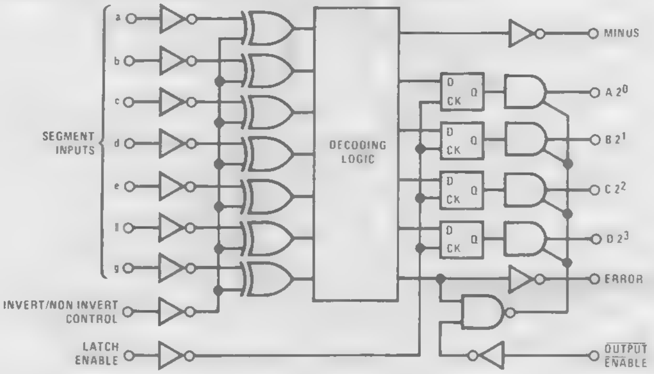
The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the Invert/Non-invert control pin. A logical "0" on the Invert/Non-invert control pin selects active high true decoding at the Segment inputs. A logical "1" on the Invert/Non-invert control pin selects active low true decoding at the Segment inputs. In addition to 4 TTL compatible BCD outputs, an Error output and Minus output are available. The Error output goes to an active "1" whenever a non-standard 7-segment code appears at the Segment inputs. The BCD outputs are forced into a TRI-STATE® condition when an error is detected. This allows the user to program his own error code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ 500k). The BCD outputs may also be forced into TRI-STATE by a logical "1" on output enable ($\overline{OE}$).

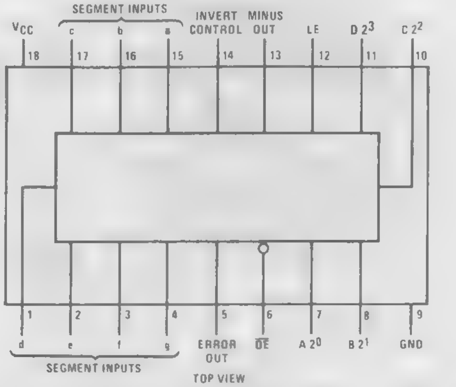
The Minus output goes to a logical "1" whenever a minus code is detected and is useful as a microprocessor interrupt. The BCD outputs are in a flow-though condition when Latch Enable (LE) is at a logical "0", and latched when LE is at a logical "1". The inputs will not clamp signals to the positive supply, allowing simple level translation from MOS to TTL.

Features

Wide supply range	3V–15V
High noise immunity	0.45 V_{CC} (typ.)
TTL compatible fan out	1 TTL load
Selectable active true inputs	
TRI-STATE outputs	
On-chip latch	
Error output	
Minus output	

Logic and Connection Diagrams





TOP VIEW

MM54C915	−55°C to +125°C	Maximum V_{CC}	18V
MM74C915	−40°C to +85°C	Lead Temperature, (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.3	4.5		V
		$V_{CC} = 10V$	8	9		V
		$V_{CC} = 15V$	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$		0.5	1.5	V
		$V_{CC} = 10V$		1	2	V
		$V_{CC} = 15V$		1.5	2.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 15V$		0.005	1	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−1	−0.005		µA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = 10\,\mu A$				
		$V_{CC} = 5V$		4.5		V
		$V_{CC} = 10V$		9		V
		$V_{CC} = 15V$		13.5		V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 10\,\mu A$				
		$V_{CC} = 5V$		0.5		V
		$V_{CC} = 10V$		1		V
		$V_{CC} = 15V$		1.5		V
I_{CC}	Supply Current	$V_{CC} = 5V$		0.25	1	mA
		$V_{CC} = 10V$		0.75	2.5	mA
		$V_{CC} = 15V$		1.00	3	mA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C915	$V_{CC} = 4.5V$	$V_{CC}-1.7$			V
	MM74C915	$V_{CC} = 4.75V$	$V_{CC}-1.7$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C915	$V_{CC} = 4.5V$			0.8	V
	MM74C915	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\,\mu A$				
	MM54C915	$V_{CC} = 4.5V$	2.4			V
	MM74C915	$V_{CC} = 4.75V$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6\,mA$				
	MM54C915	$V_{CC} = 4.5V$			0.4	V
	MM74C915	$V_{CC} = 4.75V$			0.4	V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current P-Channel	$T_A = 25°C$, $V_O = 0V$, (Note 2)				
		$V_{CC} = 5V$	−1.75	−3.3		mA
		$V_{CC} = 10V$	−8	−15		mA
		$V_{CC} = 15V$	−15	−25		mA
I_{SINK}	Output Sink Current N-Channel	$T_A = 25°C$, $V_O = V_{CC}$ (Note 2)				
		$V_{CC} = 5V$	5	8		mA
		$V_{CC} = 10V$	20	30		mA
		$V_{CC} = 15V$	30	50		mA

AC Electrical Characteristics $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or a Logical "1"	C_L = 50 pF				
		V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_{0H}, t_{1H}	Propagation Delay Time From Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10 pF				
		V_{CC} = 5V		110	200	ns
		V_{CC} = 10V		75	130	ns
		V_{CC} = 15V		60	110	ns
t_{H0}, t_{H1}	Propagation Delay Time From High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF				
		V_{CC} = 5V		150	250	ns
		V_{CC} = 10V		80	140	ns
		V_{CC} 15V		70	125	ns
t_s	Input Data Set-Up Time	C_L = 50 pF				
		V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_H	Input Data Hold Time	C_L = 50 pF				
		V_{CC} = 5V		150	0	ns
		V_{CC} = 10V		-100	0	ns
		V_{CC} = 15V		-100	0	ns
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 3)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

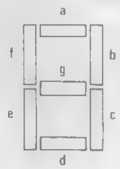
Note 3: Capacitance is guaranteed by periodic testing.

Truth Table

CHARACTER AT SEGMENT INPUTS	BCD OUTPUTS				NON-BCD OUTPUTS	
	D 2^3	C 2^2	B 2^1	A 2^0	ERROR	MINUS
0	0	0	0	0	0	0
1	0	0	0	1	0	0
1	0	0	0	1	0	0
2	0	0	1	0	0	0
3	0	0	1	1	0	0
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	0	0
9	1	0	0	1	0	0
	1	1	1	1	0	0
	X	X	X	X	1	1
All other input	X	X	X	X	1	0
combinations	X	X	X	X	1	0

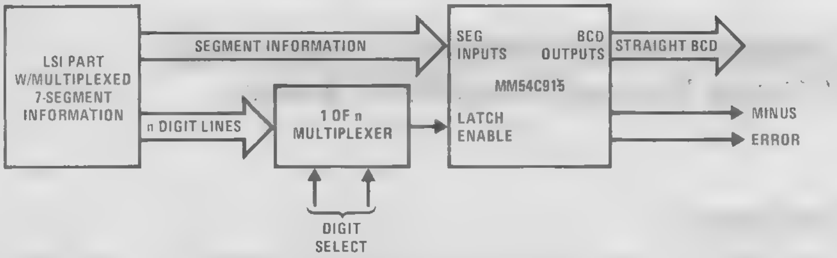
X = represents TRI-STATE condition

SEGMENT IDENTIFICATION

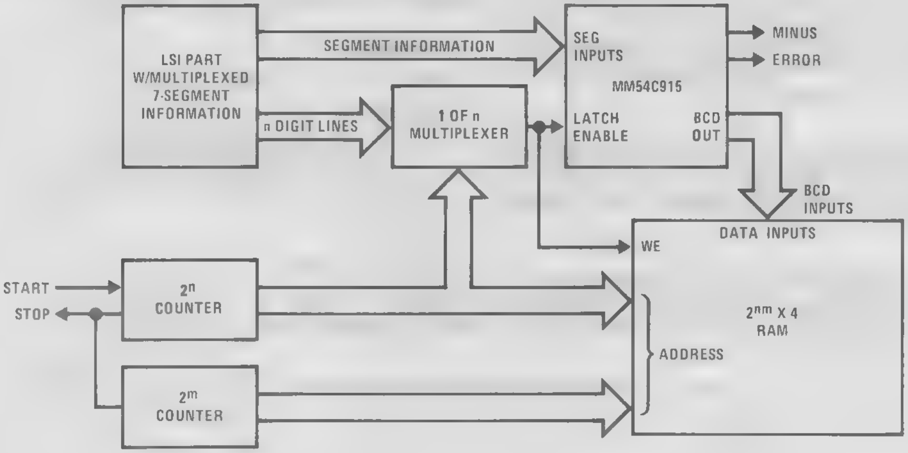


Typical Applications

Multiplex 7-Segment to Straight BCD



Memory Expansion from 7-Segment Outputs



National Semiconductor

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C920/MM74C920 256 × 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, CES and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads is thereby reduced to 18.

Complete address decoding as well as 2-chip select functions, CEL and CES, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer, as well as main frame memory applications.

Features

- 256 × 4-bit organization
- Access time
  - 250 ns max. MM74C920, MM74C921
  - 275 ns max. MM54C920, MM54C921
  - 300 ns max. MM74C920-3, MM74C921-3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5 V supply
- Data retained with V_{CC} as low as 2 V

See page 4-15
for detailed
specifications

National Semiconductor

MM54C922/MM74C922 16-Key Encoder MM54C923/MM74C923 20-Key Encoder

General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two key roll over is provided between any two switches.

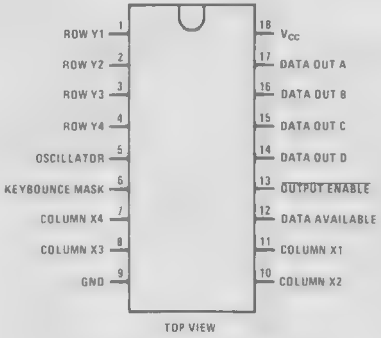
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outputs LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

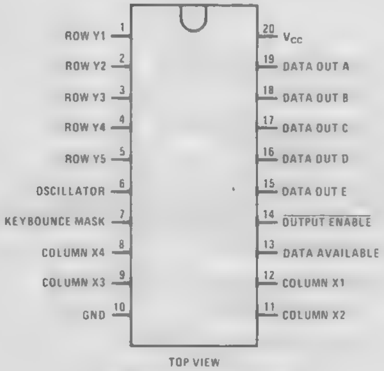
Connection Diagrams

Dual-In-Line Package



Order Number MM54C922N or MM74C922N See Package 20

Dual-In-Line Package



Order Number MM54C923N or MM74C923N See Package 20A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	V_{CC} – 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C922, MM54C923	–55°C to +125°C
MM74C922, MM74C923	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	3	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	6	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	9	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	0.7	1.4	2	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	1.4	3.2	4	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	2.1	5	6	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,	3.5	4.5		V
		V_{CC} = 10V,	8	9		V
		V_{CC} = 15V,	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,		0.5	1.5	V
		V_{CC} = 10V,		1	2	V
		V_{CC} = 15V,		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		–2	–5	µA
		V_{CC} = 10V		–10	–20	µA
		V_{CC} = 15V		–22	–45	µA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = –10µA	4.5			V
		V_{CC} = 10V, I_O = –10µA	9			V
		V_{CC} = 15V, I_O = –10µA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10µA			0.5	V
		V_{CC} = 10V, I_O = 10µA			1	V
		V_{CC} = 15V, I_O = 10µA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current	V_{CC} = 5V, Osc at 0V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005		µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V	V_{CC}–1.5			V
		74C, V_{CC} = 4.75V	V_{CC}–1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = –360µA	2.4			V
		74C, V_{CC} = 4.75V, I_O = –360µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = –360µA			0.4	V
		74C, V_{CC} = 4.75V, I_O = –360µA			0.4	V

DC Electrical Characteristics (Cont'd.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

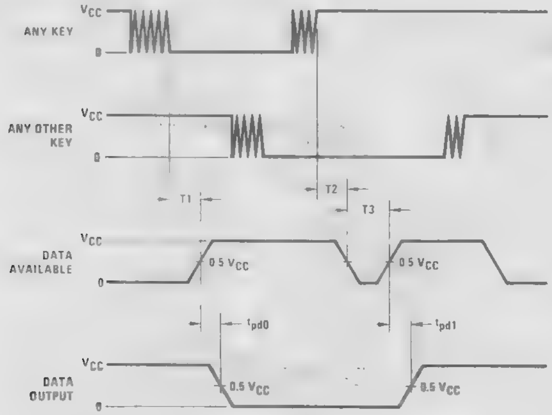
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF, *(Figure 1)*				
		V_{CC} = 5V		60	150	ns
		V_{CC} = 10V		35	80	ns
		V_{CC} = 15V		25	60	ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10pF *(Figure 2)*				
		V_{CC} = 5V R_L = 10k		80	200	ns
		V_{CC} = 10V C_L = 10 pF		65	150	ns
		V_{CC} = 15V		50	110	ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF, *(Figure 2)*				
		V_{CC} = 5V R_L = 10k		100	250	ns
		V_{CC} = 10V C_L = 50 pF		55	125	ns
		V_{CC} = 15V		40	90	ns
C_{IN}	Input Capacitance	Any Input, (Note 2)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 2)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC where R ≈ 10k and C is external capacitor at KBM input.

FIGURE 1

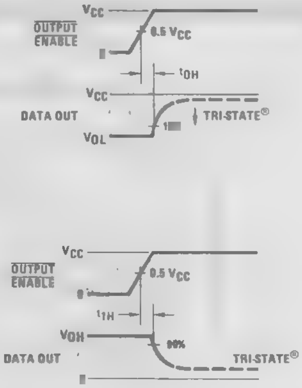
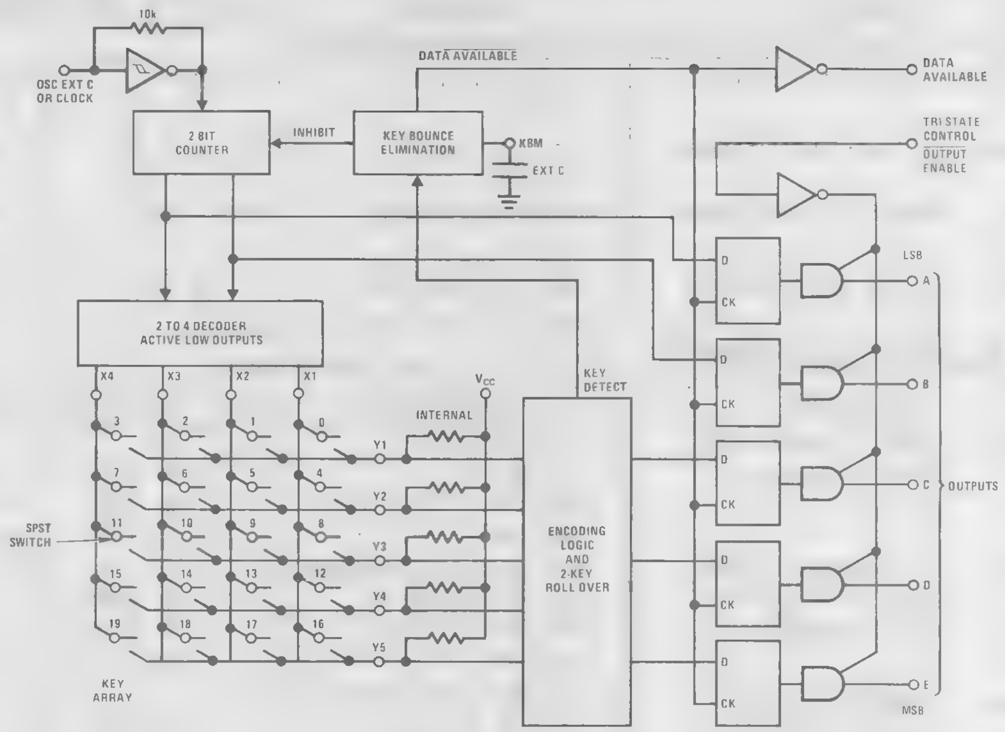


FIGURE 2

Block Diagram



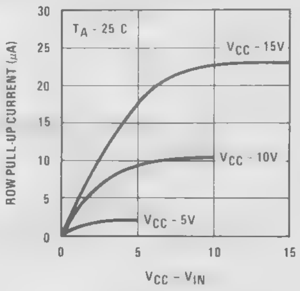
Truth Table

SWITCH POSITION	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA OUT A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

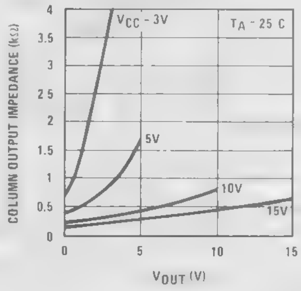
*Omit for MM54C922/MM74C922

Typical Performance Characteristics

Typical I_{rp} vs V_{IN} at Any Y Input

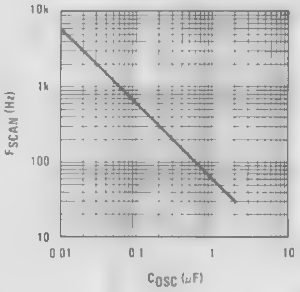


Typical R_{on} vs V_{OUT} at Any X Output

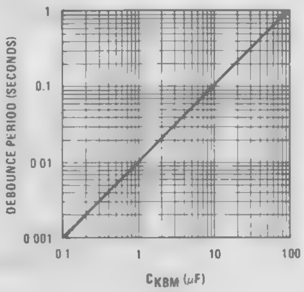


Typical Performance Characteristics (Cont'd.)

Typical F_{SCAN} vs C_{OSC}

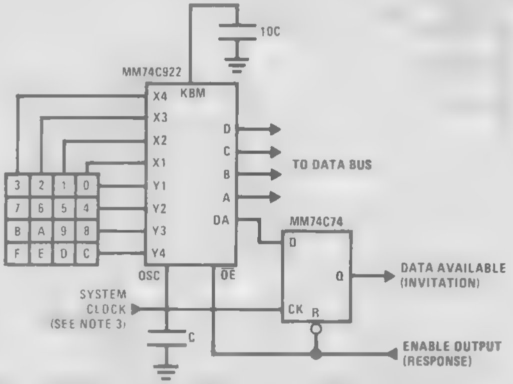


Typical Debounce Period vs C_{KBM}

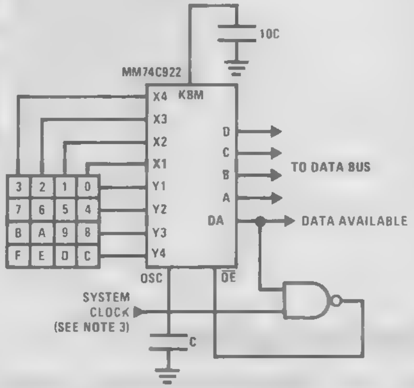


Typical Applications

Synchronous Handshake (MM74C922)



Synchronous Data Entry Onto Bus (MM74C922)



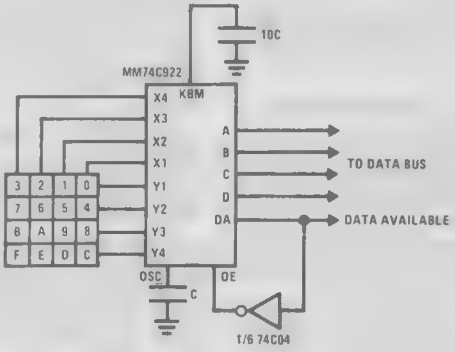
Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Asynchronous Data Entry Onto Bus (MM74C922)

Keyboard Suppliers

Mini Key Series KL
Digitran Company
Pasadena, California

Computronics Engineering
7235 Hollywood Blvd
Hollywood, California 90046

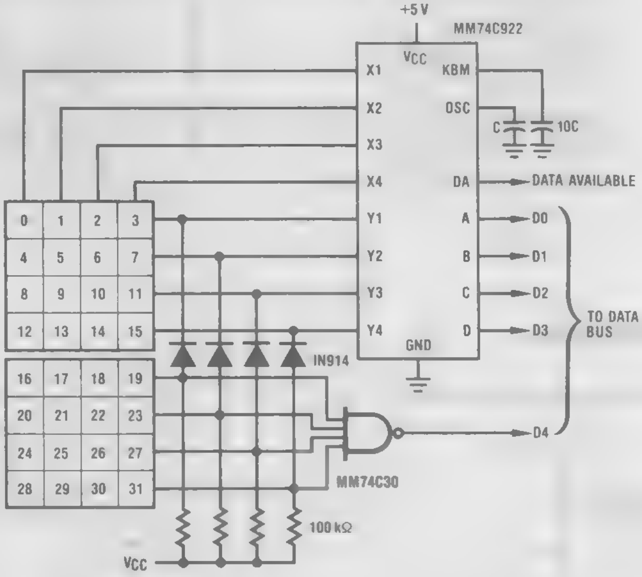


Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Typical Application (Cont'd.)

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM47C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2-4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be outputted is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two key roll over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE®, which are enabled when the Output Enable ($\overline{OE}$) input is taken low.

National Semiconductor

MM74C925, MM74C926, MM74C927, MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

General Description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

Features

Wide supply voltage range	3V to 6V
Guaranteed noise margin	1V
High noise immunity	$0.45\ V_{CC}$ (typ.)
High segment sourcing current	40 mA @ $V_{CC} - 1.6V$, $V_{CC} = 5V$
Internal multiplexing circuitry	

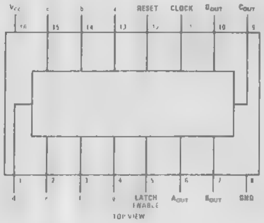
Design Considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DS75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

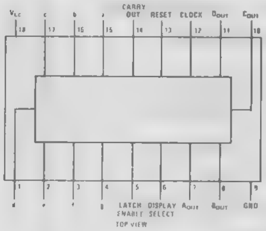
The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

Connection Diagram

Dual-In-Line Package
MM74C925



Dual-In-Line Package
MM74C926, MM74C927 and MM74C928



Functional Description

Reset	— Asynchronous, active high
Display Select	— High, displays output of counter Low, displays output of latch
Latch Enable	— High, flow through condition Low, latch condition
Clock	— Negative edge sensitive
Segment Output	— Current sourcing with 40 mA @ $V_{OUT} = V_{CC} - 1.6V$ (typ.) Also, sink capability = 2 LTTL loads
Digit Output	— Current sourcing with 1 mA @ $V_{OUT} = 1.75V$. Also, sink capability = 2 LTTL loads
Carry-out	— 2 LTTL loads. See carry-out waveforms.

Absolute Maximum Ratings (Note 1)

Voltage at Any Output Pin	Gnd − 0.3V to V_{CC}+0.3V
Voltage at Any Input Pin	Gnd − 0.3V to +15V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply at $-40°C \leq T_j \leq +85°C$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-out and Digit Output Only)	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5.0V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$•	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		V_{CC}−1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC}−1.6	V_{CC}−1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC}−2	V_{CC}−1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20		Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{JA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

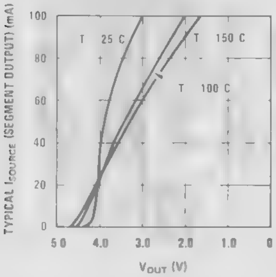
Note 4: θ_{jA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted

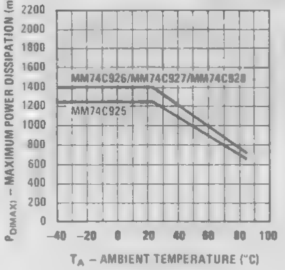
	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$				15	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	$V_{CC} = 5.0V$	$T_j = 25°C$	0	−100		ns
			$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5.0V$			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

Typical Performance Characteristics

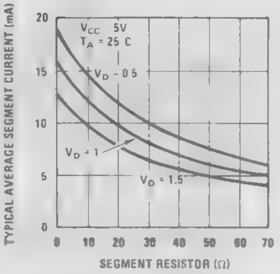
Typical Segment Current vs Output Voltage



Maximum Power Dissipation vs Ambient Temperature



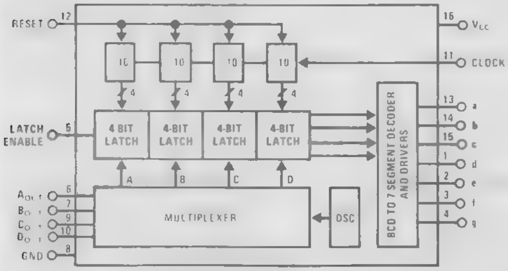
Typical Average Segment Current vs Segment Resistor Value



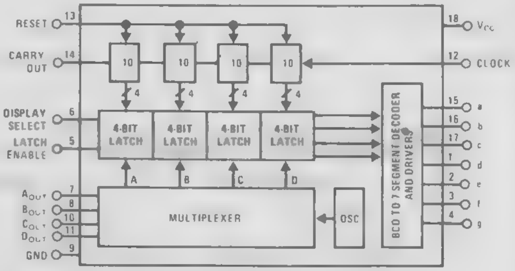
Note. V_D = Voltage across digit driver.

Logic and Block Diagrams

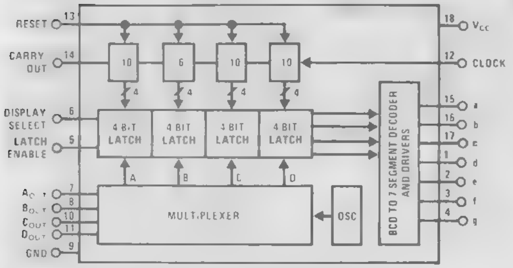
MM74C925



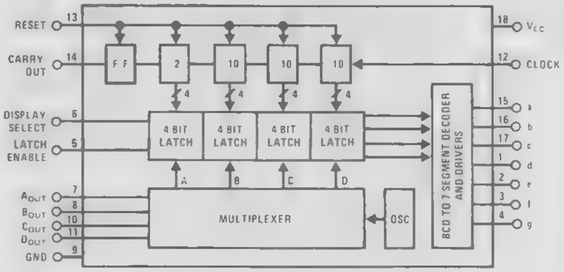
MM74C926

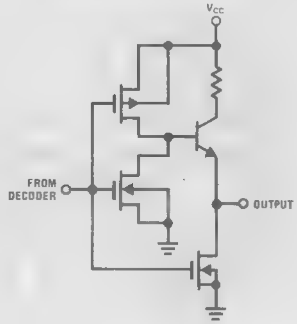


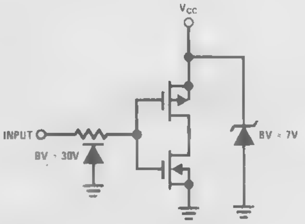
MM74C927

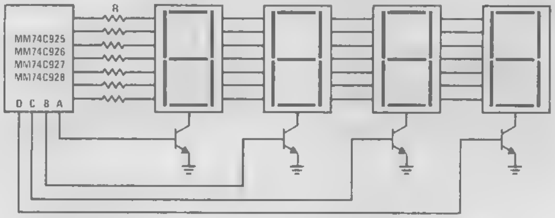


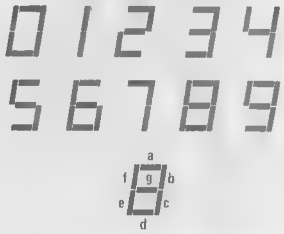
MM74C928



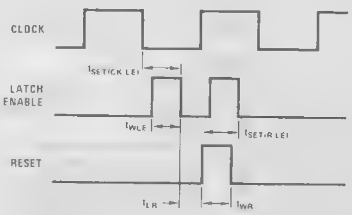

Segment Output Driver

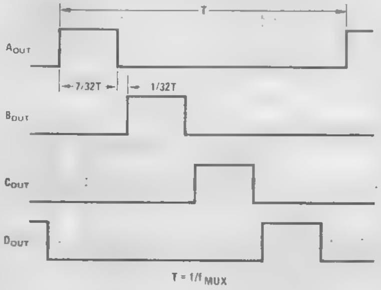

Input Protection

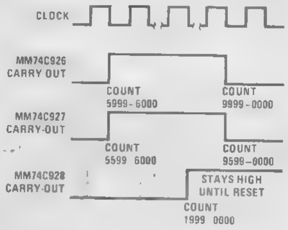

Common Cathode LED Display


Segment Identification

Switching Time Waveforms


Input Waveforms


Multiplexing Output Waveforms


Carry-Out Waveforms

National Semiconductor

MM54C929/MM74C929, MM54C930/MM74C930 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C929/MM74C929 and MM54C930/MM74C930 1024 × 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input $\overline{CS}$.

TRI-STATE is a registered trademark of National Semiconductor Corp.

Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, minicomputer and main-frame-memory applications.

Features

- Fast access — 250 ns max.
- TRI-STATE outputs
- Low power — 10 μA max. standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

See page 4–22
for detailed
specifications

National Semiconductor

MM54C932/MM74C932 Phase Comparator

General Description

The MM74C932/MM54C932 consists of two independent output phase comparator circuits. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

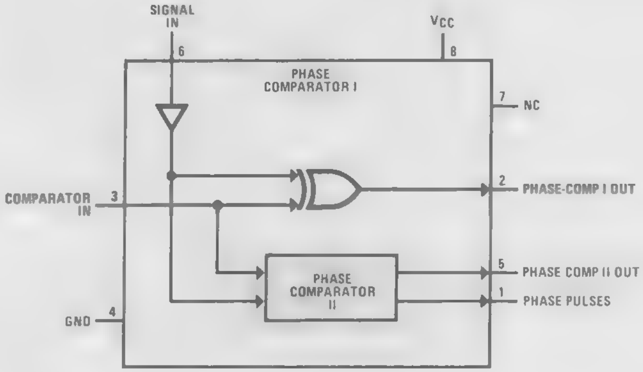
Phase comparator I, an exclusive-OR gate, provides a digital error signal (phase comp. I out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II out) and lock in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

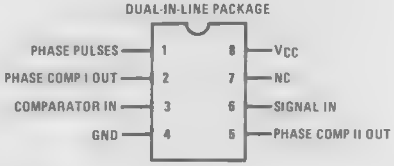
Features

- Wide supply voltage range
- Convenient mini-DIP package
- TRI-STATE® phase-comparator output (comparator II)
- 200 mV input voltage (signal in) sensitivity (typical)

Block Diagram



Connection Diagram



Absolute Maximum Ratings Note 1

Voltage at Any Pin	–0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C932	–55°C to +125°C
MM74C932	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Device Current	PIN 5 = V_{CC}, PIN 8 = V_{CC}, PIN 3 = 0_V				
		V_{CC} = 5V		0.005	150	µA
		V_{CC} = 10V		0.01	300	µA
		V_{CC} = 15V		0.015	600	µA
		PIN 5 = V_{CC}, PIN 8 = Open, PIN 3 = 0_V				
		V_{CC} = 5V		5	205	µA
		V_{CC} = 10V		20	710	µA
		V_{CC} = 15V		50	1800	µA
V_{OL}	Low Level Output Voltage	V_{CC} = 5V		0	0.05	V
		V_{CC} = 10V		0	0.05	V
		V_{CC} = 15V		0	0.05	V
V_{OH}	High Level Output Voltage	V_{CC} = 5V	4.95	5		V
		V_{CC} = 10V	9.95	10		V
		V_{CC} = 15V	14.95	15		V
V_{IL}	Low Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V		2.25	1.5	V
		V_{CC} = 10V, V_O = 1V or 9V		4.5	3.0	V
		V_{CC} = 15V, V_O = 1.5V or 13.5V		6.25	4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V	3.5	2.75		V
		V_{CC} = 10V, V_O = 1V or 9V	7.0	5.5		V
		V_{CC} = 15V, V_O = 1.5V or 13.5V	11.0	8.25		V
I_{OL}	Low Level Output Current	V_{CC} = 5V, V_O = 0.4V	0.36	0.88		mA
		V_{CC} = 10V, V_O = 0.5V	0.9	2.25		mA
		V_{CC} = 15V, V_O = 1.5V	2.4	8.8		mA
I_{OH}	High Level Output Current	V_{CC} = 5V, V_O = 4.6V	–0.36	–0.88		mA
		V_{CC} = 10V, V_O = 9.5V	–0.9	–2.25		mA
		V_{CC} = 15V, V_O = 13.5V	–2.4	–8.8		mA
I_{IN}	Input Current	All Inputs Except Signal Input				
		V_{CC} = 15V, V_{IN} = 0V		-10^{-5}	–1.0	µA
		V_{CC} = 15V, V_{IN} = 15V		10^{-5}	1.0	µA
C_{IN}	Input Capacitance	Any Input, (Note 3)			7.5	pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ, R2 = ∞, VCO_{IN} = $V_{CC}/2$				
		V_{CC} = 5V		0.07		mW
		V_{CC} = 10V		0.6		mW
		V_{CC} = 15V		2.4		mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

R_{IN}	Input Resistance Signal Input	V_{CC} = 5V	1.0	3.0		MΩ
		V_{CC} = 10V	0.2	0.7		MΩ
		V_{CC} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{CC} = 5V		10^6		MΩ
		V_{CC} = 10V		10^6		MΩ
		V_{CC} = 15V		10^6		MΩ
	AC Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000pF f = 50kHz				
		V_{CC} = 5V		200	400	mV
		V_{CC} = 10V		400	800	mV
		V_{CC} = 15V		700	1400	mV

Phase Comparator State Diagrams

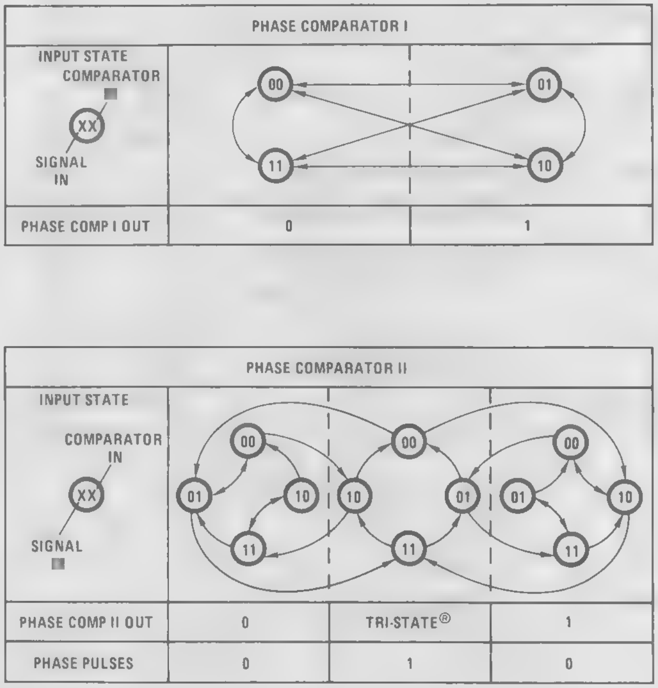


Figure 1.

Typical Waveforms

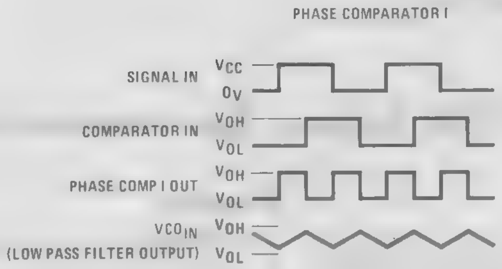


Figure 2. Typical Waveform Employing Phase Comparator I in Locked Condition

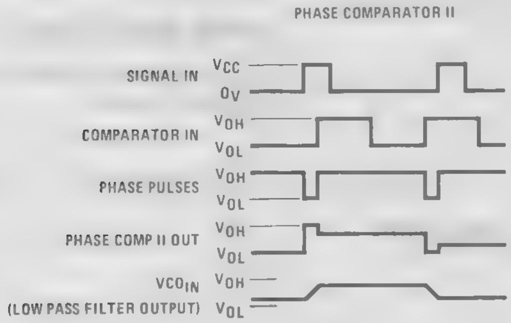
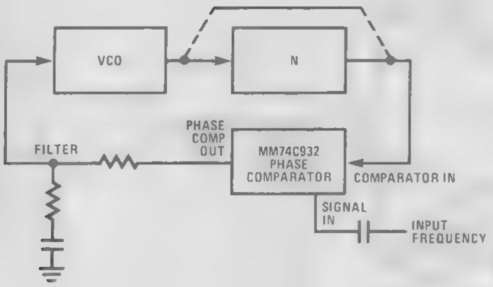


Figure 3. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Phase Locked Loop



National Semiconductor

PRELIMINARY

MM54C933/MM74C933 Address Bus Comparator

General Description

The MM54C933/MM74C933 Bus Comparator compares two binary words of up to 7 bits in length, and determines whether they are equal (bit for bit). Both enable ($\overline{EN}$) inputs must be low to enable the comparison. The output, which is normally high, goes low when inputs A_0–A_6 and B_0–B_6 are equal.

The 'A' set of inputs is provided with latches which allow the inputs to flow through when ALE is high, and are latched when ALE is brought low.

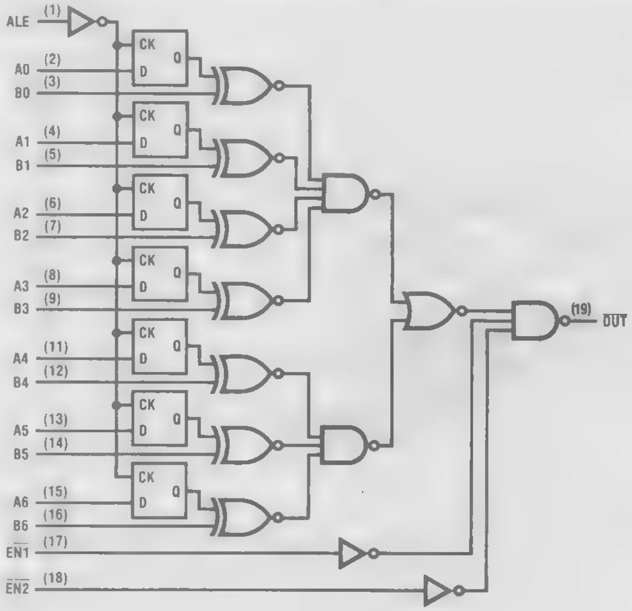
Features

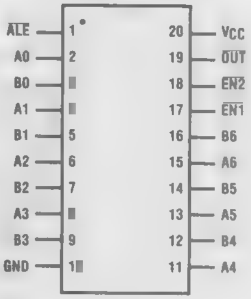
- Silicon Gate CMOS technology used for high speed
- Wide supply voltage range 3–6V
- 2 active low enables for cascading and control
- One set of latched inputs for easy interfacing to multiplexed μP busses
- Active low output compatible with memory and μP peripherals

Typical Applications

- Microprocessor Address/Data Bus decoders
- Equality detectors

Logic and Connection Diagrams





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C933	−55°C to +125°C
MM74C933	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 6.0V
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
V_{IH}	Input High Voltage	$V_{CC}=5.0V$, $V_{OUT}=0.5V$ or $4.5V$	3.5			V
V_{IL}	Input Low Voltage	$V_{CC}=5.0V$, $V_{OUT}=0.5V$ or $4.5V$			1.5	V
V_{OH}	Output High Voltage	$V_{CC}=5.0V$, $I_O=-1\mu A$ $V_{IN}=0V$ or $5.0V$	4.95			V
V_{OL}	Output Low Voltage	$V_{CC}=5.0V$, $I_O=1\mu A$ $V_{IN}=0V$ or $5.0V$			0.05	V
I_{OH}	Output High Current	$V_{CC}=5.0V$, $V_{IN}=0V$ or $5.0V$ $V_O=4.6V$	−2.0			mA
I_{OL}	Output Low Current	$V_{CC}=5.0V$, $V_{IN}=0V$ or $5.0V$ $V_O=0.4V$	+2.0			mA
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=6.0V$, $V_{IN}=V_{CC}$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=6.0V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LSTTL Interface (MM54C933: $V_{CC}=5.0V\pm10\%$, MM74C933: $V_{CC}=5.0V\pm5\%$)					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_O=0.4V$ or $V_{CC}-0.4$ $I_O=\pm10\mu A$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_O=0.4V$ or $V_{CC}-0.4$ $I_O=\pm10\mu A$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{IN}=4.0V$ or $1.0V$ $I_O=-2.0mA$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{IN}=4.0V$ or $1.0V$ $I_O=+2.0mA$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	16			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	16			mA

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PLH}, t_{PHL}	Propagation Delay A to $\overline{OUT}$	$ALE = 5.0V$, $C_L = 15\,pF$ $ALE = 5.0V$, $C_L = 100\,pF$		50 60		ns ns
t_{PLH}, t_{PHL}	Propagation Delay B to $\overline{OUT}$	$C_L = 15\,pF$ $C_L = 100\,pF$		40 50		ns ns
t_{PLH}, t_{PHL}	Propagation Delay $\overline{EN1}$ or $\overline{EN2}$ to $\overline{OUT}$	$C_L = 15\,pF$ $C_L = 100\,pF$		10 20		ns ns
t_{PLH}, t_{PHL}	Propagation Delay ALE to $\overline{OUT}$	$C_L = 15\,pF$ $C_L = 100\,pF$		30 40		ns ns
t_S	Time prior to ALE that A must be present			5.0		ns
t_H	Time after ALE that A must be present			5.0		ns
t_W	Minimum ALE Pulse Width			10		ns
t_T	Output Transition Time	$C_L = 15\,pF$		10		ns
C_{IN}	Input Capacitance	(Note 2)		10		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

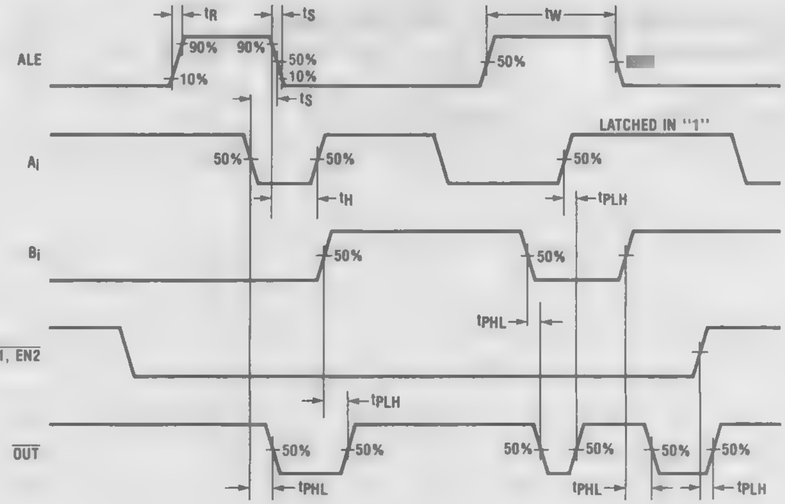
Note 3: C_{PD} determines that no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Truth Tables

$\overline{EN1}$ or $\overline{EN2}$	A_N	B_N	$\overline{OUT}$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	X	X	1

ALE	Function
0	A_N Inputs Latched
1	A_N Inputs Flow-Through

Switching Time Waveforms



National Semiconductor

MM54C941/MM74C941 Octal Buffers/Line Receivers/Line Drivers with TRI-STATE® Outputs

General Description

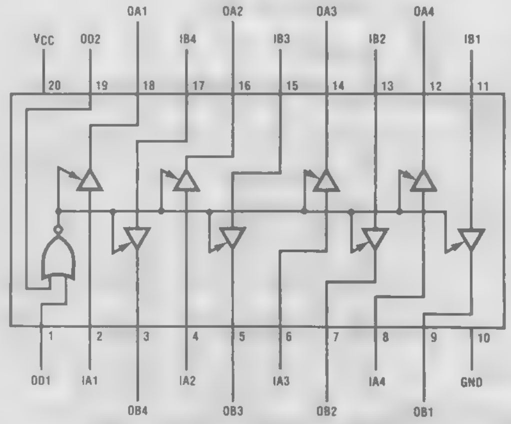
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. When $V_{CC} = 5V$ inputs can accept true TTL high and low logic levels.

TRI-STATE is a registered trademark of National Semiconductor Corp.

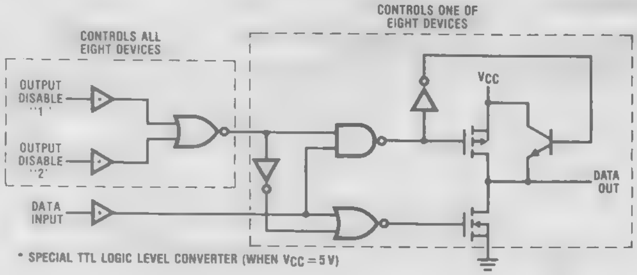
Features

- Wide supply voltage range (3V to 15V)
- Low power consumption
- TTL compatibility (improved on the inputs)
- High capacitive load
- TRI-STATE® outputs
- Input protection
- 20-pin dual-in-line package
- High output drive

Connection Diagram



Logic Diagram



* SPECIAL TTL LOGIC LEVEL CONVERTER (WHEN $V_{CC} = 5V$)

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	0.3V to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C941	−55°C to +125°C
MM74C941	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	2.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			0.8	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, I8 $=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	Tristate Leakage	$V_{CC}=15V$, $V_{OUT}=0V$ or 15V			±3.0	μA
	CMOS/TTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_C=4.5V$	$V_{CC}-2.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-2.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-450\mu A$	$V_{CC}-0.4$			V
		74C, $V_{CC}=4.75V$, $I_O=-450\mu A$	$V_{CC}-0.4$			V
		54C, $V_{CC}=4.5V$, $I_O=-2.2mA$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-2.2mA$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+2.2mA$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=+2.2mA$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−14.0	−30.0		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−36.0	−70.0		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	+12.0	+20.0		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	+48.0	+70.0		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

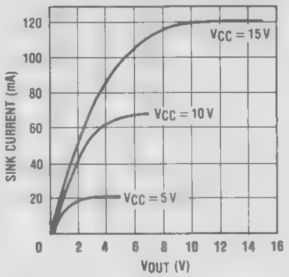
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd1}, t_{pd0}	Propagation Delay (Data IN TO OUT)	$V_{CC} = 5.0V$, $C_L = 50\,pF$		70	140	ns
		$V_{CC} = 10V$, $C_L = 50\,pF$		35	70	ns
		$V_{CC} = 5.0V$, $C_L = 150\,pF$		90	160	ns
		$V_{CC} = 10V$, $C_L = 150\,pF$		45	90	ns
t_{IH}, t_{OH}	Propagation Delay Output Disable to Logic Level (from High Impedance State) (from a Logic Level)	$R_L = 1\,k\Omega$, $C_L = 50\,pF$				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 210V$		55	110	ns
t_{H1}, t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1\,k\Omega$, $C_L = 50\,pF$				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 10V$		55	110	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0V$, $C_L = 50\,pF$		50	100	ns
		$V_{CC} = 10V$, $C_L = 50\,pF$		30	60	ns
		$V_{CC} = 5.0V$, $C_L = 150\,pF$		80	160	ns
		$V_{CC} = 10V$, $C_L = 150\,pF$		50	100	ns
C_{PD}	Power Dissipation Capacitance	(See Note 3)				
	(Output Enabled per Buffer)			100		pF
	(Output Disabled per Buffer)			10		pF
C_{IN}	Input Capacitance (Any Input)	(See Note 2) $V_{IN} = 0V$, $f = 1\,MHz$ $T_A = 25°C$		10		pF
C_O	(Output Capacitance) (Output Disabled)	$V_{IN} = 0v$, $f = 1\,MHz$, $T_A = 25°C$		10		pF

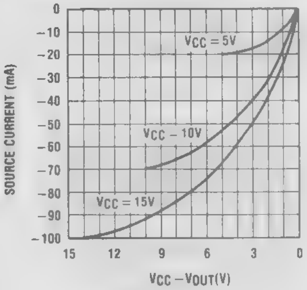
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

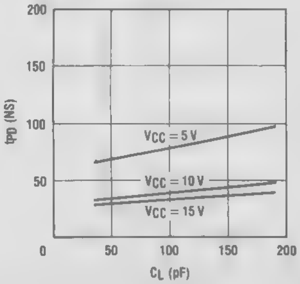
Truth Table

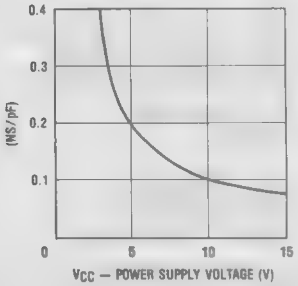
OD1	OD2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	Z
1	0	X	Z
1	1	X	Z

1 = High
0 = Low
X = Don't Care
Z = TRI-STATE®

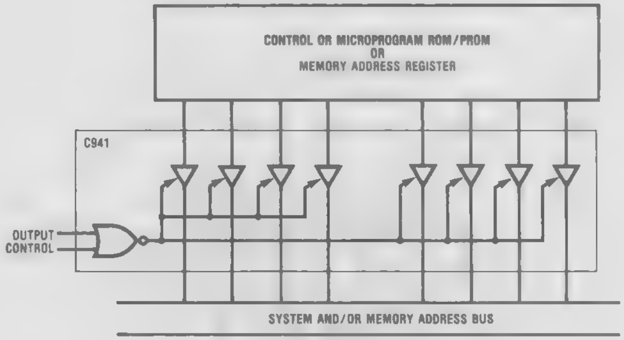

N-Channel Output Drive
@ 25°C


P-Channel Output Drive
@ 25°C

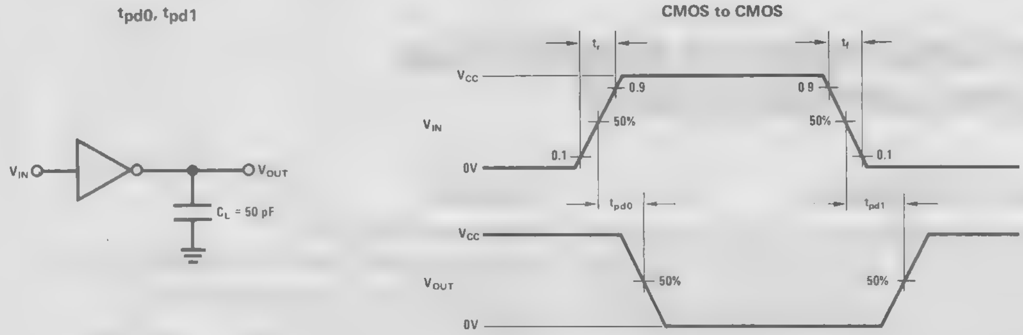

Propagation Delay vs.
Load Capacitance

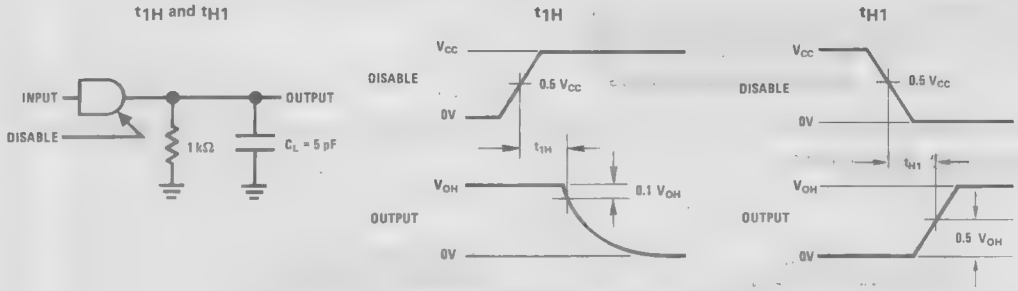

Δ tPD per pF of Load
Capacitance

Applications

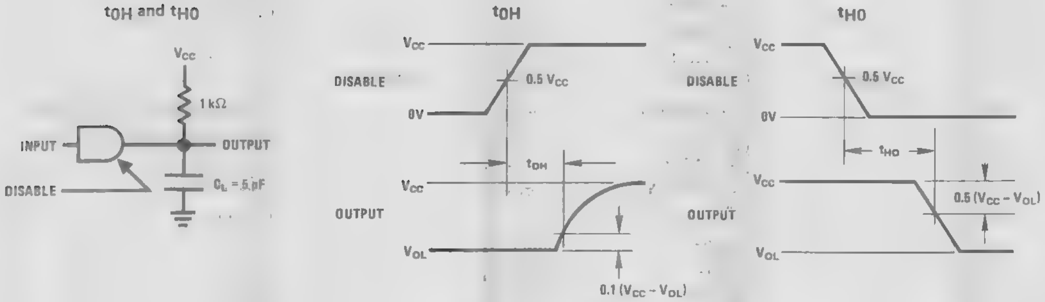

CONTROL OR MICROPROGRAM ROM/PROM
OR
MEMORY ADDRESS REGISTER
C941
OUTPUT
CONTROL
SYSTEM AND/OR MEMORY ADDRESS BUS

AC Test Circuits and Switching Time Waveforms





NOTE: V_{OH} IS DEFINED AS THE DC OUTPUT HIGH VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO GROUND.



NOTE. V_{OL} IS DEFINED AS THE DC OUTPUT LOW VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

ADVANCE INFORMATION

MM74C945, MM74C947 4-Digit Up/Down Counter/Latch/Decoder Driver

General Description

The MM74C945, MM74C947 are 4-digit counters for directly driving LCD displays. The MM74C945 contains a 4-decade up/down counter, output latches, counter/latch select multiplexer and 7-segment decoders. Also included are the backplane oscillator/driver, segment drivers and display blanking circuitry.

The MM74C947 differs from the MM74C945 in that it has no counter/latch multiplexer, but provides true leading zero blanking. All leading zeroes are automatically blanked except the least significant digit, which can be optionally blanked.

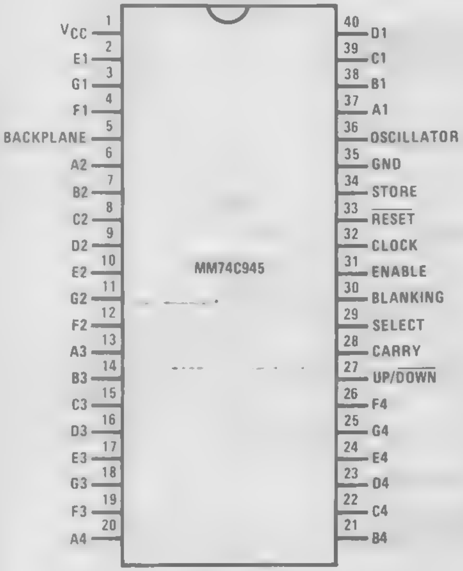
Both devices provide 28-segment outputs to drive a 4-digit display. Segment and backplane waveforms are generated internally, but can also be slaved to an external signal. This facilitates cascading of multiple displays.

Features

- 4-decade up/down count
- Direct 4-digit drive for high contrast and long display life
- Carry/borrow out for cascading counters
- Schmitt trigger clock input
- MM74C945 has display select to allow viewing of counter or latch
- Store and reset inputs allow operation as frequency or period counter
- MM74C947 has true ripple blanking; least significant digit may be optionally blanked

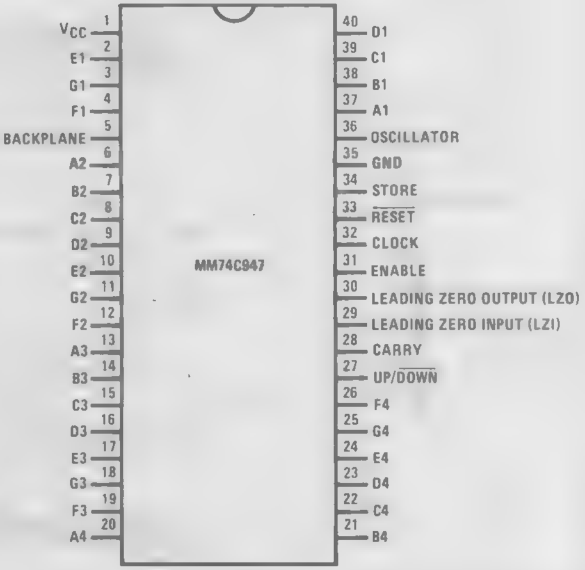
Connection Diagrams

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 6.0V
MM74C945/MM74C947	−40°C to +85°C	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	$V_{CC}=5V$		3.3		V
V_{T-} Negative Going Threshold Voltage (Clock Only)	$V_{CC}=5V$		1.8		V
Hysteresis ($V_{T+}-V_{T-}$) (Clock Only)	$V_{CC}=5V$		1.5		V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Inputs Except Clock)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Inputs Except Clock)	$V_{CC}=5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=-10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=+10\ \mu A$			0.5	V
Logical "1" Input Current ($I_{IN(1)}$) (Note 2)	$V_{CC}=5V$, $V_{IN}=5V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$) (Note 2)	$V_{CC}=5V$, $V_{IN}=0V$	−1.0	−0.005		μA
Oscillator Input Current (I_{OSL})	$V_{CC}=5V$, $V_{IN}=0V/5V$		±2		μA
Supply Current (I_{CC}) (Note 3)	$V_{CC}=5V$, $V_{IN}=0V/5V$		10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) (Clock Input)	$V_{CC}=5V$	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$) (Clock Input)	$V_{CC}=5V$			0.7	V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Inputs Except Clock)	$V_{CC}=5V$	$V_{CC}-1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Inputs Except Clock)	$V_{CC}=5V$			0.4	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=4.75V$, $I_O=-360\ \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=4.75V$, $I_O=360\ \mu A$			0.4	V
OUTPUT DRIVE					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC}=5V$ $T_A=25°C$		2.6		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC}=5V$ $T_A=25°C$		2.8		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC}=5V$ $T_A=25°C$		1.9		mA
Output Sink Current (I_{SINK}) (Segment Output)	$V_{CC}=5V$ $T_A=25°C$		1.6		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC}=5V$ $T_A=25°C$		16.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC}=5V$ $T_A=25°C$		13.0		mA

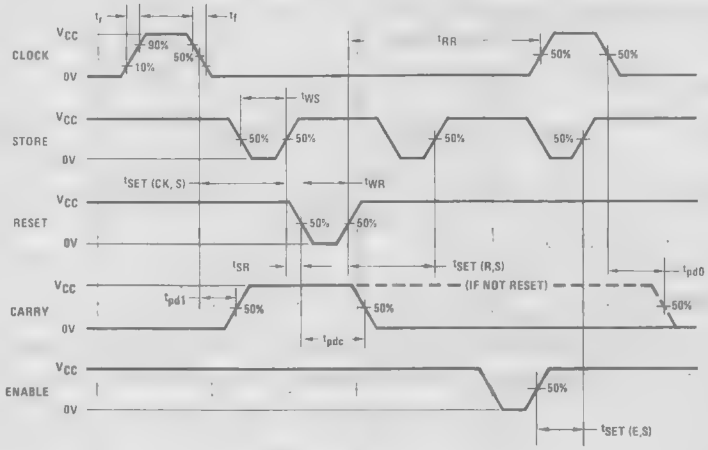
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry					
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$		2		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$			No Limit	µs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$				ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0V$				ns
$t_{SET(CK, S)}$	Clock to Store Set-Up Time	$V_{CC} = 5.0V$				ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0V$				ns
$t_{SET(R, S)}$	Reset to Store Set-Up Time	$V_{CC} = 5.0V$				ns
$t_{SET(E, S)}$	Enable to Store Set-Up Time	$V_{CC} = 5.0V$				ns
t_{RR}	Reset Removal	$V_{CC} = 5.0V$				ns
t_{pdc}	Propagation Delay Reset to Carry	$V_{CC} = 5.0V$				ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating		125		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 2)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{load} = 200$ pF		0.5		µs
t_{rfb}	Backplane Rise/Fall Time	$C_{load} = 5000$ pF		1.5		µs
f_{osc}	Oscillator Frequency	Pin 36 Floating		16		kHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

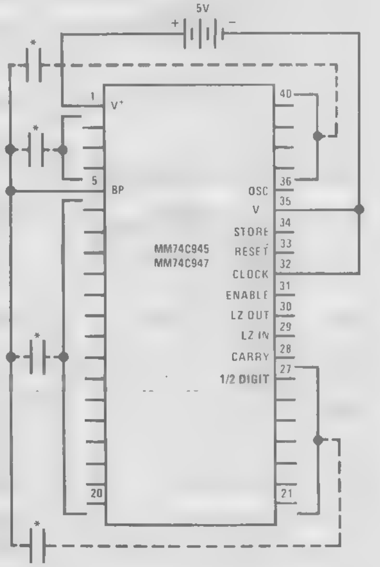
Note 2: Does not apply to backplane and oscillator pins.

Note 3: Display blanked. See test circuit.

AC Waveforms

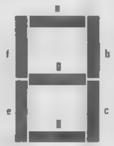


Test Circuit



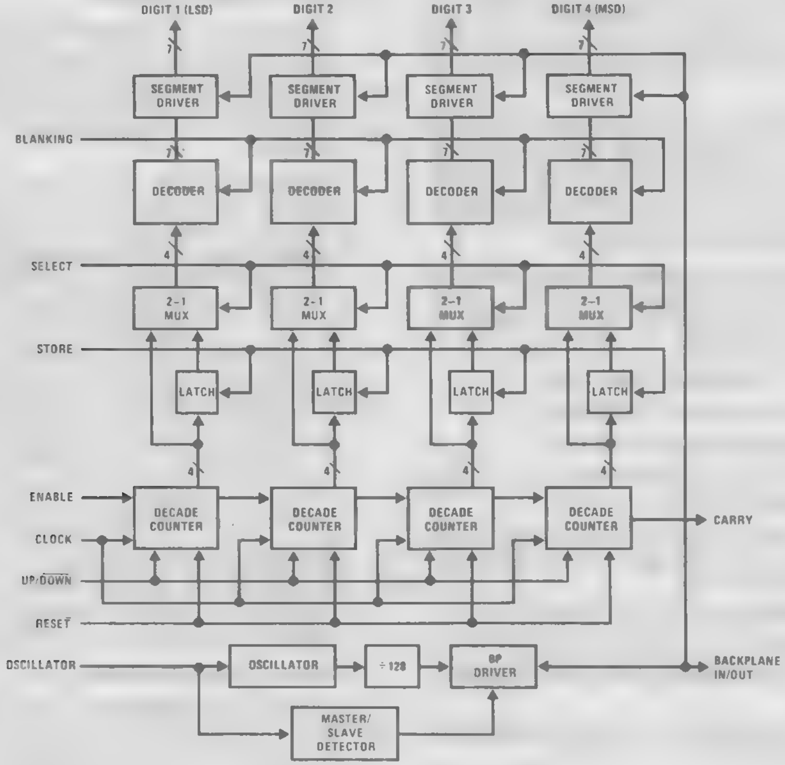
* Each segment to backplane with 200 pF capacitor.

Segment Identification

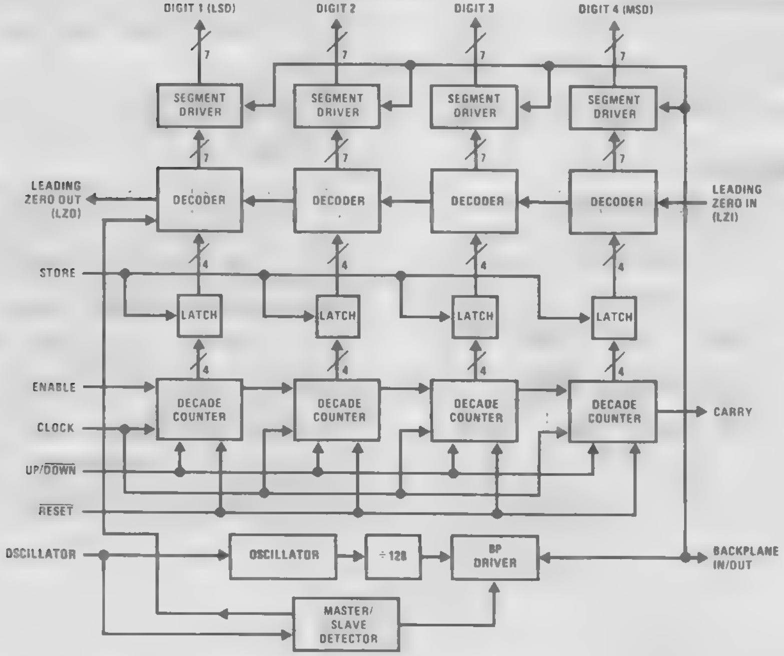


Block Diagrams

MM74C945



MM74C947



Pin Description

Backplane In/Out—When the oscillator input is grounded this pin is an input allowing an external device to generate a backplane waveform. When the oscillator input is left open this pin is an output supplying backplane drive for the display.

Oscillator—The oscillator frequency may be lowered by tying a capacitor to this pin. On the MM74C947 when the oscillator pin is open the LSD is inhibited from blanking when leading zero blanking is enabled. If this pin is grounded the backplanes on both parts become inputs, slaving the device to an external backplane.

Store—This input controls the on-chip latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high, the data on the counter outputs are stored in the latches.

Reset—When low, counters are reset to zero.

Clock—Advances counters on negative edge.

Enable—When low, halts counter operation.

Leading Zero Input (LZI)—(MM74C947) When high, enables leading zero blanking.

Leading Zero Output (LZO)—(MM74C947) This output goes high when the latch contents equal zero, LZI is high and the oscillator pin is open.

Blanking—(MM74C945) When high, blanks display.

Select—(MM74C945) When high, the contents of the counter are displayed. When low, the contents of the latch are displayed.

Carry—This output goes high when 9999 is reached (up) or 0000 is reached (down).

Up/Down—When high, the counter counts up. When low, the counter counts down.

A1-G1—Digit 1 segment outputs.

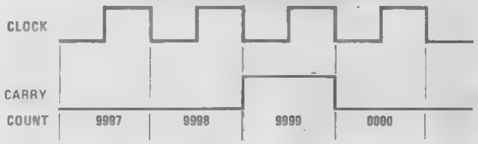
A2-G2—Digit 2 segment outputs.

A3-G3—Digit 3 segment outputs.

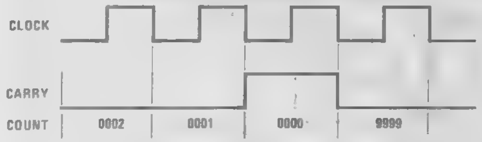
A4-G4—Digit 4 segment outputs.

Timing Diagrams

Carry Out Timing (Up Mode)



Carry Out Timing (Down Mode)



Application Hints

Display Circuitry Description

The MM74C945 and MM74C947 have 28 segment outputs capable of directly driving 4 digits of 7 segments. Both the segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life.

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. This allows several devices to be driven by a single master backplane waveform which can be generated by another MM74C945, MM74C947 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven by several counters. The maximum fanout of a master backplane driver is limited by its total capacitive load, which is the sum of the slaved backplane input capacitances and the display backplane capacitance. (The MM74C947 oscillator pin controls the least significant digit blanking as well.)

An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency is typically 125 Hz, but may be slowed by connecting an external capacitor between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane pin will be put in the slave (input) mode.

Counter Circuitry Description

The MM74C945, MM74C947 are 4-decade up/down counters. The direction of the count is controlled by the up/down input. A high level on this pin causes the counter to count up. The counter advances on the negative clock edge. The carry output is high for 1 clock period during a count of 9999 in up mode and also high during a count of 0000 in down mode. The carry is designed to enable cascading of several circuits in either ripple carry or synchronous modes.

Reset and Enable controls are provided to allow period and frequency measurements. The Reset control clears the counter when low and the Enable control disables counting when taken low.

The counter chain feeds a series of 4-bit flow-through latches. These latches enable the display to follow the counter when the Store input is low. When the Store pin is taken high the data on the counter outputs at this time become latched and the display will remain unchanged. (Assuming the latch display is selected on MM74C945.)

On the MM74C945 the latch outputs feed a multiplexer which selects either the latch outputs or counter outputs for display. This allows an intermediate count to be stored in the latches while the counter continues to be displayed. This is equivalent to a stopwatch lap feature.

The output of the MM74C945's multiplexer feeds a decoder which converts 4-bit input to 7-segment. A blank control into these decoders blanks the display.

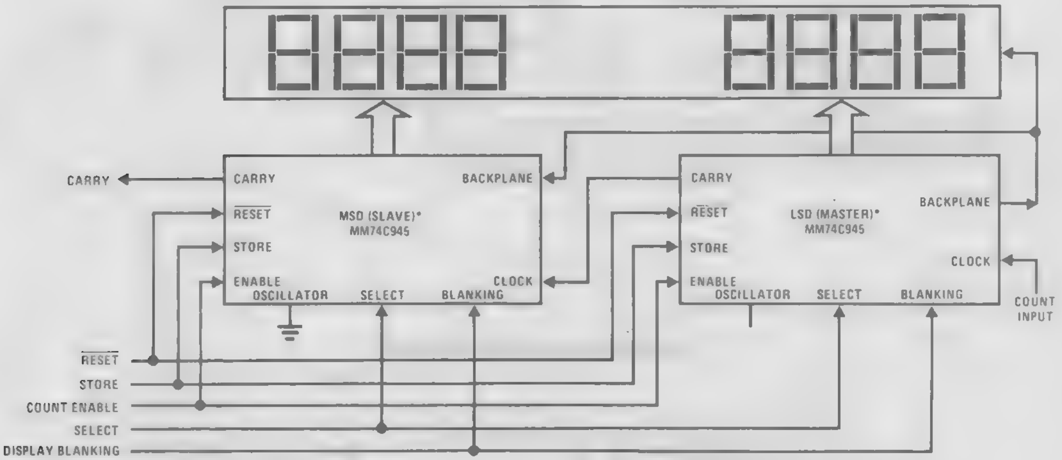
Application Hints (Continued)

On the MM74C947 the latch outputs feed the decoders directly, but these decoders have a special ripple blanking capability that enables all leading zeroes except the least significant digit (LSD) to be blanked, even when counters are cascaded. Thus when the entire counter reads zero, instead of blanking all digits, the LSD will remain on. (When multiple counters are cascaded, all except the least significant counter will blank entirely on zeroes.) This feature is properly implemented by configuring the least significant device as the master (oscillator pin ungrounded) thereby inhibiting LSD blanking.

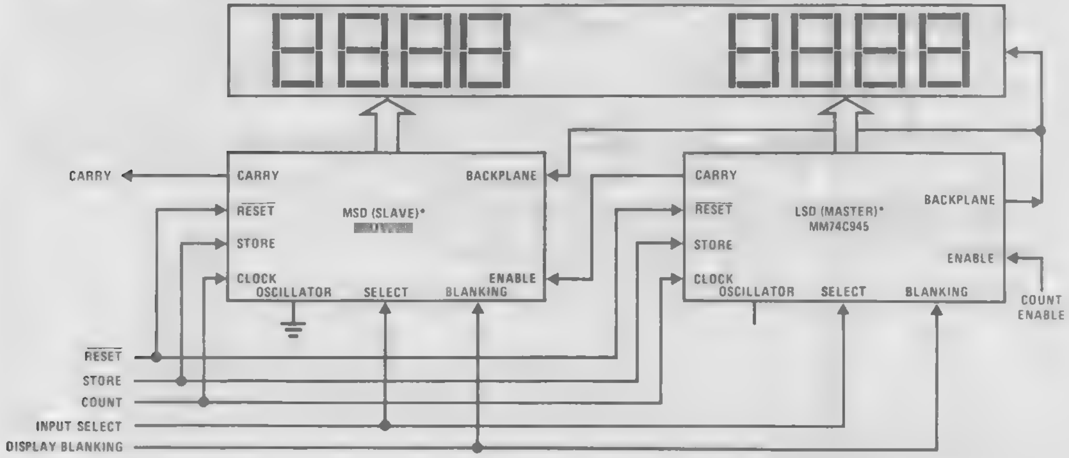
The outputs of the decoders for both devices control the segment drivers which in turn enable display operation.

Typical Applications

Ripple Carry Cascading—MM74C945



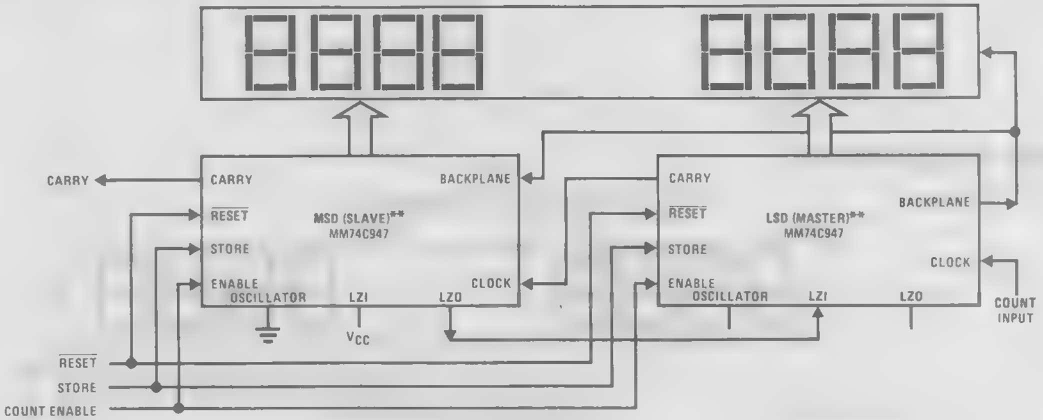
Synchronous Cascading—MM74C945



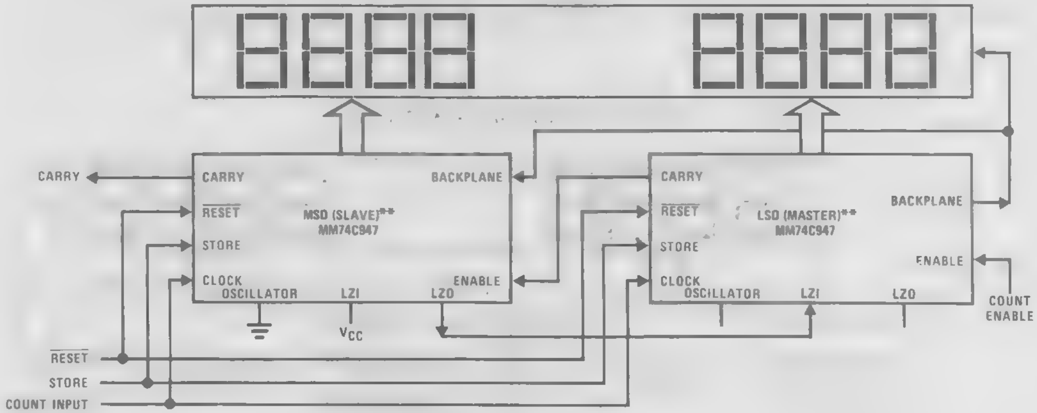
* Master/slave selecton is arbitrary and dependent only on which oscillator pin is grounded.

Typical Applications (Continued)

Ripple Cascading—MM74C947



Synchronous Cascading—MM74C947



** To correctly implement leading zero blanking the least significant device must be the master.

National Semiconductor

ADVANCE INFORMATION

MM74C946 4½-Digit Counter/Decoder/Driver for LCD Displays

General Description

The MM74C946 is a 4½-digit CMOS counter which contains a counter chain, decoders, output latches, LCD segment drivers, count inhibit and backplane oscillator/driver circuitry. This device also contains leading zero blanking and a carry output to increase flexibility and facilitate cascading of multiple 4-digit sections.

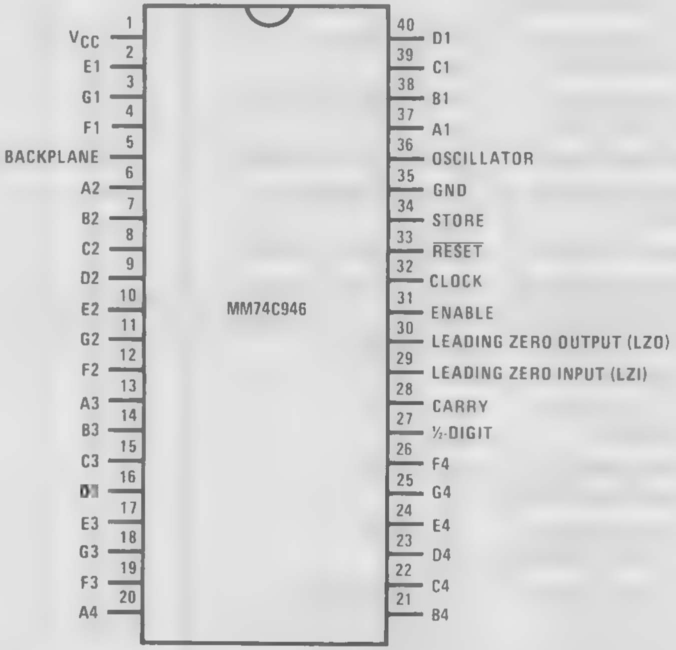
This device provides 29 segment outputs to drive a standard 4½-digit liquid crystal display. An on-chip backplane oscillator/driver is also provided. This can be disabled by grounding the oscillator pin, thus allowing the device to be slaved to an external backplane signal via the backplane pin.

Features

- Low power operation—less than 100 μW quiescent
- Direct 4½-digit 7-segment display drive for higher contrast and long display life
- Pin compatible to Intersil's ICM7224
- Store and Reset inputs permit operation as frequency or period counter
- True count inhibit disables first counter stage
- Carry output for cascading 4-digit blocks
- Schmitt trigger on the clock input allows operation in noisy environments or with slowly changing inputs
- Leading zero blanking input and output for correct leading zero blanking with cascaded devices
- On-chip backplane oscillator/driver which can be disabled to permit slaving of multiple devices to an external backplane signal

Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range MM74C946	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Input)	$V_{CC}=5V$		3.3		V
V_{T-} Negative Going Threshold Voltage (Clock Input)	$V_{CC}=5V$		1.8		V
Hysteresis ($V_{T+}-V_{T-}$) (Clock Input)	$V_{CC}=5V$		1.5		V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Inputs Except Clock Input)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Inputs Except Clock Input)	$V_{CC}=5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=-10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=+10\ \mu A$			0.5	V
Clock Input Current $\|I_{IN}\|$	$V_{CC}=5V$, $V_{IN}=5V/0V$		0.005	1.0	µA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC}=5V$, $V_{IN}=0V$	−2.0		−25.0	µA
Oscillator Pin Current (I_{OSL})	$V_{CC}=5V$, $V_{IN}=0V/5V$		±2		µA
Supply Current (I_{CC}) (Note 3)	$V_{CC}=5V$, $V_{IN}=0V/5V$		10		µA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) (Clock Input)	$V_{CC}=5V$	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$) (Clock Input)	$V_{CC}=5V$			0.7	V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Input Except Clock)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Input Except Clock)	$V_{CC}=5V$			0.4	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.4 0.4	V V

DC Electrical Characteristics (Continued)

(I_{SOURCE}) (LZO and Carry)	$T_A = 25°C$				
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC} = 5V$ $T_A = 25°C$		2.8		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC} = 5V$ $T_A = 25°C$		1.9		mA
Output Sink Current (I_{SINK}) (Segment Outputs)	$V_{CC} = 5V$ $T_A = 25°C$		1.6		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC} = 5V$ $T_A = 25°C$		16.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC} = 5V$ $T_A = 25°C$		13.0		mA
Output Source Current (I_{SOURCE}) (½-Digit)	$V_{CC} = 5V$ $T_A = 25°C$		3.8		mA
Output Sink Current (I_{SINK}) (½-Digit)	$V_{CC} = 5V$ $T_A = 25°C$		3.2		mA

AC Electrical Characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified.

	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	$V_{CC} = 5.0V$				
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$		2		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$			No Limit	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$				ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0V$				ns
$t_{SET(CK, S)}$	Clock to Store Set-Up Time	$V_{CC} = 5.0V$				ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0V$				ns
$t_{SET(R, S)}$	Reset to Store Set-Up Time	$V_{CC} = 5.0V$				ns
$t_{SET(E, S)}$	Enable to Store Set-Up Time	$V_{CC} = 5.0V$				ns
t_{RR}	Reset Removal	$V_{CC} = 5.0V$				ns
t_{pdc}	Propagation Delay Reset to Carry	$V_{CC} = 5.0V$				ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating		125		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 4)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{load} = 200$ pF		0.5		μs
t_{rfb}	Backplane Rise/Fall Time	$C_{load} = 5000$ pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating		16		kHz

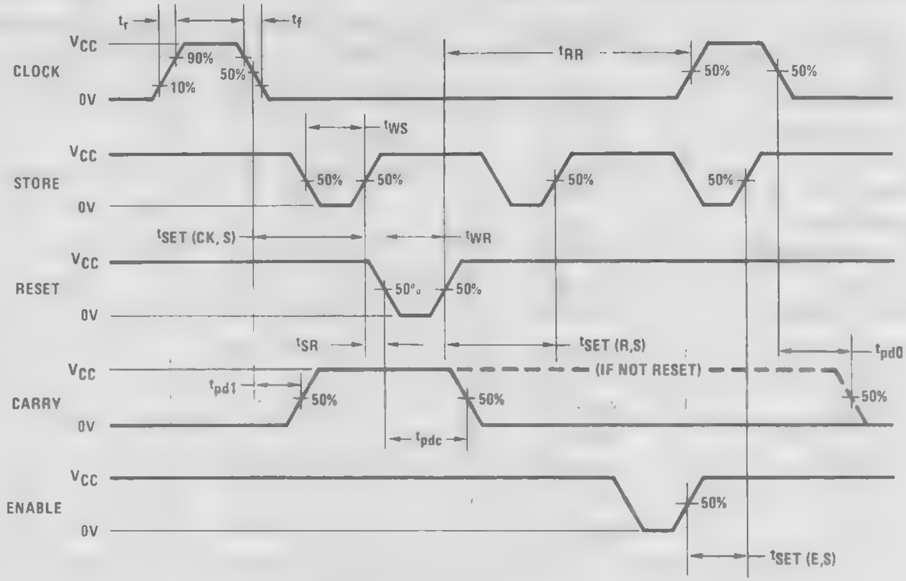
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These input pins have pull-ups to V_{CC}.

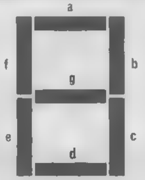
Note 3: See test circuit. Display blanked.

Note 4: Does not apply to backplane and oscillator pins.

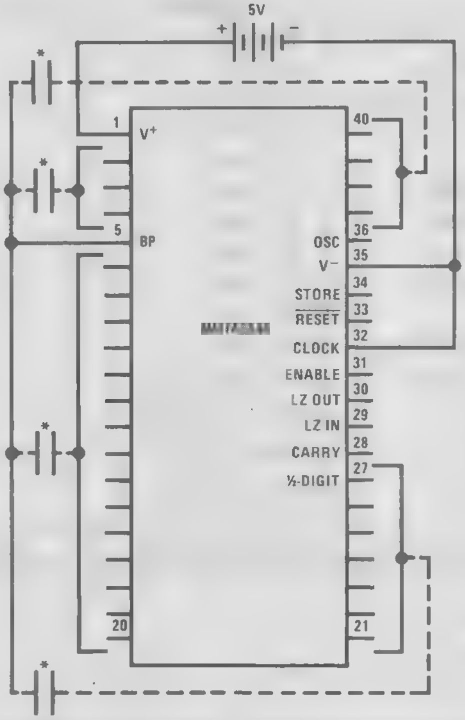
AC Waveforms



Segment Identification

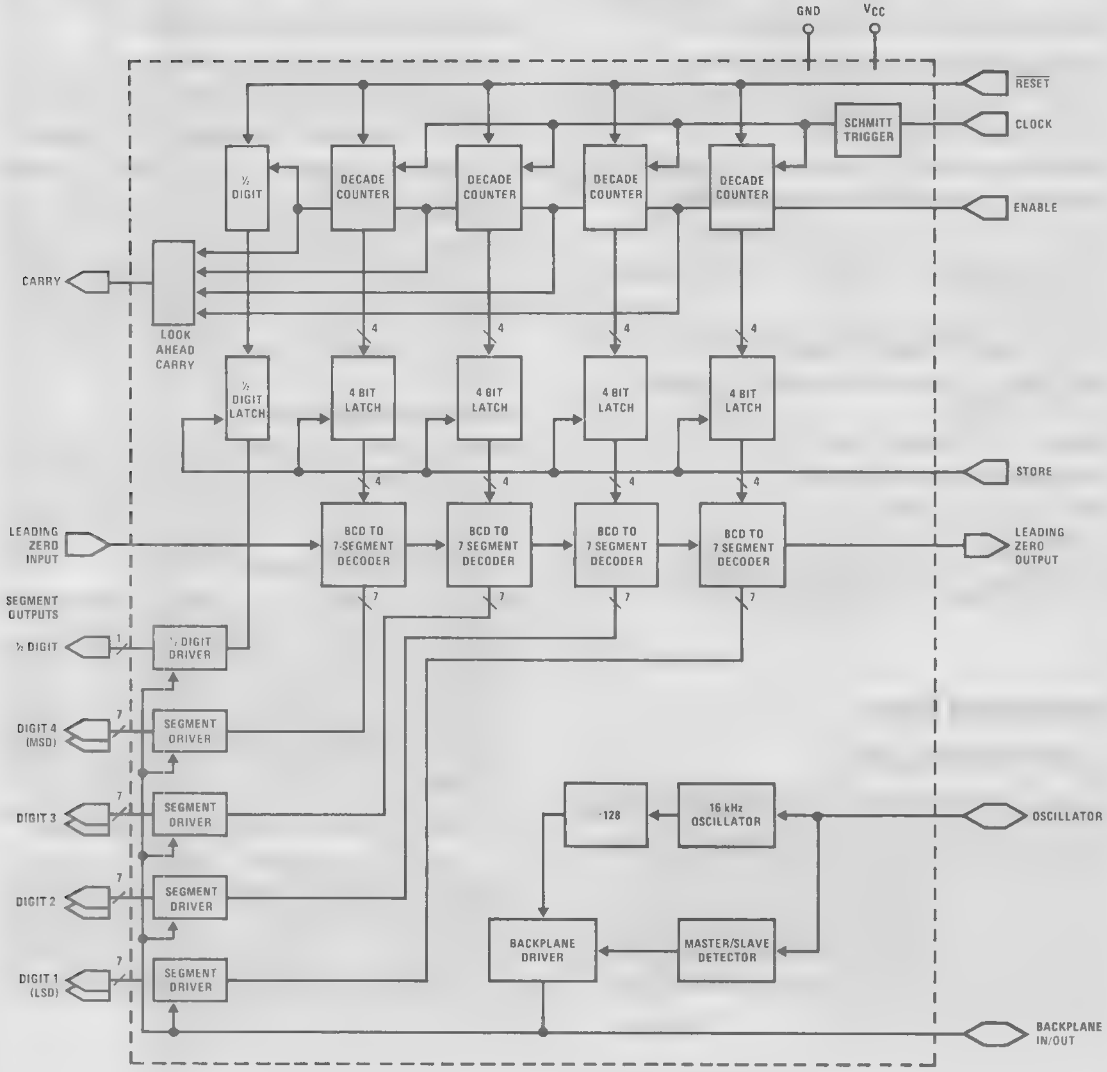


Test Circuit



* Each segement to backplane with 200 pF capacitor.

Block Diagram



an LCD.

Oscillator—The oscillator frequency may be lowered by tying a capacitor between this pin and ground. If this pin is grounded the backplane pin becomes an input.

Store Input—This controls the latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high data on counter outputs is stored in latches and displayed.

Reset Input—When low, counters are reset to zero.

Clock Input—Advances counter on negative edge.

Enable Input—When low, halts counter operation.

Leading Zero Input (LZI)—When high, enables leading zero blanking.

Leading Zero Output (LZO)—This signal goes high when counter equals zero and LZI is high.

Carry Output—Goes high for one clock period when count of 9999 is reached.

A1–G1—Digit 1 segment outputs.

A2–G2—Digit 2 segment outputs.

A3–G3—Digit 3 segment outputs.

A4–G4—Digit 4 segment outputs.

½-Digit Output—Goes high when count goes from 9999 to 0000 and stays high until Reset goes low.

Application Hints

Counter Circuitry Description

The MM74C946 contains a 4-digit resettable synchronous counter with a Schmitt trigger on the clock input. An additional D flip-flop clocked by the counter carry out provides a true ½-digit, or it can be used to indicate an overflow condition. The counters increment on the negative clock edge. The ½-digit sets on the negative clock edge which increments the counter past 9999. It can be reset only when the counter is reset by taking the reset pin to ground. The counter and carry output operation is independent of the state of the ½-digit flip-flop.

using the enable input.

The counter can be inhibited from responding to clock input pulses by taking the enable input low, thus freezing the counter to its state prior to the event.

The counter outputs feed a series of flow-through latches. When the store input is low, the latch outputs follow their inputs. When the store input is taken high, the contents of the counter are stored in the latches and are displayed.

The latch outputs feed 4 decimal to 7-segment decoders which include circuitry to provide leading zero blanking. When the leading zero input is low or the ½-digit is set, leading zero blanking is inhibited. When the leading zero input is high, all leading zeroes will be blanked. A leading zero output is provided to allow correct blanking of all leading zeroes in multiple device designs. This output will be high when all 4 digits are blanked. (Remember the leading zero input must be high and the ½-digit must be reset.)

Display Circuitry Description

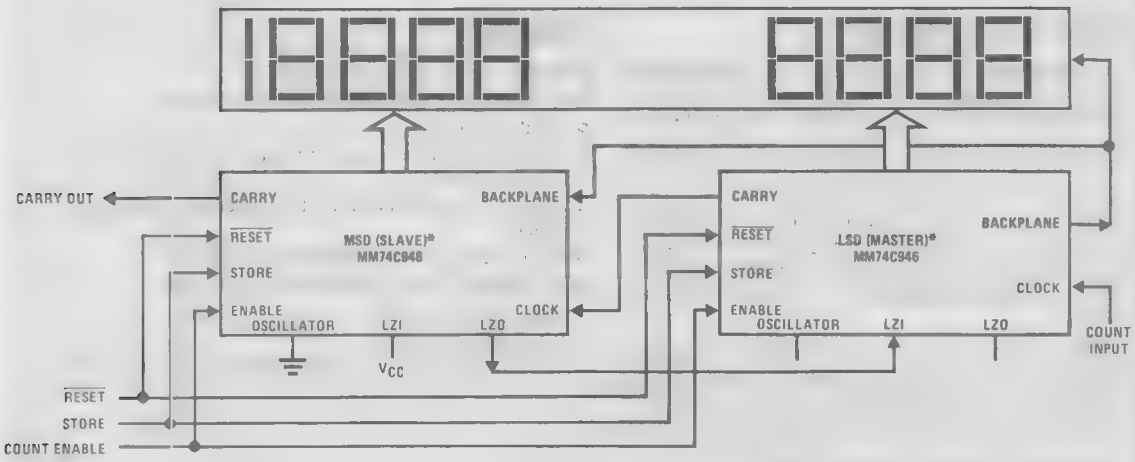
The MM74C946 has 30 segment outputs capable of directly driving 4 digits of 7 segments plus an additional ½-digit of 2 segments. The segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life.

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. This allows several devices to be driven by a single master backplane waveform which can be generated by another MM74C946 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven by multiple counters. The maximum fanout of a master backplane driver is limited by its total capacitive load which is the sum of the slaved backplane input capacitances and the display backplane capacitance.

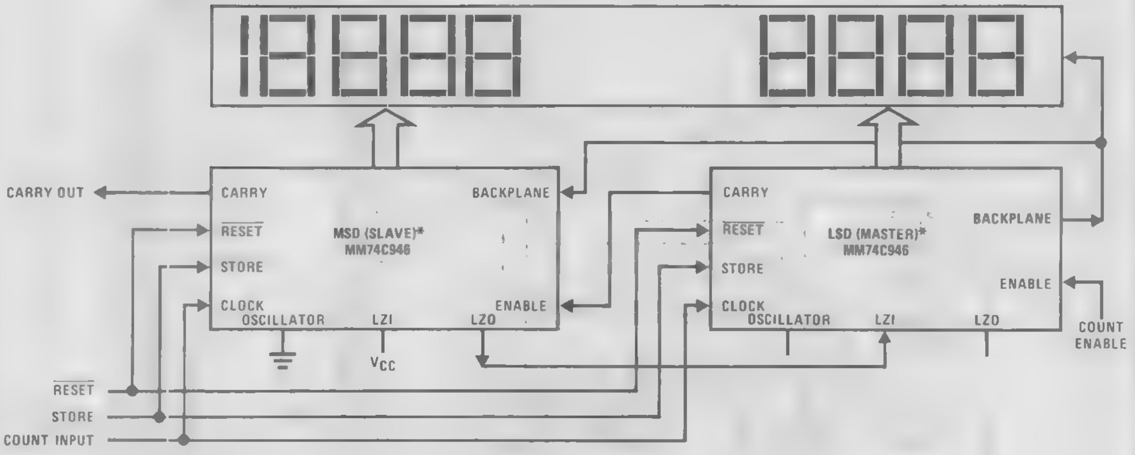
An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency typically is 125 Hz, but may be slowed by connecting an external capacitor between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane will be put in the slave mode.

Typical Applications

Ripple Carry Cascading



Synchronous Cascading



* Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

National Semiconductor

PRELIMINARY

MM74C956 4-Digit, 17-Segment Alpha-Numeric Display Driver, with Memory, Decoder, and LED Drivers

General Description

The MM74C956 monolithic LED intelligent display driver circuit is manufactured using standard complementary MOS technology. The convention and speed of the data entry procedure is designed to be microprocessor bus and TTL compatible with no interface circuitry required.

The integrated circuit has memory to store four 7-bit ASCII words corresponding to the four digits, an ASCII to 17-segment alpha-numeric ROM decoder, multiplexing and drive circuitry to drive four 17-segment digits. It has direct drive capabilities of 2.5 mA/segment average current.

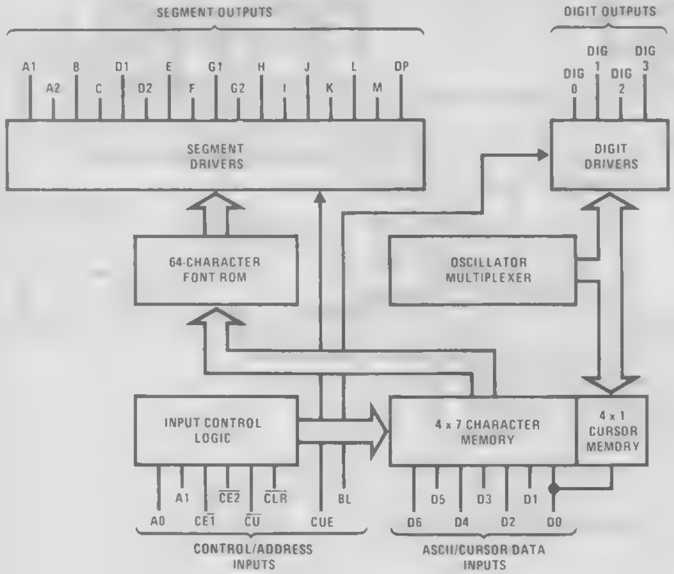
The internal memory can be written asynchronously through the 7-bit data bus (D0–D6) into the digit location addressed by the 2-bit address bus (A0, A1). For multiple chip circuits, two chip select inputs ($\overline{CE1}$, $\overline{CE2}$) can be decoded or a one-of-n decoder can be used for displays incorporating more than four MM74C956's.

The cursor function will cause all segments of a digit to be lit but will not write over the contents of the memory corresponding to that digit. Therefore, when the cursor is erased, the original character will reappear at that digit location.

Features

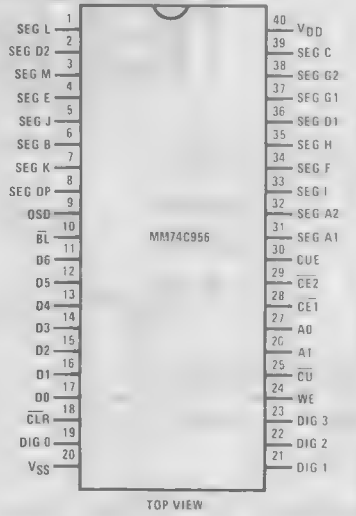
- Microprocessor bus compatible
- All inputs are TTL compatible; 5V power supply
- On-chip memory
- On-chip decoder converts from standard 7-bit ASCII to alpha-numeric
- On-chip multiplexing with LED segment and digit drivers
- Independent and asynchronous digit access
- Independent cursor function: can be disabled
- Display clear function
- Display blank function
- Two chip select inputs for multiple chip systems

Block Diagram



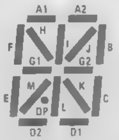
Connection Diagram

Dual-In-Line Package



TOP VIEW

Segment Designation



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range MM74C956	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	700 mW
Operating V_{CC} Range	4.5V to 5.5V
V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 25°C$

Parameter		Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	2.4			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 5V$		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	−100.0	25.0		µA
I_{CC}	Supply Current	$V_{CC} = 5V$ @ $T_A = 25°C$ All Outputs Open All Inputs @ 5V		0.5	1.0	mA
OUTPUT DRIVE (Notes 2 and 3)						
Peak Output Source Current (I_{SOURCE}) (P-Channel Segment Driver with 1 Segment On)		$V_{CC} = 5.0V$, $V_{OUT} = 1.9V$ $T_A = 25°C$			14.8	mA
Peak Output Source Current (I_{SOURCE}) (P-Channel Segment Driver with 17 Segments On)		$V_{CC} = 10V$, $V_{OUT} = 3.3V$ $T_A = 25°C$	4.2			mA
Peak Output Sink Current (I_{SINK}) (N-Channel Digit Driver with 3 Segments On)		$V_{CC} = 5.0V$, $V_{OUT} = 0.25V$ $T_A = 25°C$	18.5			mA
Peak Output Sink Current (I_{SINK}) (N-Channel Digit Driver with 17 Segments On)		$V_{CC} = 10V$, $V_{OUT} = 1.3V$ $T_A = 25°C$			172.0	mA

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$

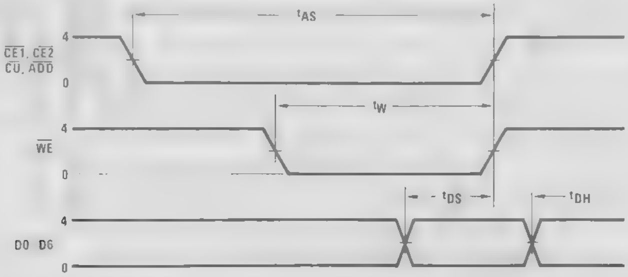
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_W	Write Pulse Width	All Inputs Swing from 0V–4V	240			ns
t_{DS}	Data Set-Up Time	All Inputs Swing from 0V–4V	100			ns
t_{DH}	Data Hold Time	All Inputs Swing from 0V–4V	50			ns
t_{AS}	Address Set-Up Time	All Inputs Swing from 0V–4V	300			ns
t_{AH}	Address Hold Time	All Inputs Swing from 0V–4V	0			ns
t_{CLR}	Clear Time	All Inputs Swing from 0V–4V	1			µs

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating Range they are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

Note 2: Average drive current ≈ peak drive current ÷ 4.

Note 3: Current/segment is dependent upon total number of segments on. Maximum current occurs with 1 segment on; minimum current occurs with 17 segments on.

Timing Diagram for data access


t_{AS}
4
$\overline{CE1}$, $\overline{CE2}$
$\overline{CU}$, $\overline{ADD}$
0
t_W
4
$\overline{WE}$
0
t_{DS}
t_{DH}
4
D0 D6
0

To enter an ASCII code, the $\overline{CE1}$ and $\overline{CE2}$ inputs must be low, $\overline{CU}$ must be high. When the address is set up at A0 and A1, the $\overline{WE}$ can go low, at which time the internal RAM will respond to the data inputs (D0–D6). Note that the data need not be set up prior to the $\overline{WE}$ transition.

All digits can be cleared by holding the $\overline{CLR}$ input low for the specified interval.

Entry into Cursor Memory

This is accomplished by setting the $\overline{CE1}$ and $\overline{CE2}$ inputs as well as the $\overline{CU}$ input low. The cursor memory consists of 4 bits corresponding to the four digits, each one addressable by way of the A0 and A1 inputs. Once the address is stable, the $\overline{WE}$ input must go low and the cursor memory will respond to the D0 input. That is, if D0 is high, a cursor will be written and if D0 is low, the cursor will be erased. $\overline{CLR}$ will not erase a cursor. A cursor will only be displayed when CUE is high and the cursor function can be bypassed by tying CUE low. A flashing cursor can be implemented by pulsing CUE; this results in alternately displaying the cursor and the character originally written in that digit. CUE will not alter the contents of either the cursor or data memory.

Display blanking can be realized by using taking $\overline{BL}$ low, the display will be disabled while leaving the contents of the data and cursor memory unchanged. A flashing display will occur if $\overline{BL}$ is pulsed. The display is blanked by $\overline{BL}$ regardless of whether a cursor or character is being displayed.

Illegal Code

If an illegal ASCII code is entered into the data memory (i.e., D6 = D5) the display will automatically be blanked for the corresponding digit.

OSD Pin

Taking the OSD pin high disables the internal oscillator and prohibits normal multiplex scanning. This pin is pulled low internally and is primarily meant to be used in testing the part only. This pin should be grounded or left open in normal operation.

Clearing the Display

Pulsing the $\overline{CLR}$ pin low for the specified time will clear all internal data memories while leaving the cursor memories unchanged.

TABLE I. DATA AND CURSOR ENTRY FUNCTION EXAMPLE

Assume initially D6 = 1 and D5 – D0 = 0 for all internal digit memories. Cursor memory is cleared. Table is intended to be read in sequence.

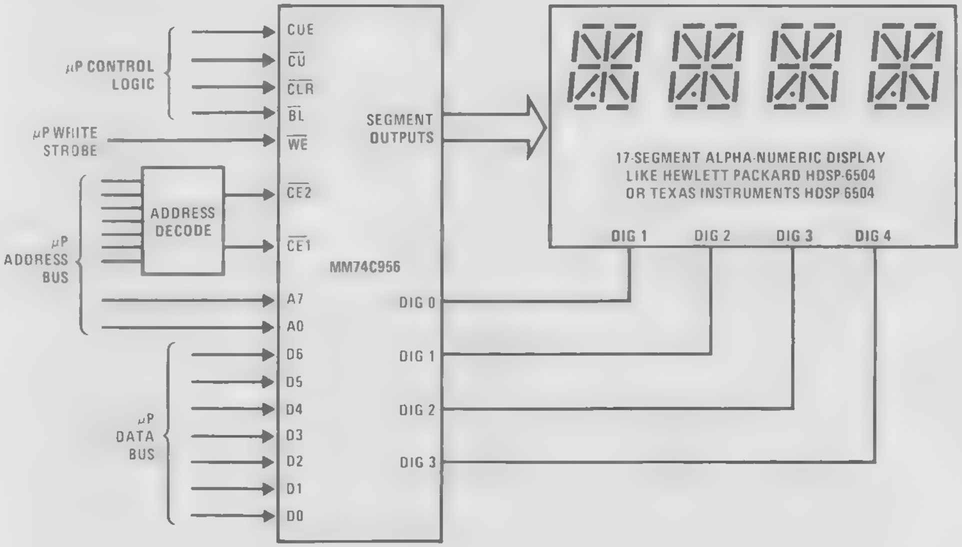
	BL	CE1	CE2	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	A0	D6	D5	D4	D3	D2	D1	D0	DIG 3	DIG 2	DIG 1	DIG 0
DATA ENTRY FUNCTION	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X				
	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	@	@	@	@
	1	0	1	X	X	X	1	X	X	X	X	X	X	X	X	X	@	@	@	@
	1	0	0	X	X	1	1	X	X	X	X	X	X	X	X	X	@	@	@	@
	1	0	0	X	1	0	1	0	0	1	0	0	0	1	1	1	@	@	@	G
	1	0	0	X	1	0	1	1	0	0	1	1	0	1	0	0	@	4	@	G
	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X				
	1	0	0	X	1	0	1	0	0	1	0	0	0	0	0	1				A
	1	0	0	X	1	0	1	0	1	1	0	0	0	0	1	0			B	A
	1	0	0	X	1	0	1	1	0	1	0	0	0	0	1	1		C	B	A
	1	0	0	X	1	0	1	1	1	1	0	0	0	1	0	0	D	C	B	A
CURSOR ENTRY FUNCTION	1	0	0	1	0	0	1	0	0	X	X	X	X	X	X	1	D	C	B	▩
	1	0	0	1	0	0	1	0	1	X	X	X	X	X	X	1	D	C	▩	▩
	1	0	0	1	0	0	1	1	1	X	X	X	X	X	X	1	▩	C	▩	▩
	1	0	0	1	0	0	1	1	0	X	X	X	X	X	X	1	▩	▩	▩	▩
	1	X	X	0	1	1	1	X	X	X	X	X	X	X	X	X	D	C	B	A
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X	▩	▩	▩	▩
	1	0	0	1	0	0	1	0	0	X	X	X	X	X	X	0	▩	▩	▩	A
	1	0	0	0	0	0	1	1	0	X	X	X	X	X	X	0	D	C	B	A
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X	▩	C	▩	A
	0	X	X	X	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X	▩	C	▩	A
	1	X	X	1	1	X	0	X	X	X	X	X	X	X	X	X	▩		▩	
	1	0	0	1	0	0	1	1	1	X	X	X	X	X	X	0			▩	
	1	0	0	1	0	0	1	0	1	X	X	X	X	X	X	0				

X = don't care

TABLE II. ROM OUTPUT FONT FOR ASCII TO ALPHA-NUMERIC DECODING

Character Set			D0	L	H	L	H	L	H	L	H
			D1	L	L	H	H	L	L	H	H
			D2	L	L	L	L	H	H	H	H
D6	D5	D4	D3								
L	H	L	L		!	"	#	$	%	&	'
L	H	L	H	(	)	*	+	,	-	.	/
L	H	H	L	0	1	2	3	4	5	6	7
L	H	H	H	8	9	:	;	<	=	>	?
H	L	L	L	@	A	B	C	D	E	F	G
H	L	L	H	H	I	J	K	L	M	N	O
H	L	H	L	P	Q	R	S	T	U	V	W
H	L	H	H	X	Y	Z	[	\	]	^	_

Typical Application



Section 3

CMOS A/D Converters

National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

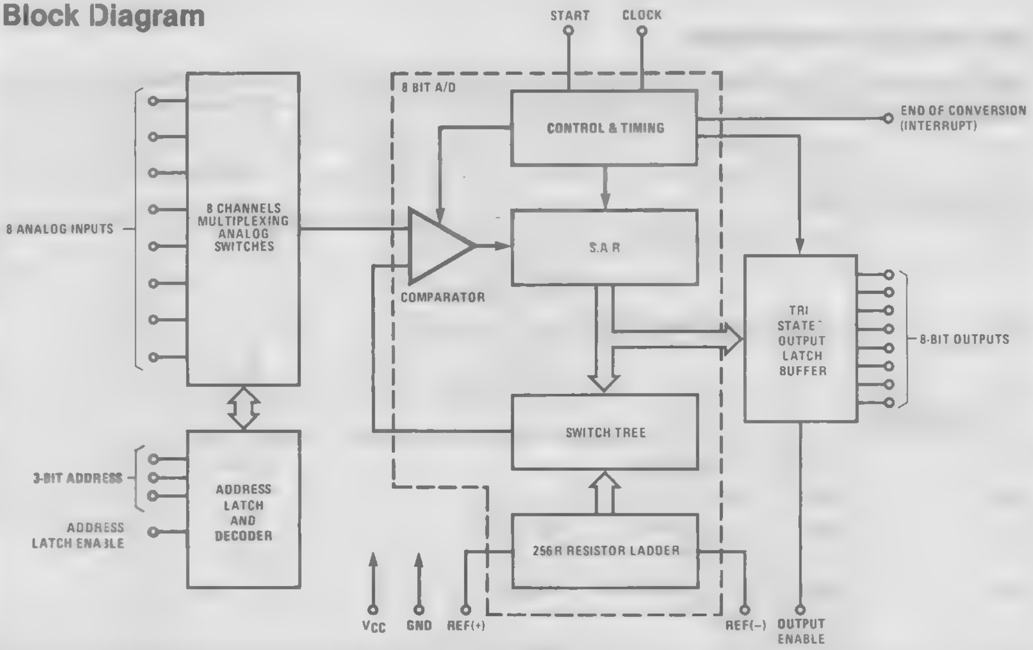
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output

Block Diagram



TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	$-0.3V$ to ($V_{CC}+0.3V$)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	$-0.3V$ to $+15V$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0808CJ	$-55°C \leq T_A \leq +125°C$
ADC0808CCJ, ADC0808CCN, ADC0809CCN	$-40°C \leq T_A \leq +85°C$
Range of V_{CC} (Note 1)	$4.5\ V_{DC}$ to $6.0\ V_{DC}$

Electrical Characteristics

Converter Specifications: $V_{CC} = 5\ V_{DC} = V_{REF(+)}$, $V_{REF(-)} = GND$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640$ kHz unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808 Total Unadjusted Error (Note 5)	25°C			± 1/2	LSB
		T_{MIN} to T_{MAX}			± 3/4	LSB
	ADC0809 Total Unadjusted Error (Note 5)	0°C to 70°C			± 1	LSB
		T_{MIN} to T_{MAX}			± 1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		$V_{CC}+0.10$	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	− 0.1	0		V
	Comparator Input Current	$f_c = 640$ kHz, (Note 6)	− 2	± 0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted

	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$,				
		$T_A = 25°C$		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$,				
		$T_A = 25°C$	− 200	− 10		nA
		T_{MIN} to T_{MAX}	− 1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN} = 0$	− 1.0			μA
I_{CC}	Supply Current	$f_{CLK} = 640$ kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	V_{CC}-0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = 5V$			3	µA
		$V_O = 0$	−3			µA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 µs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

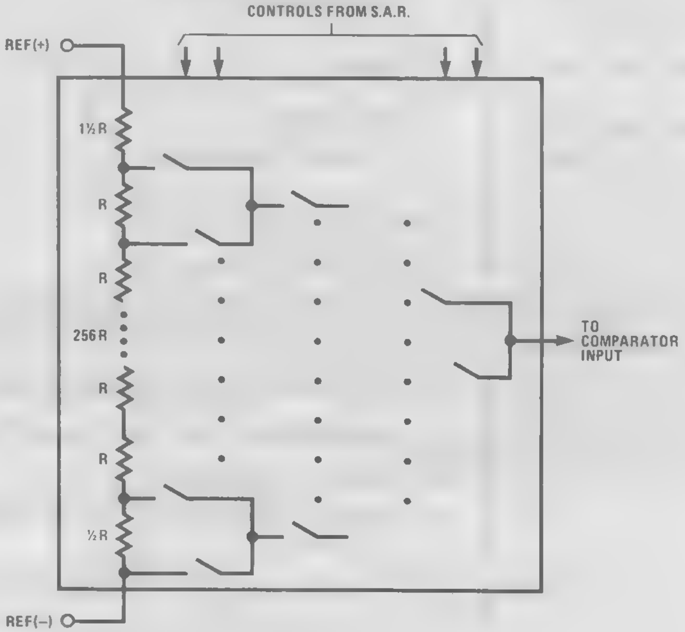


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

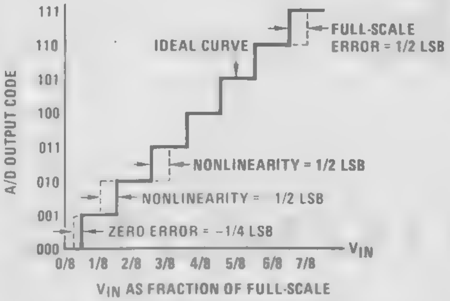


FIGURE 2. 3-Bit A/D Transfer Curve

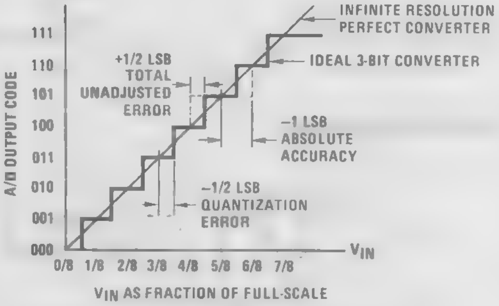


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

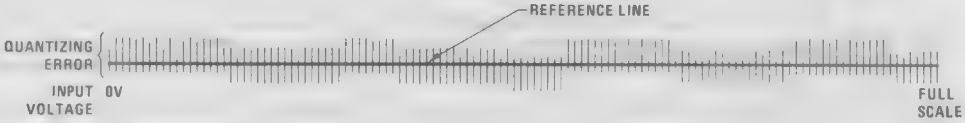
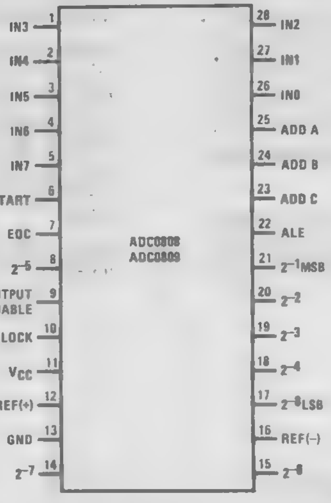


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram

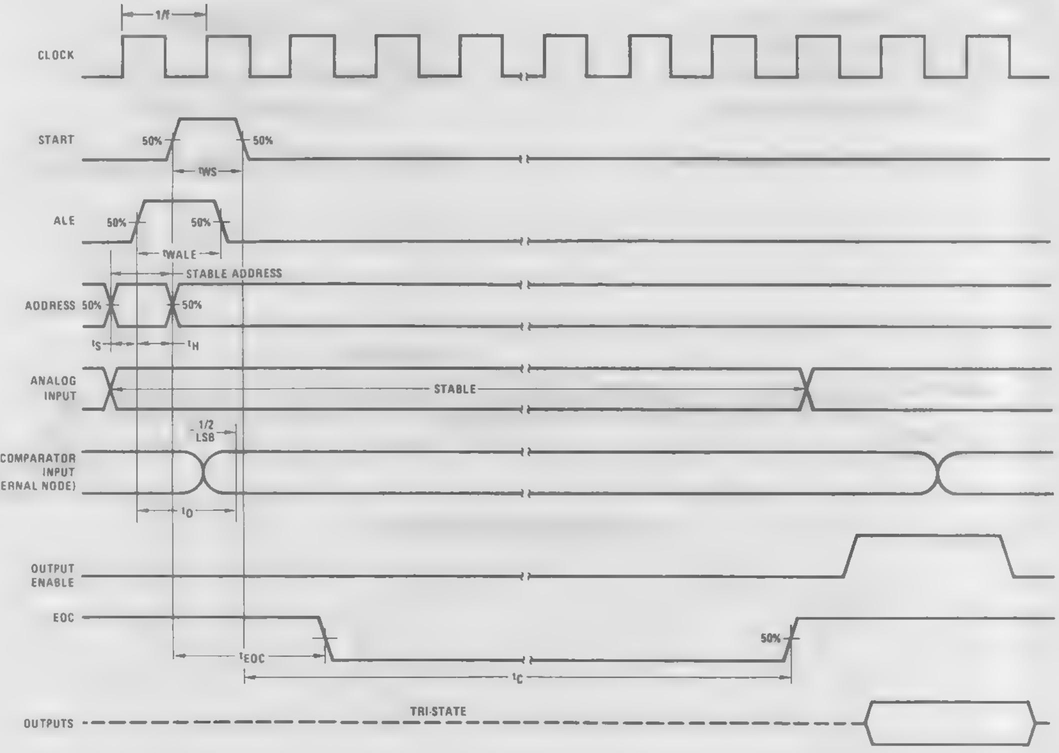


FIGURE [illegible]

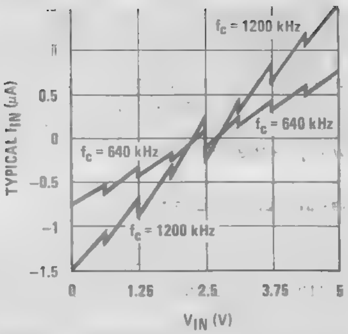


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

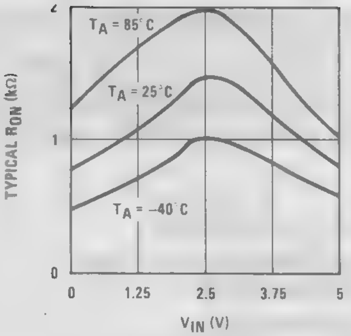


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

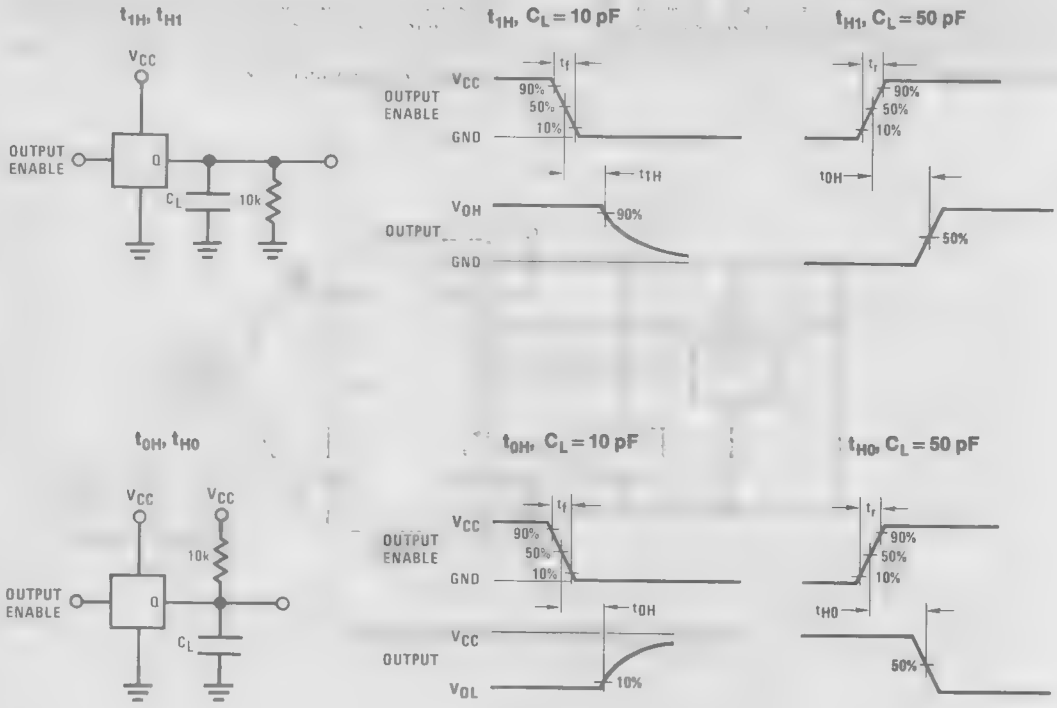


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \qquad (1)$$

V_{IN} = Input voltage into the ADC0808
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

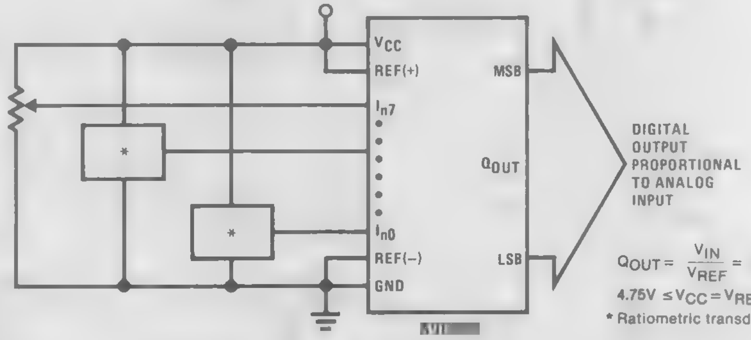
Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

* Ratiometric transducers

FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

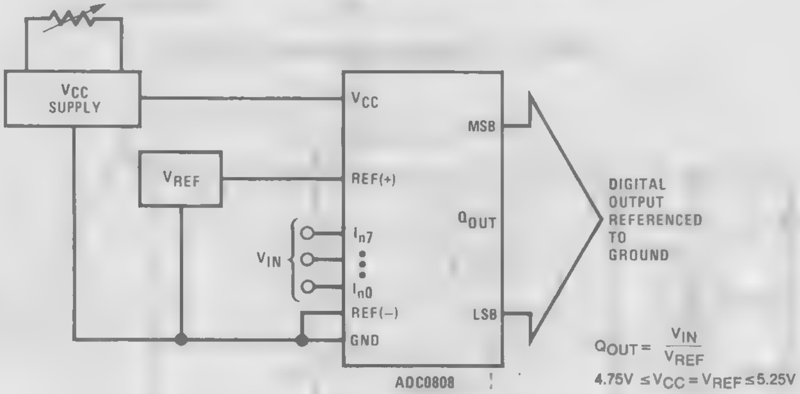


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

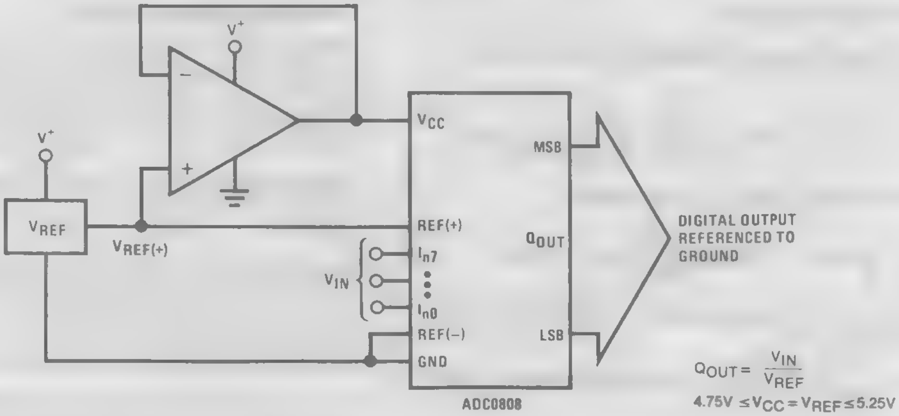


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

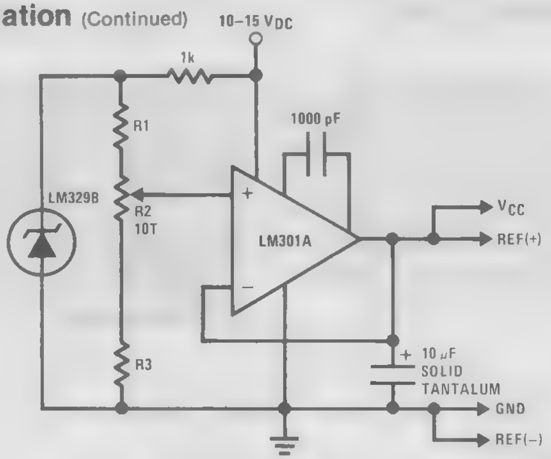


FIGURE 12. Typical Reference and Supply Circuit

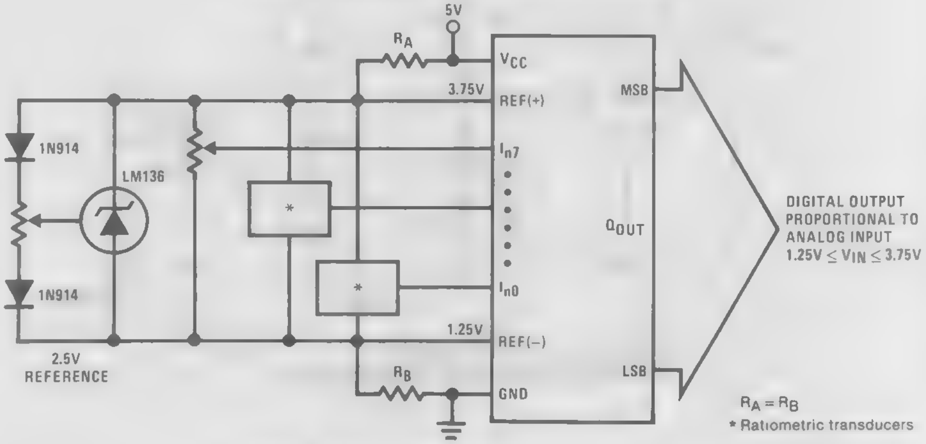


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \qquad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

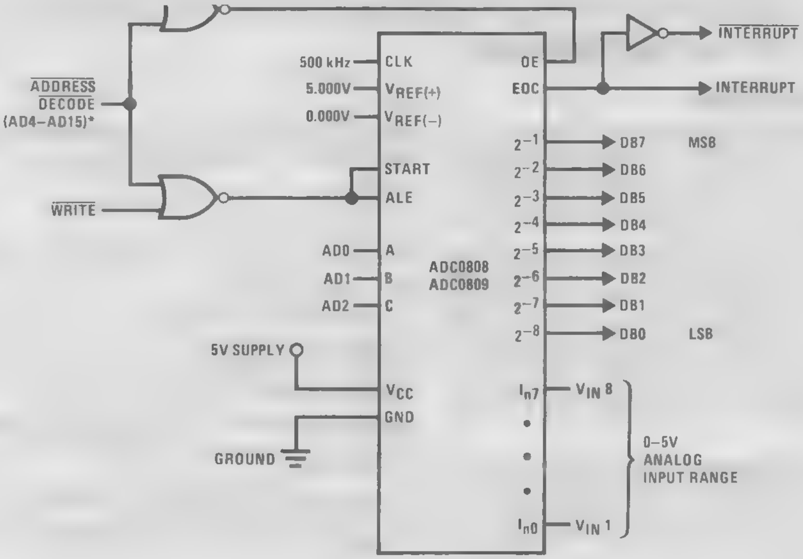
4.0 Analog Comparator Inputs

The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.



* Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·ϕ2·R/W	VMA·ϕ2·$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

National Semiconductor

ADC0816, ADC0817 8-Bit µP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

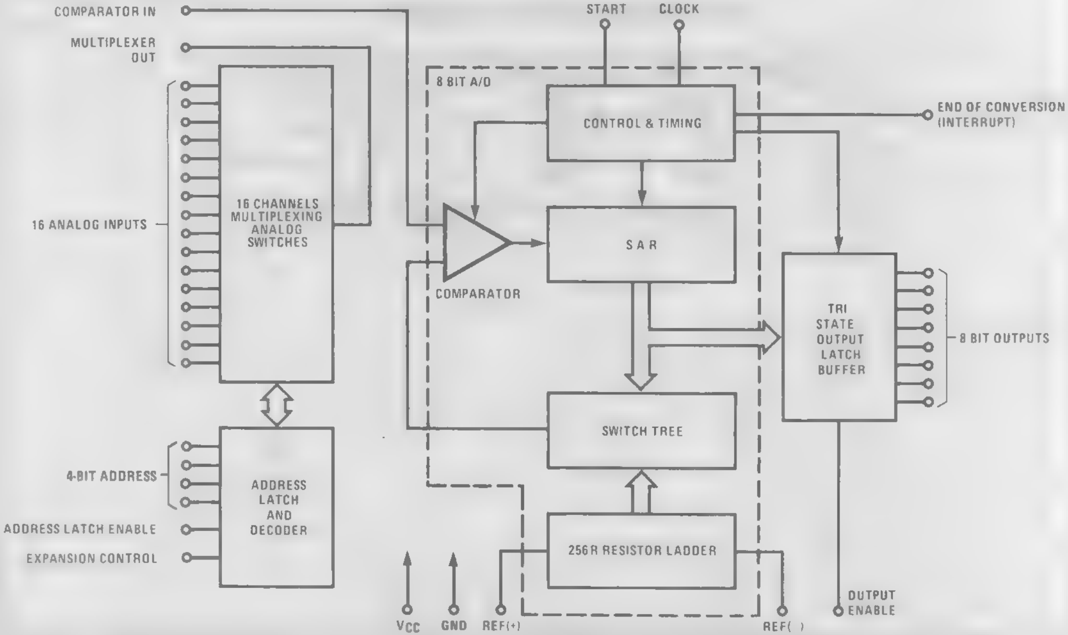
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 µs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	$-0.3V$ to $(V_{CC}+0.3V)$
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	$-0.3V$ to 15V
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	$-55°C \le T_A \le +125°C$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: $V_{CC} = 5\ V_{DC} = V_{REF(+)}$, $V_{REF(-)} = GND$, $V_{IN} = V_{COMPARATOR\ IN}$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	25°C			± 1/2	LSB
		T_{MIN} to T_{MAX}			± 3/4	LSB
	ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C			± 1	LSB
		T_{MIN} to T_{MAX}			± 1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		$V_{CC}+0.10$	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	− 0.1	0		V
	Comparator Input Current	$f_c = 640$ kHz, (Note 6)	− 2	± 0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN $4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) $T_A = 25°C$, $R_L = 10k$		1.5	3	kΩ
		$T_A = 85°C$			6	kΩ
		$T_A = 125°C$			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10k$		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$, $T_A = 25°C$		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$, $T_A = 25°C$	− 200			nA
		T_{MIN} to T_{MAX}	− 1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN} = 0$	− 1.0			μA
I_{CC}	Supply Current	$f_{CLK} = 640$ kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ — $4.5V \leqslant V_{CC} \leqslant 5.5V$, $-55°C \leqslant T_A \leqslant +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN — $4.75V \leqslant V_{CC} \leqslant 5.25V$, $-40°C \leqslant +85°C$ unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\mu A$, $T_A = 85°C$ $I_O = -300\mu A$, $T_A = 125°C$	$V_{CC} - 0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6mA$			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2mA$			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = V_{CC}$ $V_O = 0$	 −3.0		3.0 	μA μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE Outputs. (Note 7)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3.* None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13.*

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6).* See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

nel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

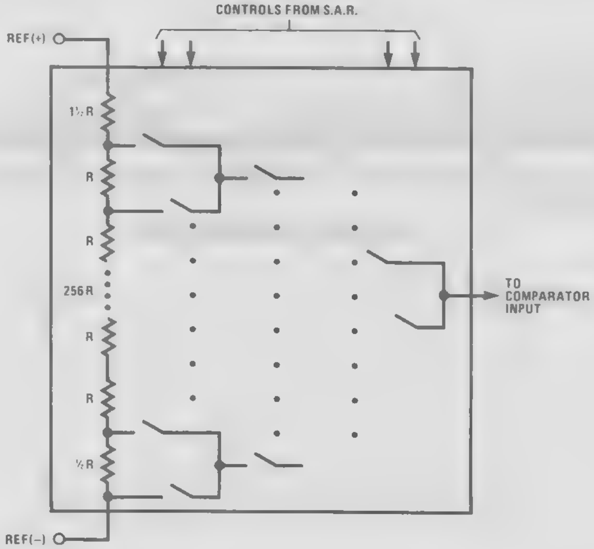


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

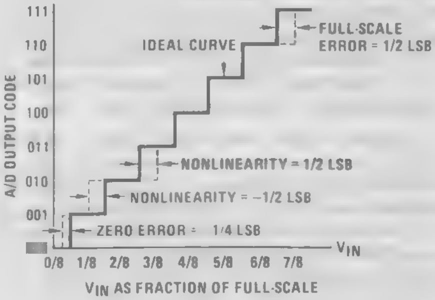


FIGURE 2. 3-Bit A/D Transfer Curve

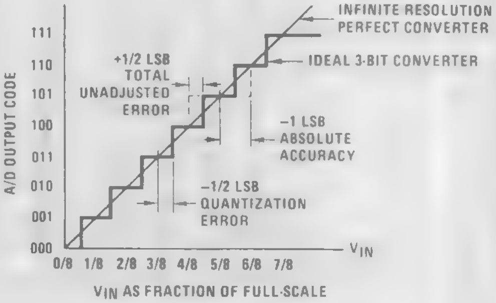


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

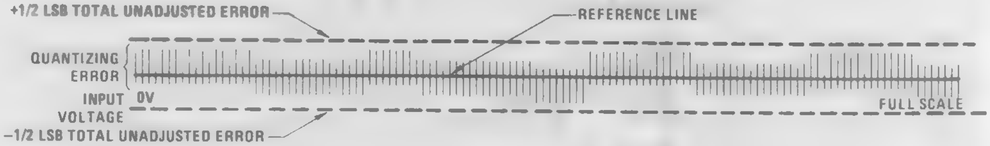
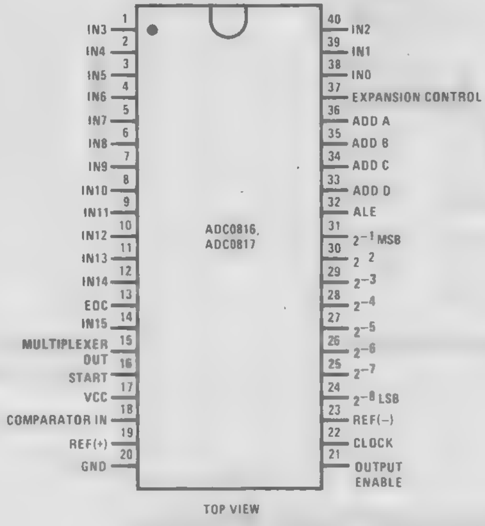


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



Timing Diagram

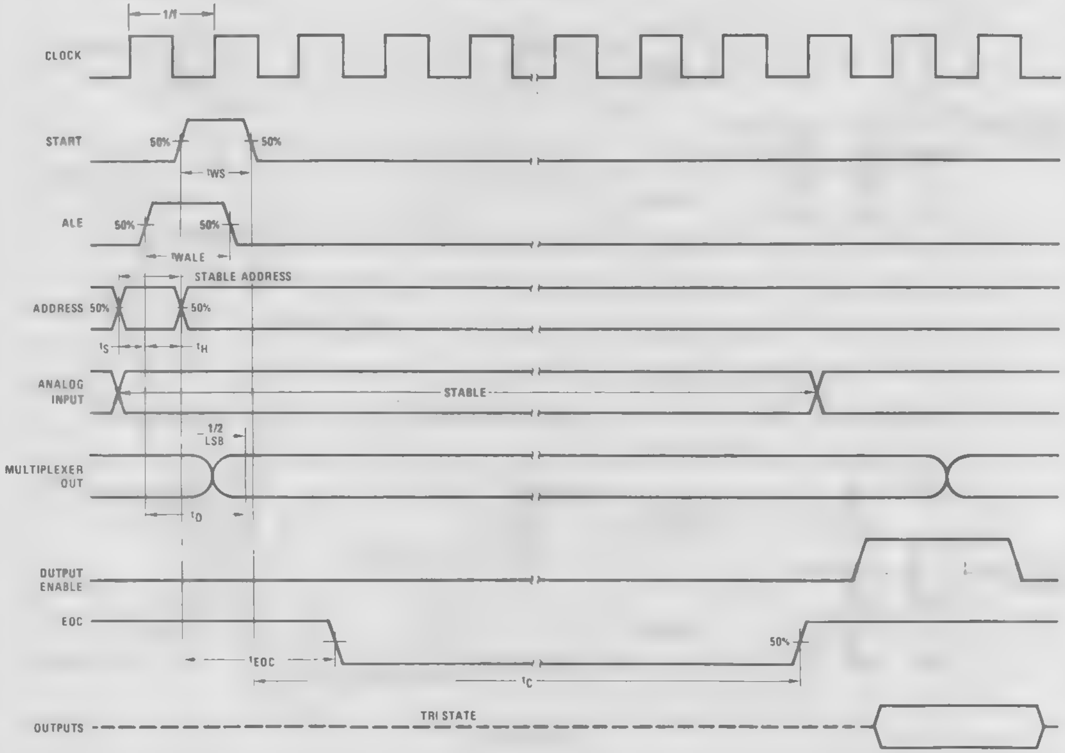


FIGURE 5

Typical Performance Characteristics

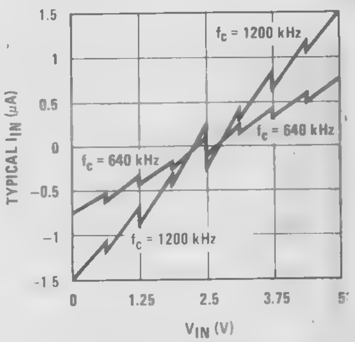


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

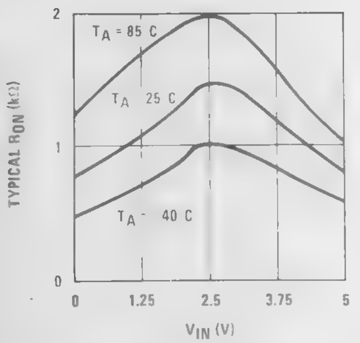


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

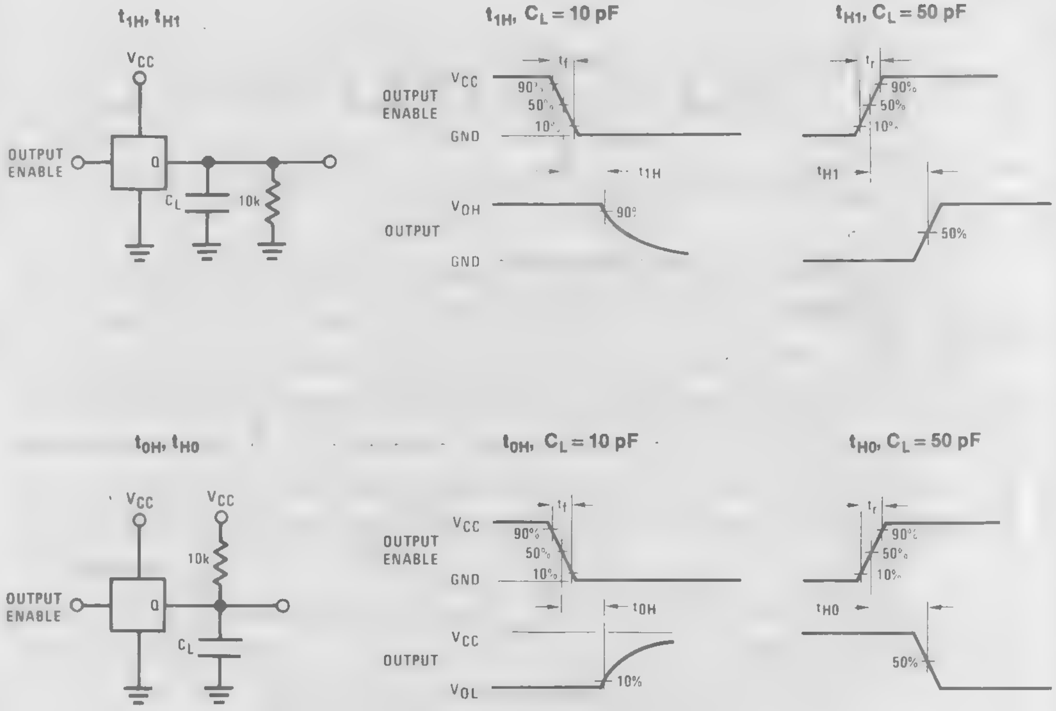


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \qquad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9).*

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

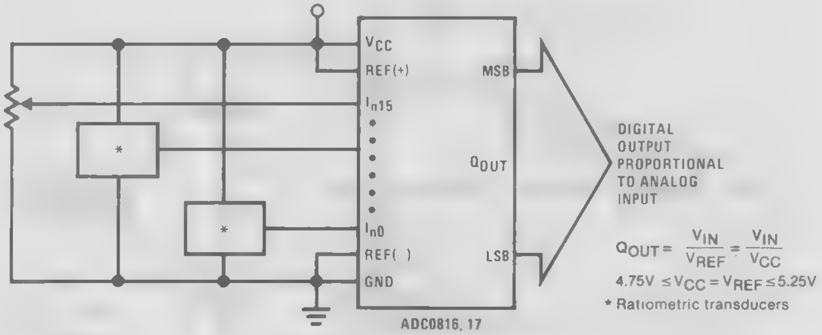
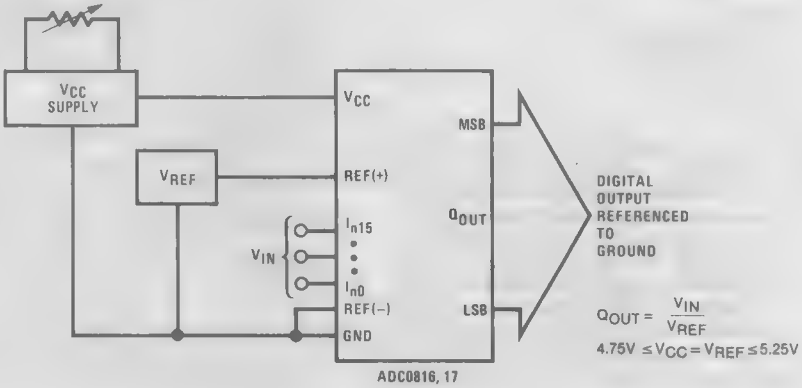

V_CC
REF(+)
MSB
I_n15
Q_OUT
I_n0
REF( )
LSB
GND
*
*
ADC0816, 17
DIGITAL OUTPUT PROPORTIONAL TO ANALOG INPUT
Q_OUT = V_IN / V_REF = V_IN / V_CC
4.75V ≤ V_CC = V_REF ≤ 5.25V
* Ratiometric transducers

FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

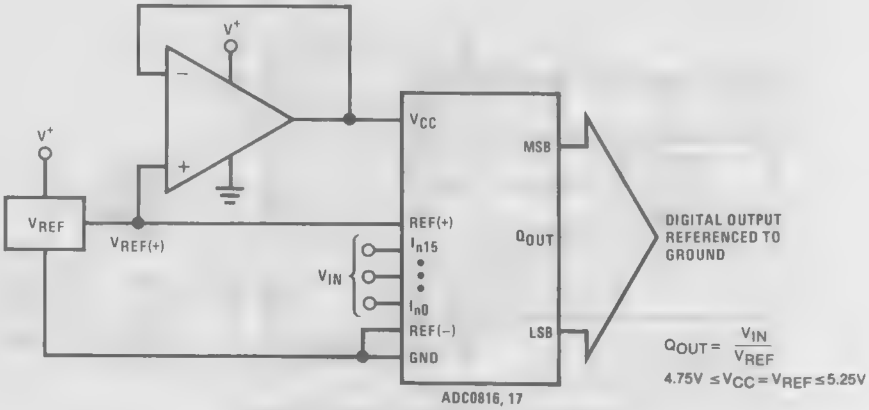
The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.



V_{CC} SUPPLY
V_{REF}
V_{CC}
MSB
REF(+)
Q_{OUT}
I_{n15}
V_{IN}
I_{n0}
REF(−)
LSB
GND
ADC0816, 17
DIGITAL OUTPUT REFERENCED TO GROUND
$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$
$4.75V \le V_{CC} = V_{REF} \le 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



V^+
−
+
V^+
V_{REF}
$V_{REF(+)}$
V_{CC}
MSB
REF(+)
I_{n15}
Q_{OUT}
V_{IN}
I_{n0}
REF(−)
LSB
GND
ADC0816, 17
DIGITAL OUTPUT REFERENCED TO GROUND
$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$
$4.75V \le V_{CC} = V_{REF} \le 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

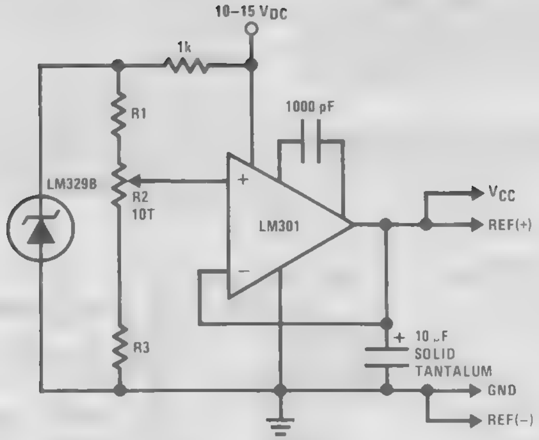
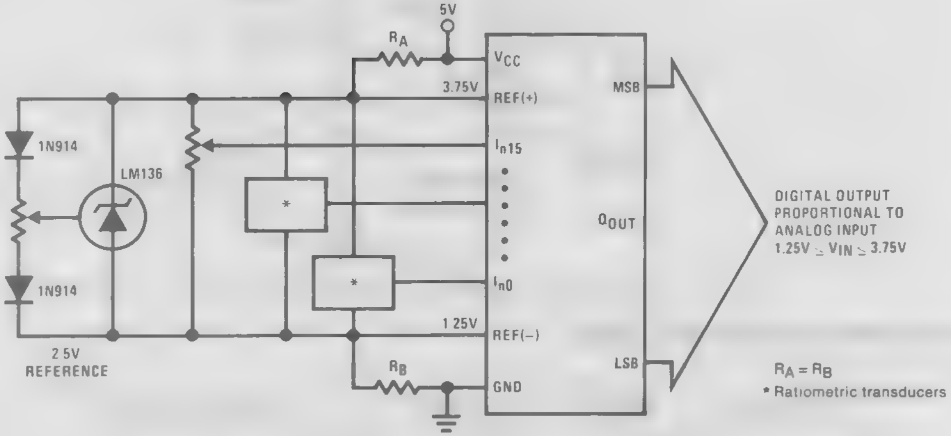


FIGURE 12. Typical Reference and Supply Circuit



$R_A = R_B$

* Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \qquad (4)$$

where: V_{IN} = Voltage at comparator input

$V_{REF(+)}$ = Voltage at Ref(+)

$V_{REF(-)}$ = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 Analog Comparator Inputs

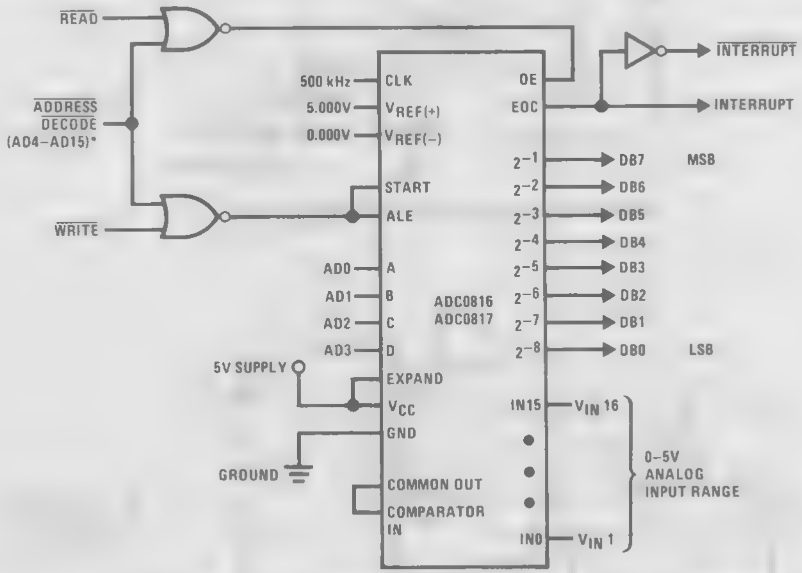
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6.*

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·ϕ2·R/W	VMA·ϕ2·$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	±1/2 Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	±1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

National Semiconductor

ADC3511
3 1/2-Digit Microprocessor Compatible A/D Converter
ADC3711
3 3/4-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937-1, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

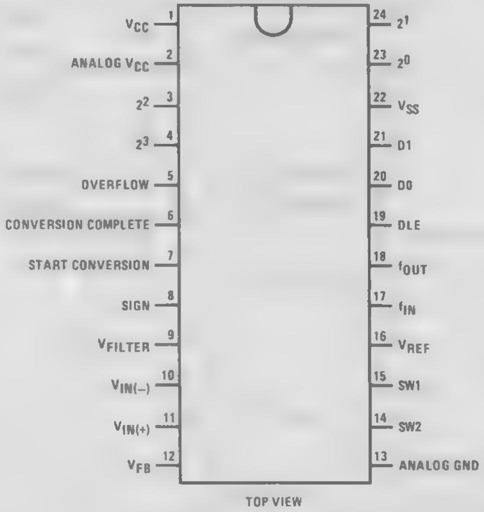
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range (T_A)	$-40^\circ C$ to $+85^\circ C$
Package Dissipation at $T_A = 25^\circ C$	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 seconds)	$300^\circ C$

DC Electrical Characteristics ADC3511CC, ADC3711CC

$4.75V \leq V_{CC} \leq 5.25V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		$V_{CC}-0.6$			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except $2^0, 2^1, 2^2, 2^3$)	$I_O = 360\mu A$	$V_{CC}-0.4$			V
$V_{OUT(1)}$	Logical "1" Output Voltage ($2^0, 2^1, 2^2, 2^3$)	$I_O = 360\mu A$	$V_{CC}-1.0$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	$V_{IN} = V_{CC}$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	$V_{IN} = 0V$	1.0	−0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

$V_{CC} = 5V$; $T_A = 25^\circ C$; $C_L = 50$ pF; $t_r = t_f = 20$ ns; unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC ADC3711CC	$f_{IN}/64{,}512$ $f_{IN}/129{,}024$			conversions/sec conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to $2^0, 2^1, 2^2, 2^3$	DLE = 0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to $2^0, 2^1, 2^2, 2^3$			2.0	5.0	μs
t_{SET-UP}	Set-Up Time D0, D1, to DLE	$t_{HOLD} = 0$ ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

	Non-Linearity	V_{IN} = 0–2V Full Scale V_{IN} = 0–200 mV Full Scale	−0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		−1		+0	Counts
	Offset Error	V_{IN} = 0V	−0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		−0		+0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	T_A = 25°C	−5	±1	+5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

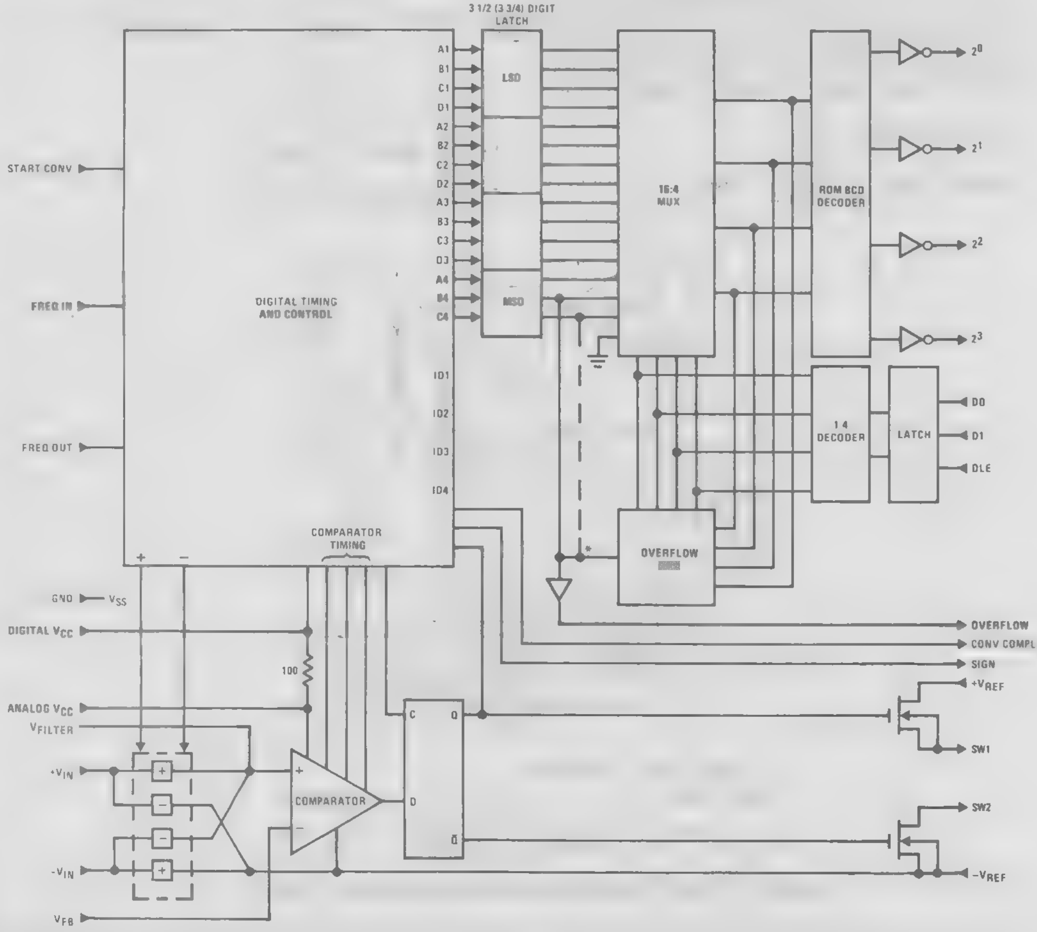
Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = 1/2 count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Block Diagram

ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D)



Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

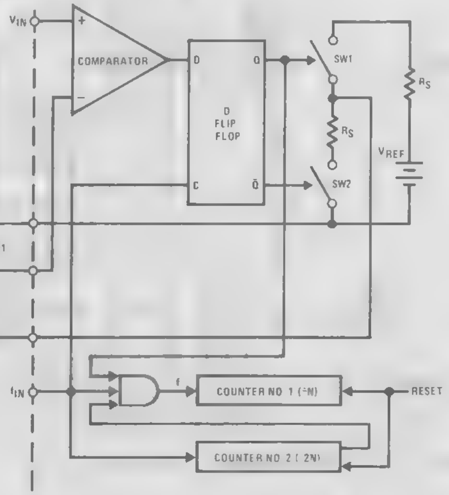
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



$$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$$

$$f = \text{(duty cycle)} \times f_{IN}$$

$$\text{Count in counter no. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 x $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$ on the ADC3511, or 128 x $1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ (129,024 x $1/f_{IN}$ for the ADC3711) and the minimum time is 256 x $1/f_{IN}$ (512 x $1/f_{IN}$ for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

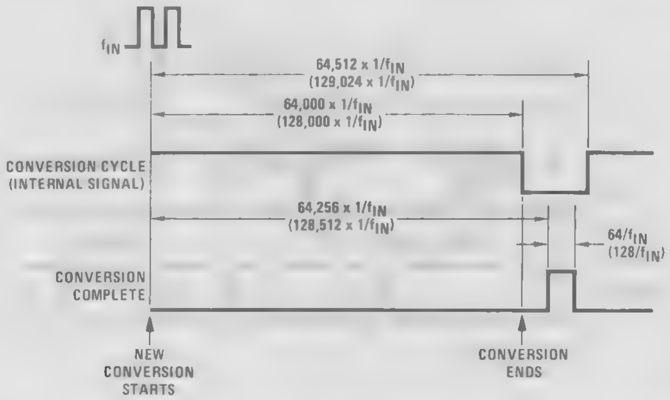


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

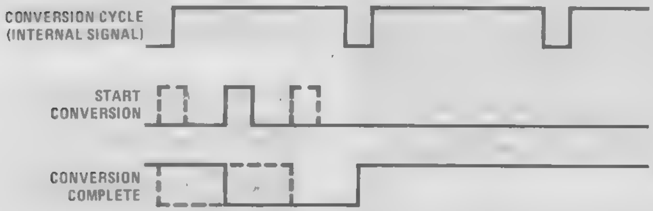


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = Low logic level
H = High logic level
X = Irrelevant logic level

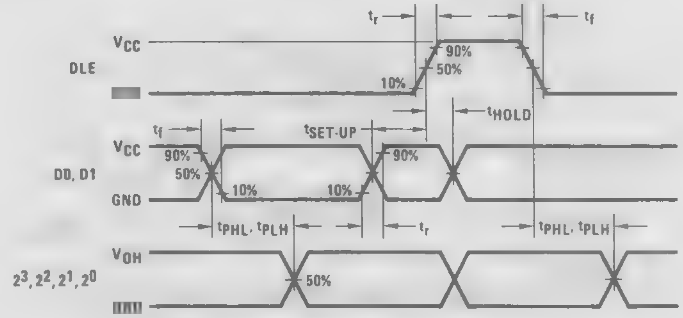
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



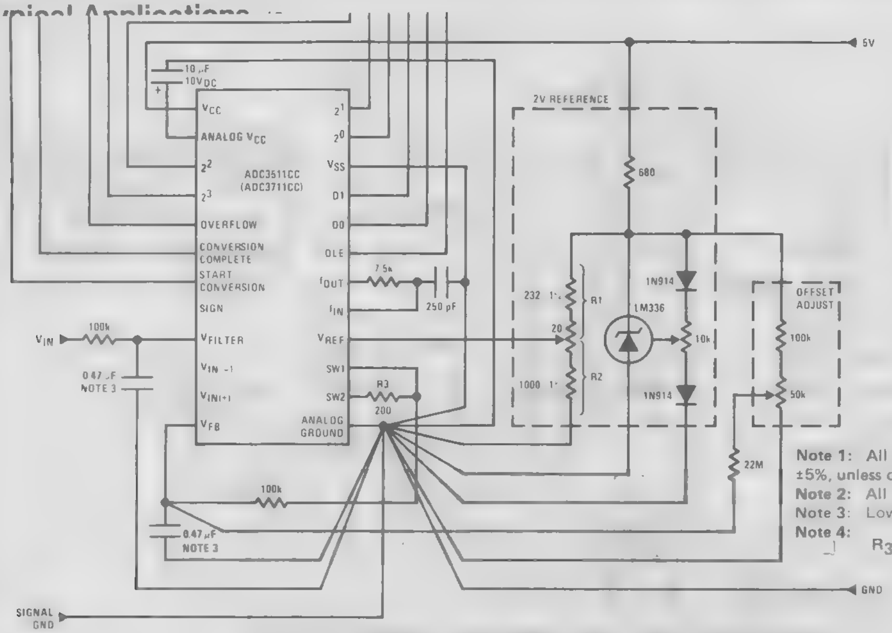
Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6*.

Figures 5 and 6 show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

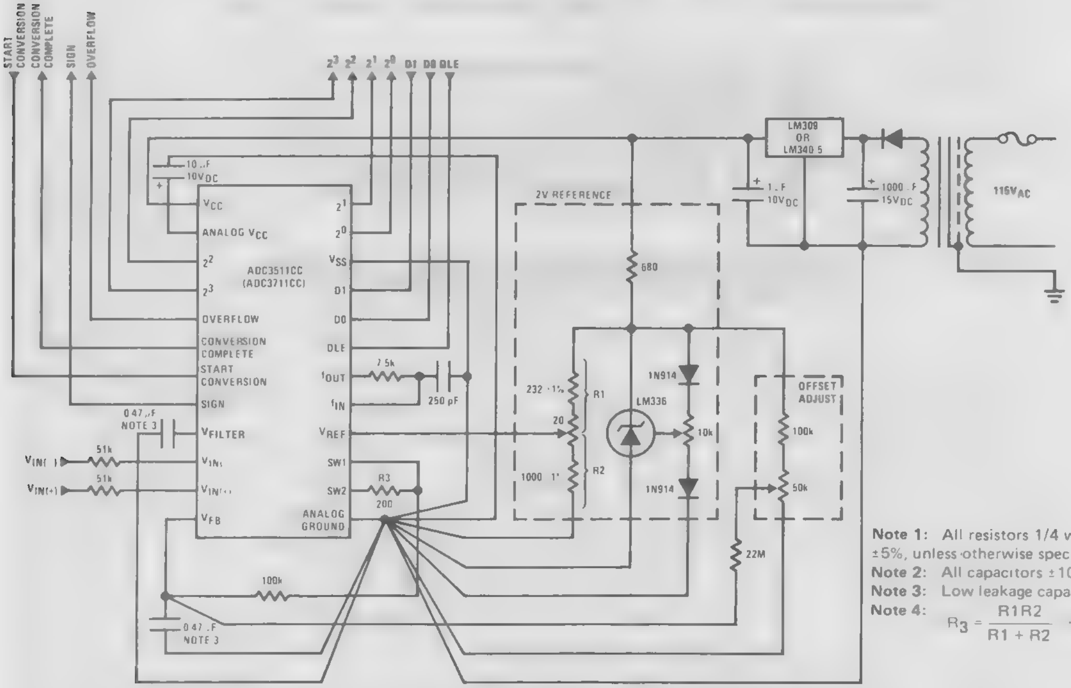
The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error (1.0×10^{-9}A x 100 kΩ = 0.1 mV). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

Typical Applications



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4: $R_3 = \frac{R1R2}{R1 + R2}$ ±25Ω.

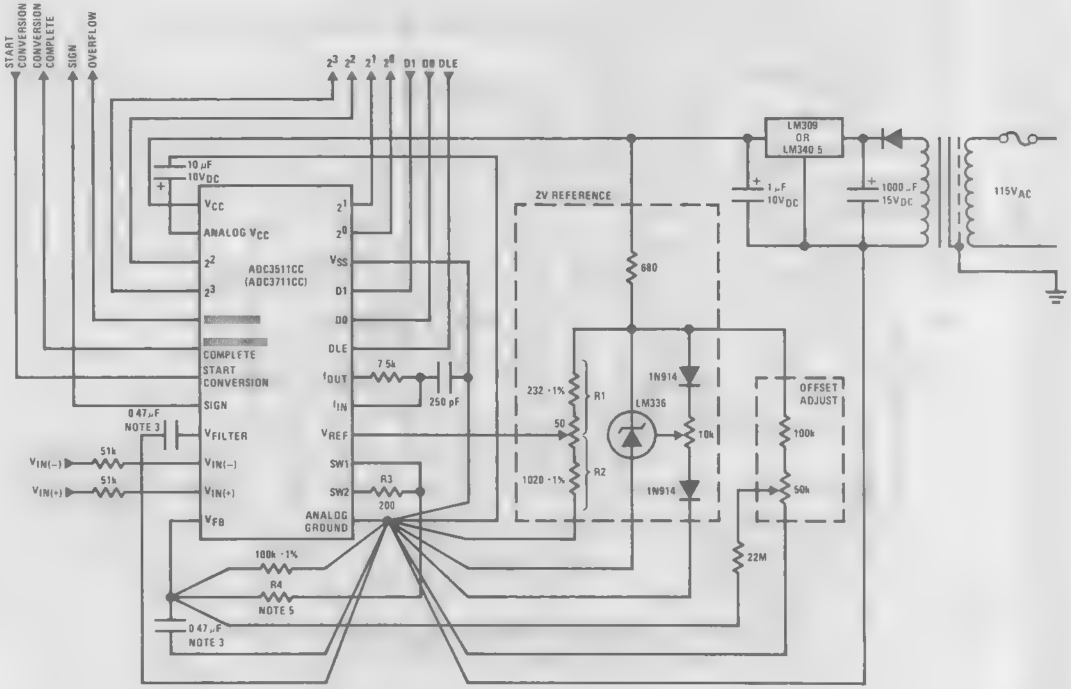
FIGURE 4. 3 1/2-Digit A/D; +1999 Counts, +2.000 Volts Full Scale
(3 3/4-Digit A/D; +3999 Counts, +2.000 Volts Full Scale)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4: $R_3 = \frac{R1R2}{R1 + R2}$ ±25Ω.

FIGURE 5. 3 1/2-Digit A/D; ±1999 Counts, ±2.000 Volts Full Scale
(3 3/4-Digit A/D; ±3999 Counts, ±2.000 Volts Full Scale)

Typical Applications (Continued)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.

Note 2: All capacitors ±10%.

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega$.

Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.
R4 = 400k ±1% for the ADC3711CC, 400.0 mV Full-Scale.

FIGURE 6. 3 1/2-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale (3 3/4-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)

National Semiconductor

ADD3501 3½ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3501 (MM74C935-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

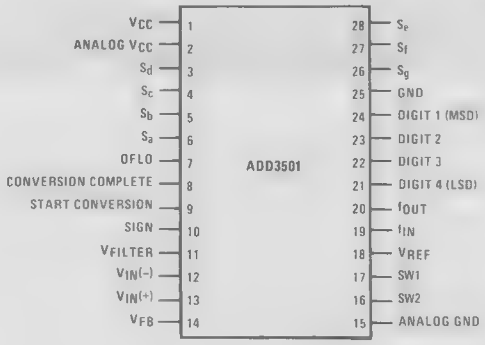
Features

- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed — 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at $T_A = 25°C$	800 mW
derate at $\theta_{JA(MAX)} = 125°C/Watt$ above $T_A = 25°C$	
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics $4.75V \leqslant V_{CC} \leqslant 5.25V$, $-40°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.

ADD3501

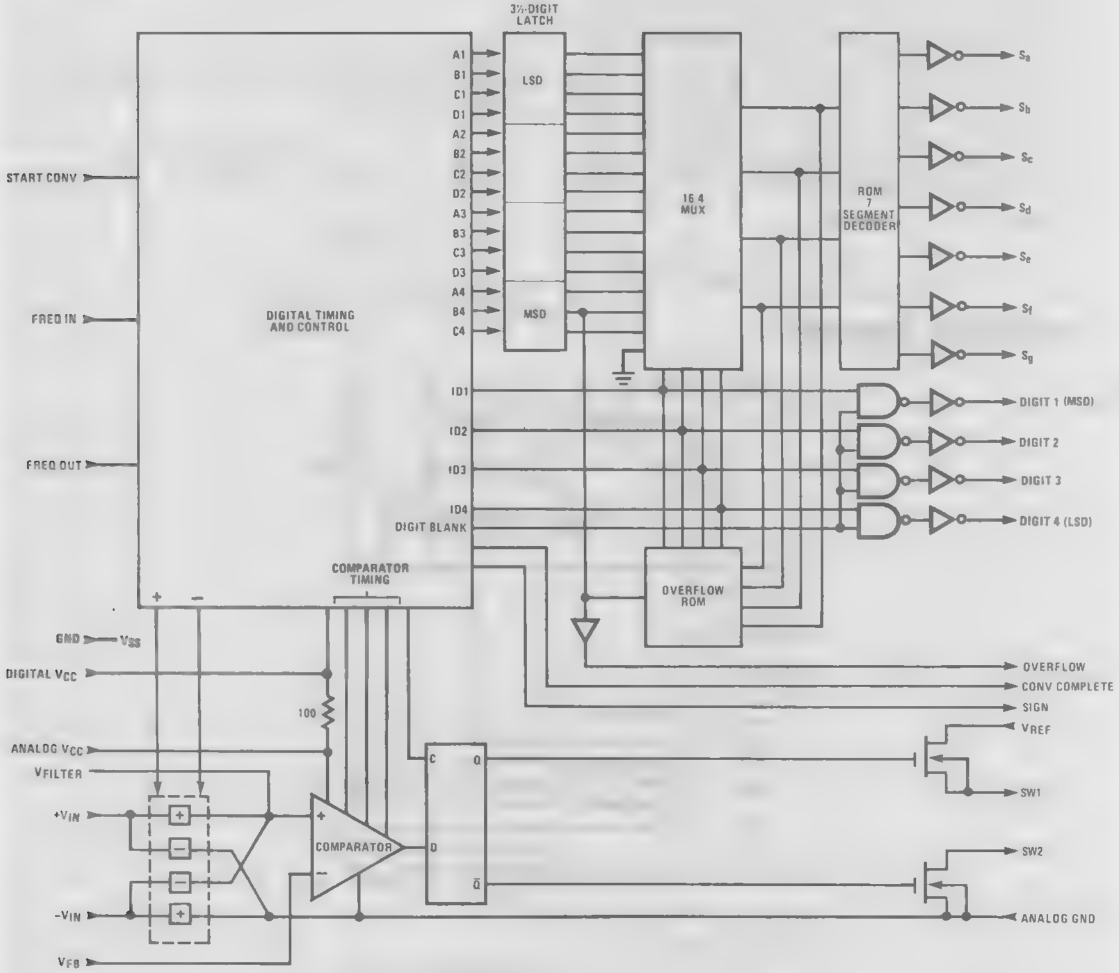
PARAMETER		CONDITIONS	MIN	TYP (2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs except Digit Outputs)	$I_O = 1.1\,mA$			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7\,mA$			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50\,mA$ @ $T_J = 25°C$ $V_{CC} = 5V$ $I_O = 30\,mA$ @ $T_J = 100°C$	$V_{CC} - 1.6$ $V_{CC} - 1.6$	$V_{CC} - 1.3$ $V_{CC} - 1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs except Segment Outputs)	$I_O = 500\mu A$ (Digit Outputs) $I_O = 360\mu A$ (Conv. Complete, +/−, Oflo Outputs)	$V_{CC} - 0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 1.5V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0V$	−1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/64{,}512$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/256$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for $T_A = 25°C$.

	V_{IN} = 0 - 200mV Full Scale				full scale
Quantization Error		−1		+0	counts
Offset Error, V_{IN} = 0V		−0.5	+1.5	+3	mV
Rollover Error		−0		+0	counts
Analog Input Current ($V_{IN}+$, $V_{IN}-$)	T_A = 25°C	−5	+0.5	+5	nA

block diagram



ADD3501 3½-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and Q outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\left(\frac{T_{ON}}{T_{ON} + T_{OFF}}\right) = V_{REF}\,(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\,(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\,(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

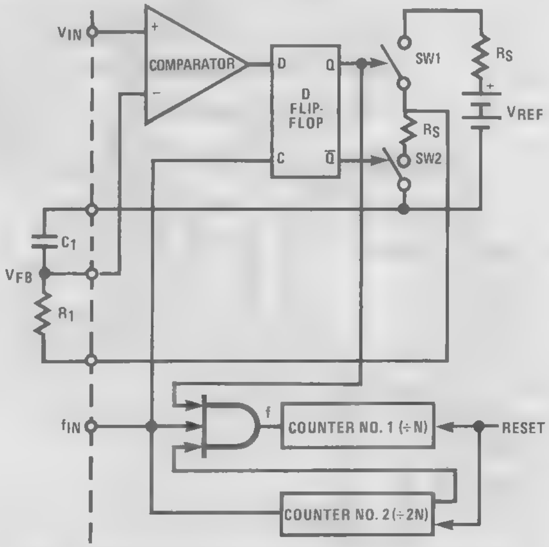
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3501, N = 2000.

Schematic Diagram



$$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$$

$$f = (\text{duty cycle}) \times f_{IN}$$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

general information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 64,512 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADD3501 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ and the minimum time is 256 x $1/f_{IN}$.

Timing Waveforms

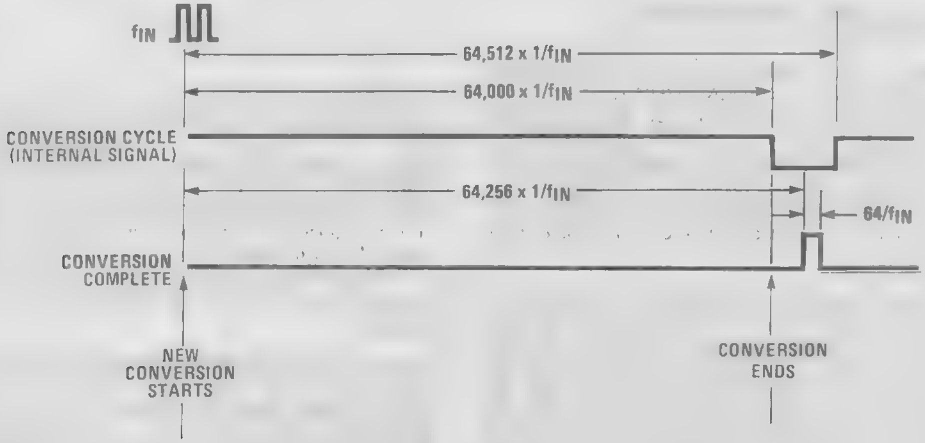


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

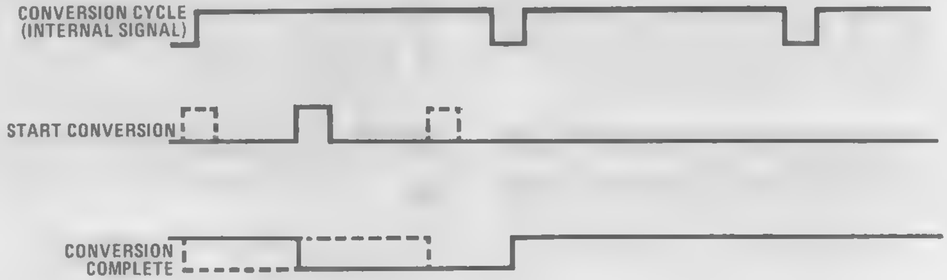


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3501 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3501 to minimize these problems but poor printed circuit layout can negate these features.

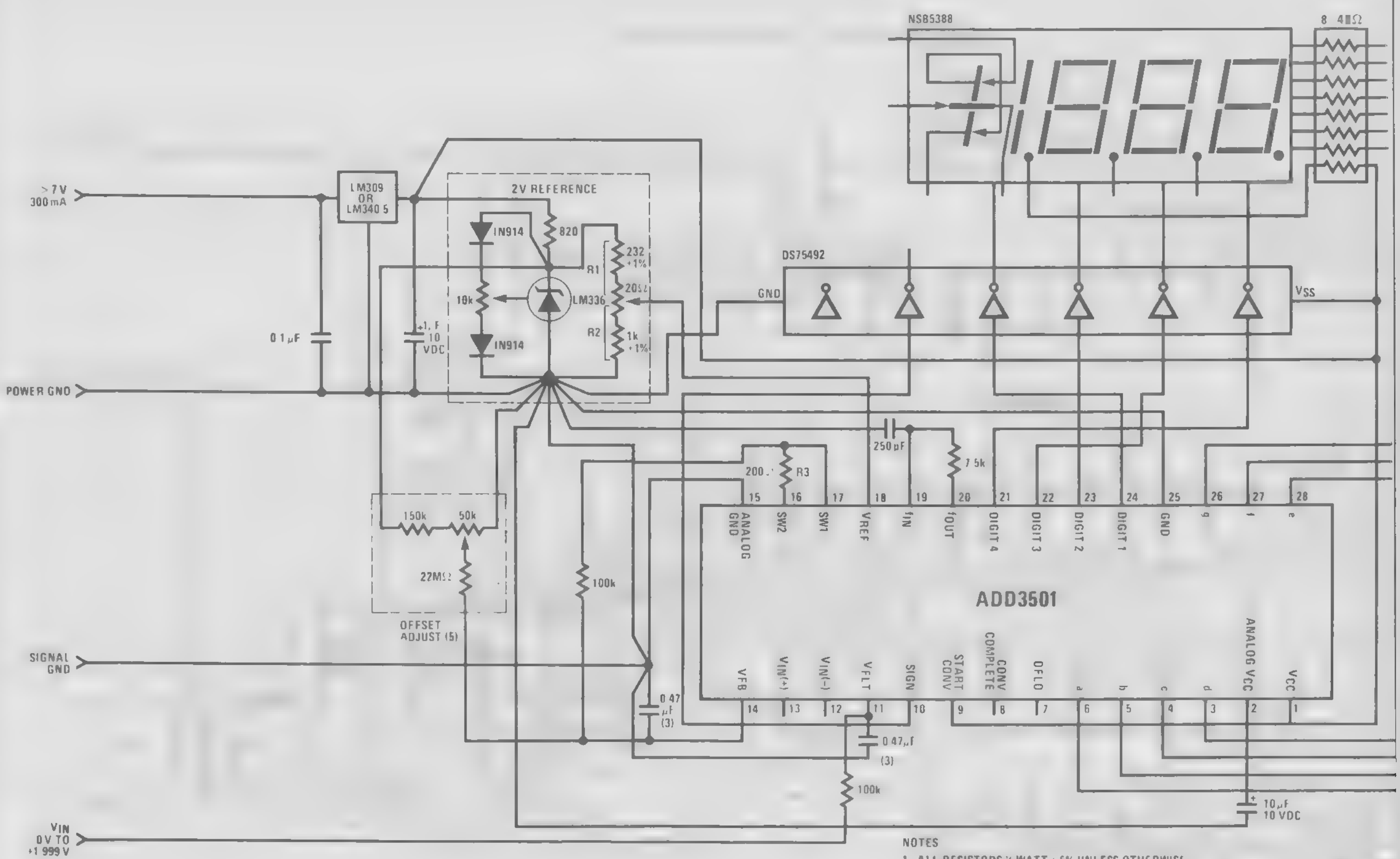
Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators both function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0V to 1.999V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 6.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

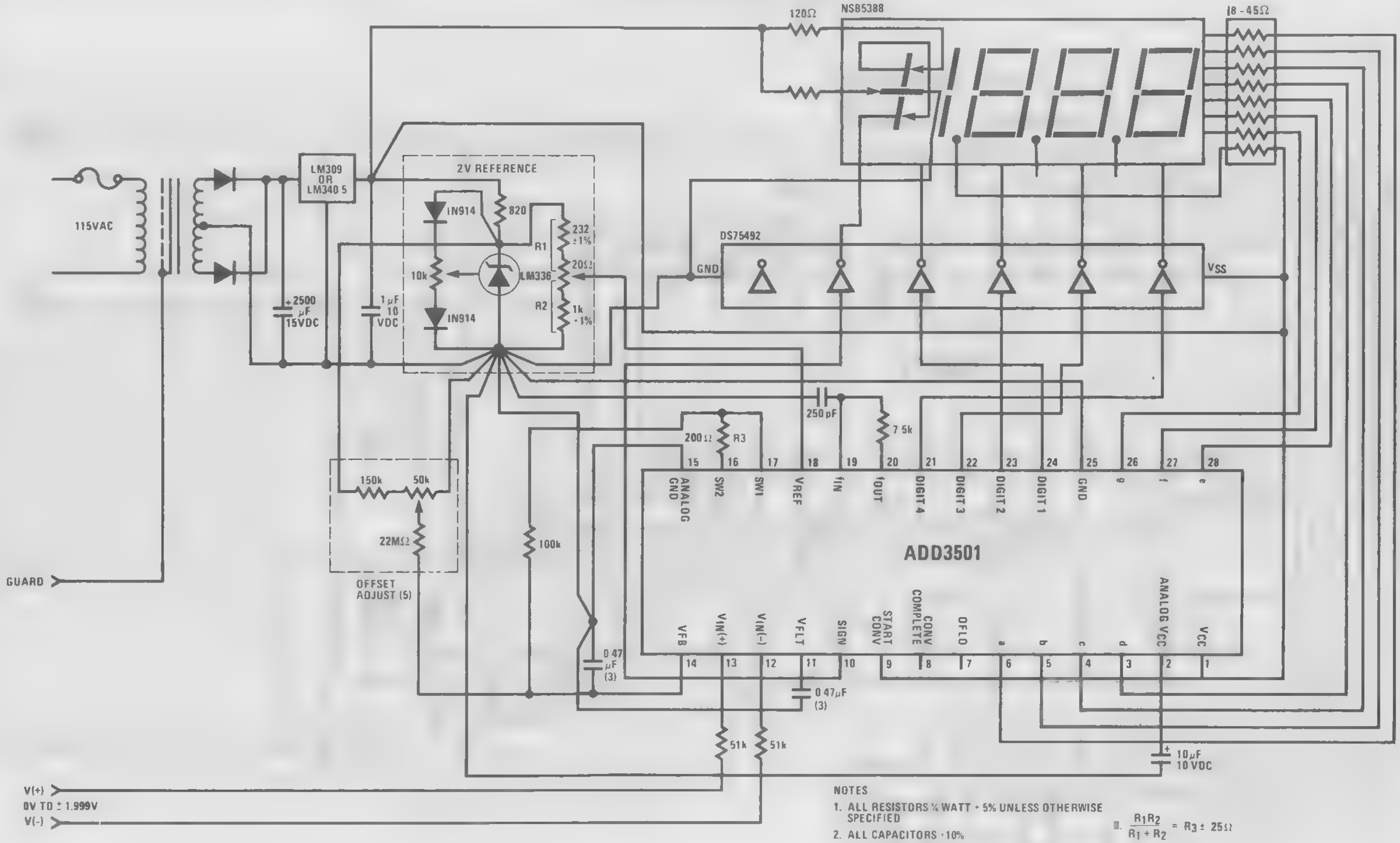
The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0nA of leakage current will cause 0.1mV error ($1.0 \times 10^{-9}A \times 100k\Omega = 0.1mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 4. 3½-Digit DPM, +1.999 Volts Full Scale



NOTES

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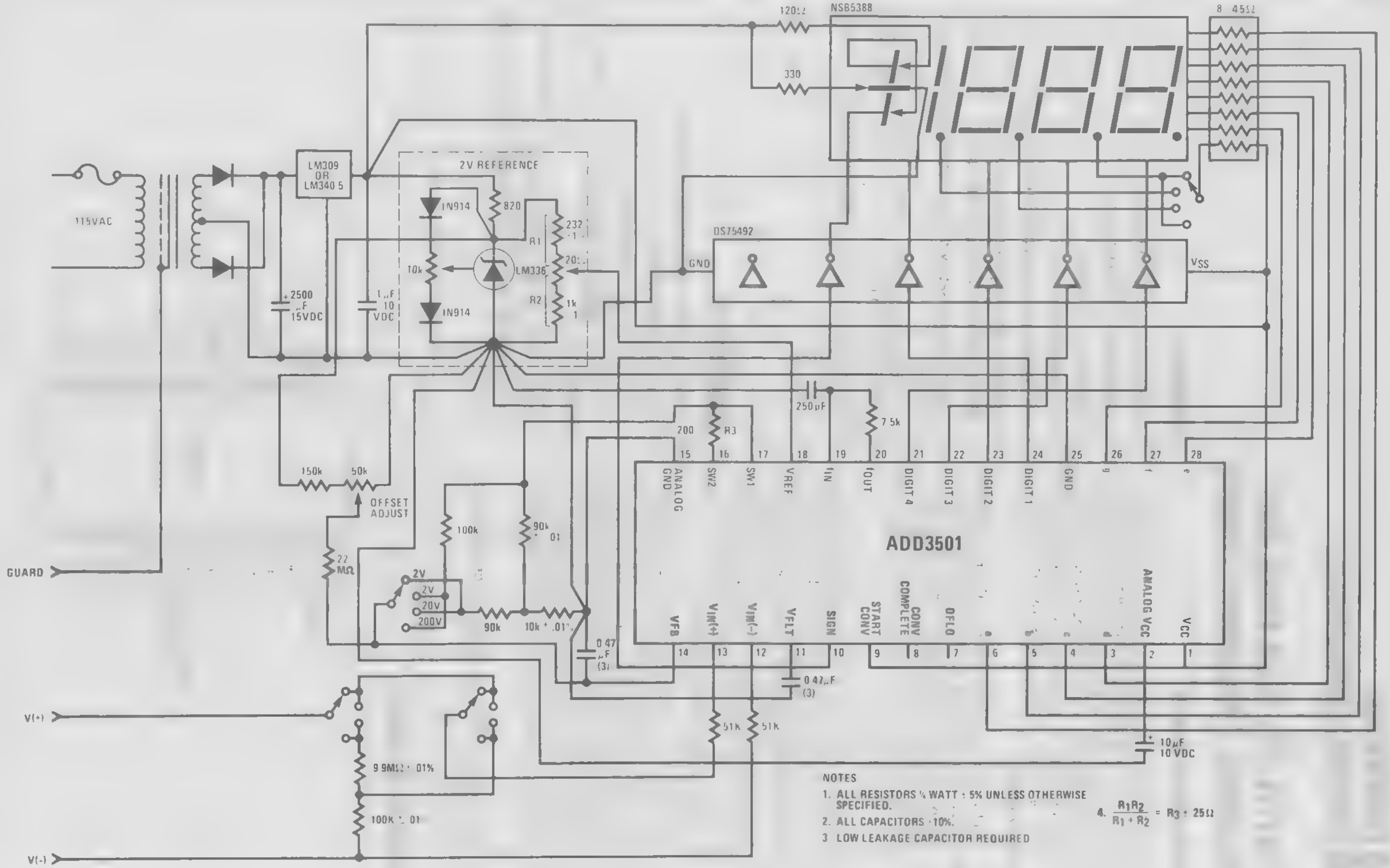
3. LOW LEAKAGE CAPACITOR REQUIRED

[illegible]. $\frac{R_1R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 5. 3½-Digit DPM, ±1.999 Volts Full Scale



NOTES

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ± 10%.
3. LOW LEAKAGE CAPACITOR REQUIRED
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 6. 3½-Digit DVM, Four Decade, ±0.2 V, ±2 V, ±20 V and ±200 V Full Scale

National Semiconductor

ADD3701 3¾ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5 V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

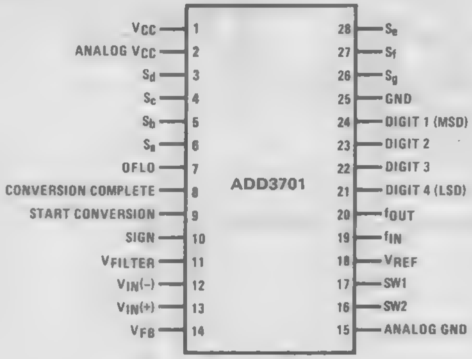
Features

- Operates from single 5 V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram



Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics ADD3701

$4.75V \leqslant V_{CC} \leqslant 5.25V$, $-40°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.

Parameter		Conditions	Min	Typ[2]	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs Except Digit Outputs)	$I_O = 1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50$ mA @ $T_J = 25°C$ $V_{CC} = 5V$ $I_O = 30$ mA @ $T_J = 100°C$	$V_{CC} - 1.6$ $V_{CC} - 1.6$	$V_{CC} - 1.3$ $V_{CC} - 1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	$I_O = 500\,\mu A$ (Digit Outputs) $I_O = 360\,\mu A$ (Conv. Complete, +/−, OFLO Outputs)	$V_{CC} - 0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0\,V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 15\,V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0\,V$	−1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/129{,}024$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/512$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32\,f_{MUX})$		seconds
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for $T_A = 25°$ C.

Note 3: Full scale = 4000 counts; therefore 0.025% of full scale = 1 count and 0.05% of full scale = 2 counts.

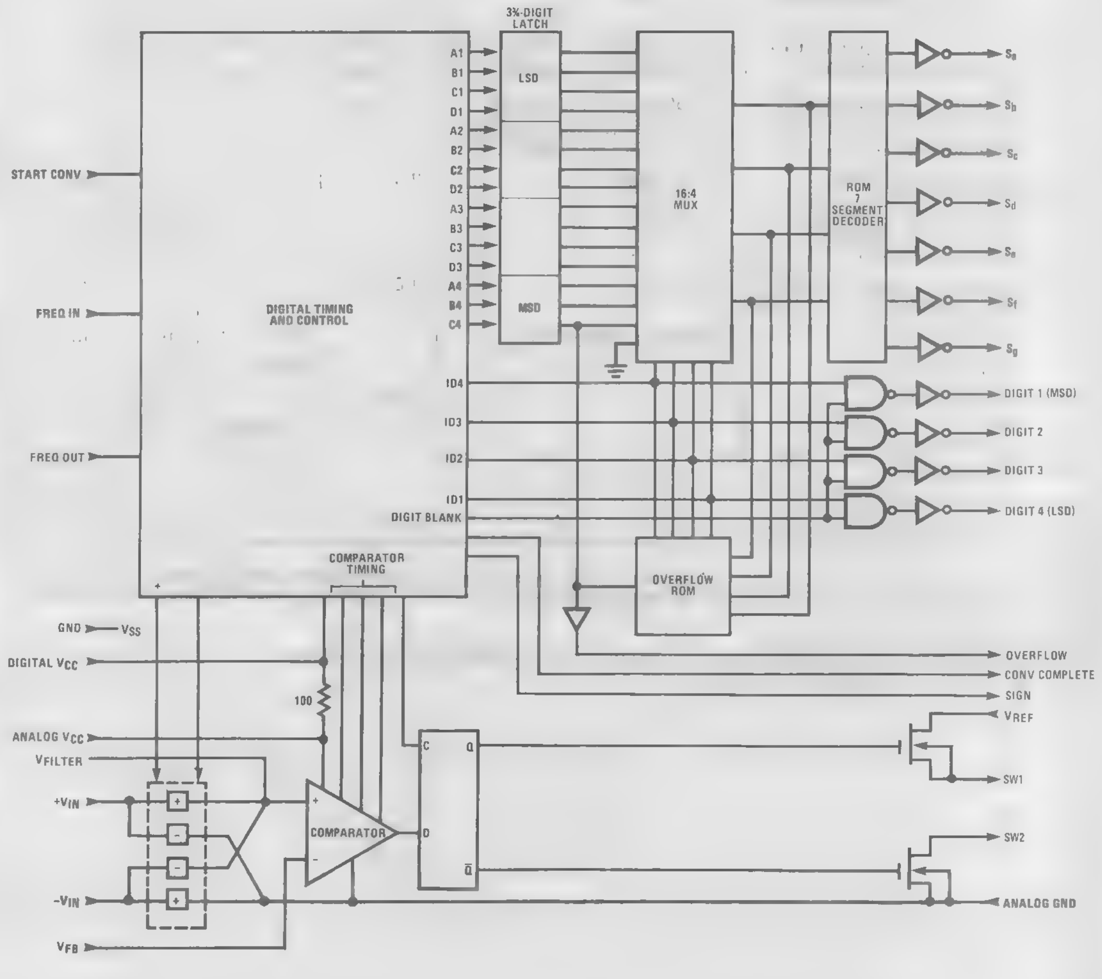
Note 4: For 2.000 Volts full scale, 1 mV = 2 counts.

Electrical Characteristics ADD3701

t_C = 2.5 conversions/second, $0°C \leq T_A \leq +70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ[2]	Max	Units
Non-Linearity of Output Reading	V_{IN} = 0–2 V Full Scale V_{IN} = 0–200 mV Full Scale	−0.05	±0.025	+0.05	% full scale (Note 3)
Quantization Error		−1		+0	counts
Offset Error, V_{IN} = 0 V		−0.5	+1.5	+3	mV (Note 4)
Rollover Error		−0		+0	counts
Analog Input Current (V_{IN^+}, V_{IN^-})	T_A = 25°C	−5	±1	+5	nA

Block Diagram



ADD3701 3¾-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0\,V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and Q outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0 V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0 V. At this time V_{FB} will start discharging toward 0 V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0 V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF}\ (\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\ (\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\ (\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

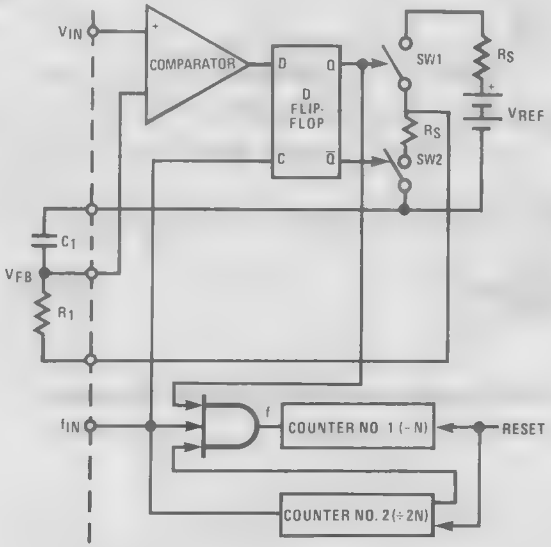
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3701 N = 4000.

Schematic Diagram



$$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$$

$$f = (\text{duty cycle}) \times f_{IN}$$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 129,024 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 128 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADD3701 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 129,024 x $1/f_{IN}$ and the minimum time is 512 x $1/f_{IN}$.

Timing Waveforms

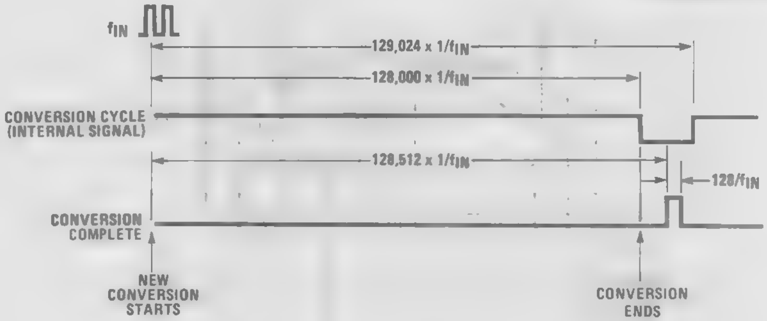


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

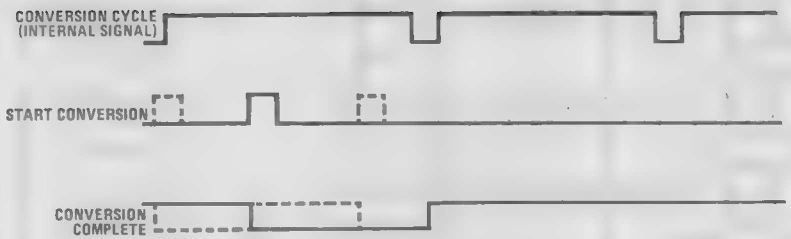


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3701 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3701 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

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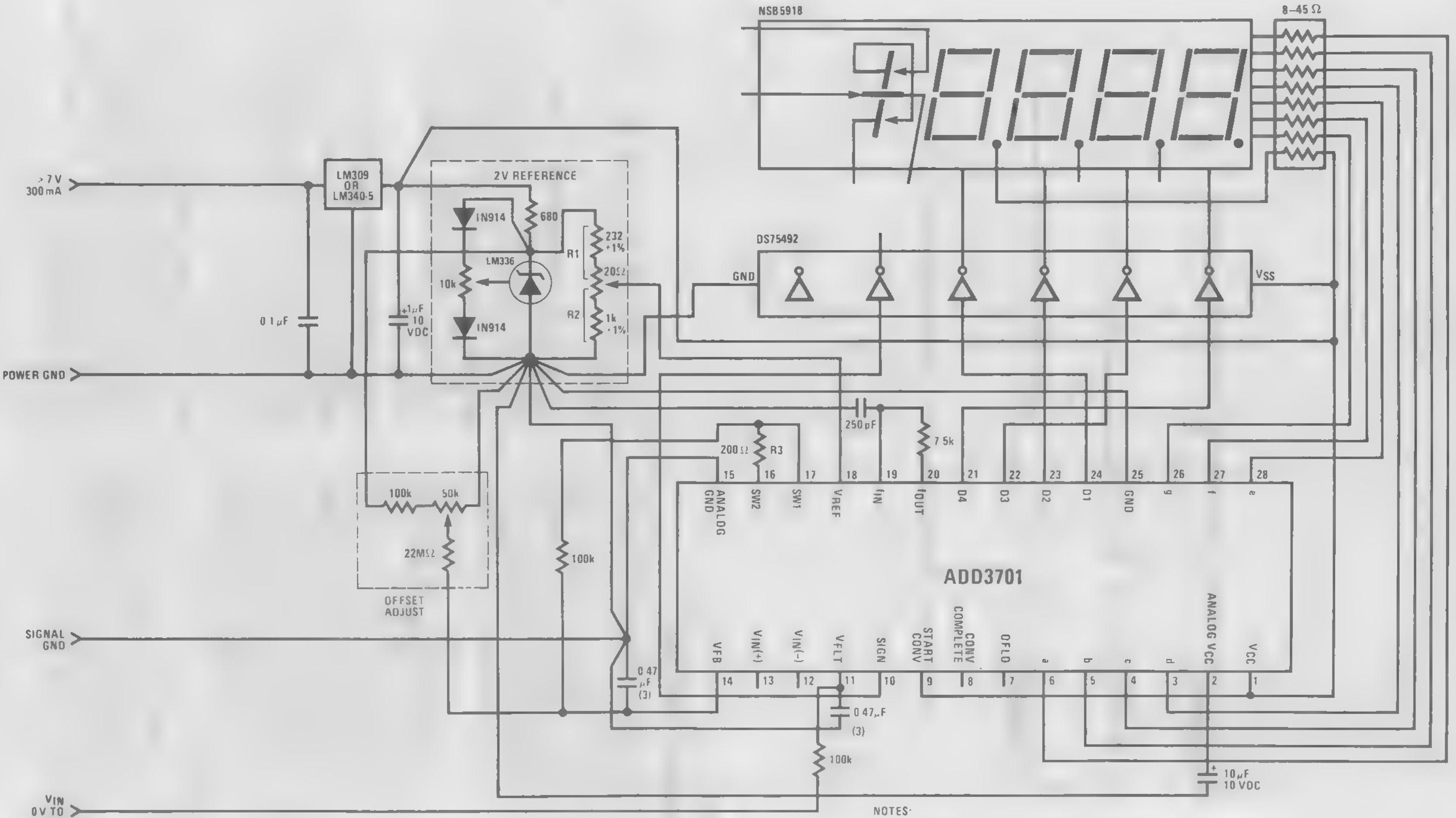
The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0 to +3.999 counts operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 5.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

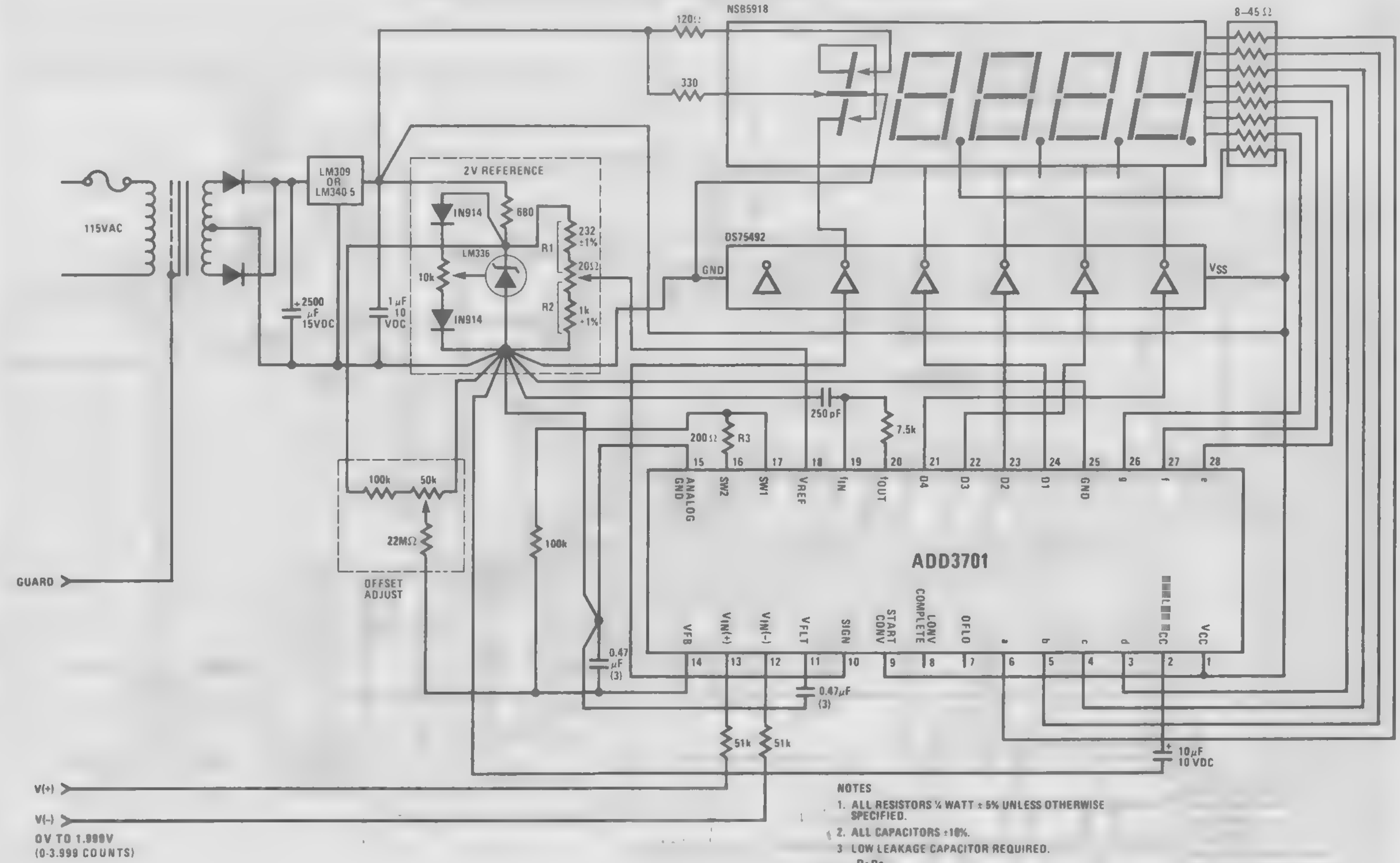
The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error (1.0×10^{-9} A x 100 kΩ = 0.1 mV). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 4. 3¾-Digit DPM, +3.999 Count Full Scale



NOTES

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Figure 5. 3¾-Digit DPM, ±3.999 Counts Full Scale

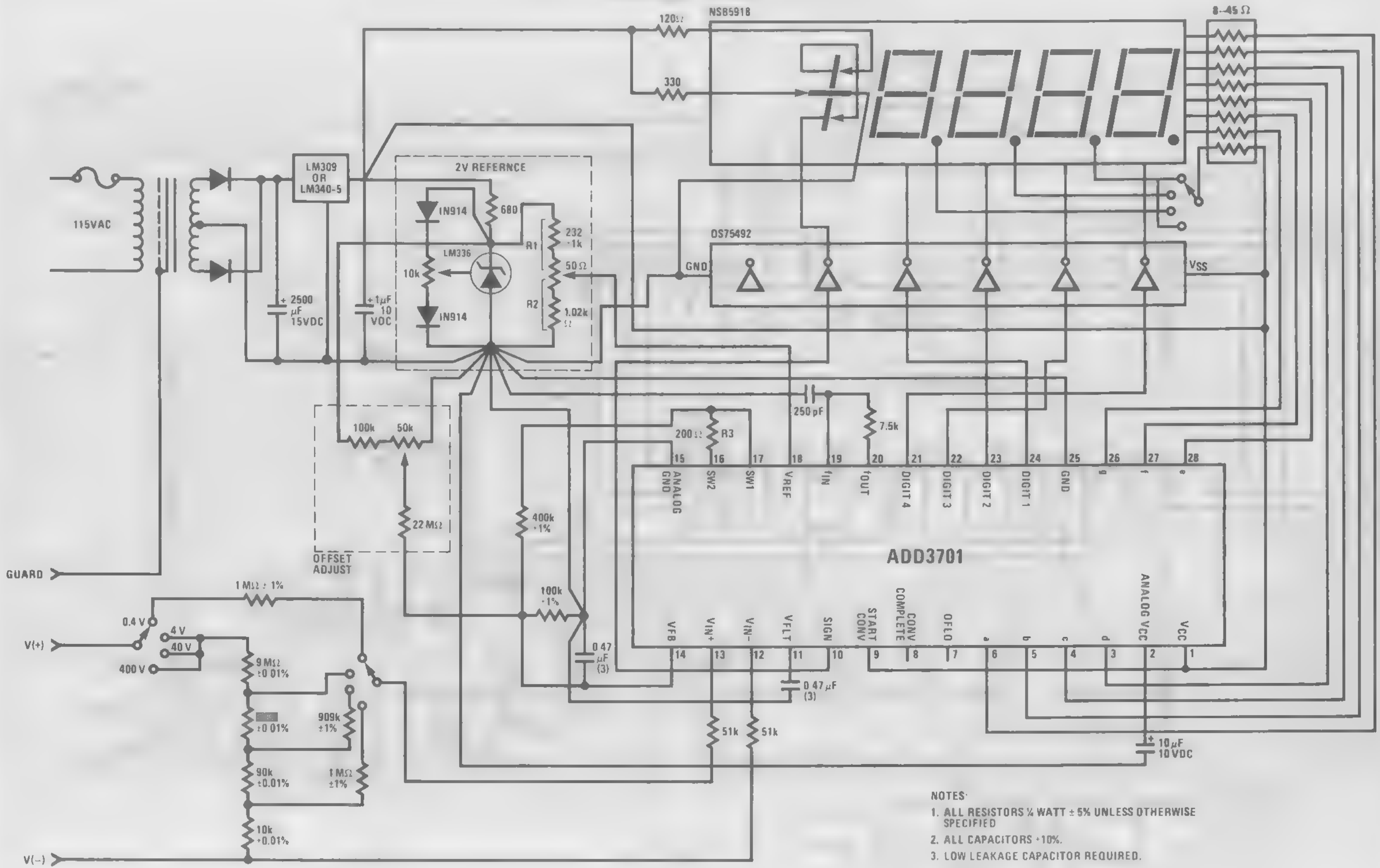

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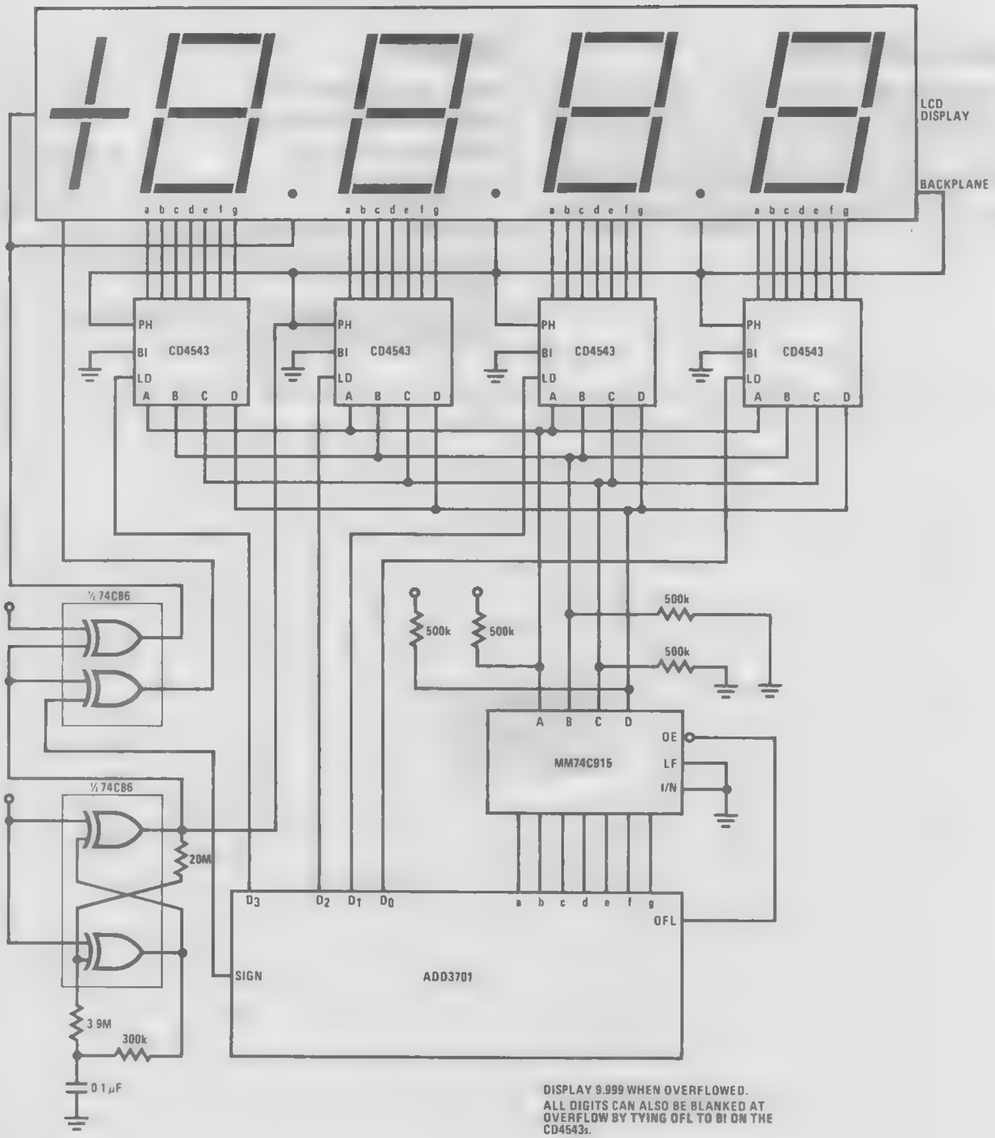
Figure 6. 3¾-Digit DVM, Four Decade, ±0.4V, ±4V, ±40V, and ±400V Full Scale



DISPLAY 9.999 WHEN OVERFLOWED.

ALL DIGITS CAN ALSO BE BLANKED AT OVERFLOW BY TYING OFL TO BI ON THE CD4543s.

Figure 7. ADD3701 Driving Liquid Crystal Display

National Semiconductor

MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	10. V
■ High noise immunity	0.45 V_{CC} typ.
■ Low power TTL compatibility	fan out of 2 driving 74L

- Provision for register extension or truncation
- Operates in START/STOP or continuous conversation mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

See page 2-7
for Detailed
Specifications

National Semiconductor

PRELIMINARY

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the 8080A control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

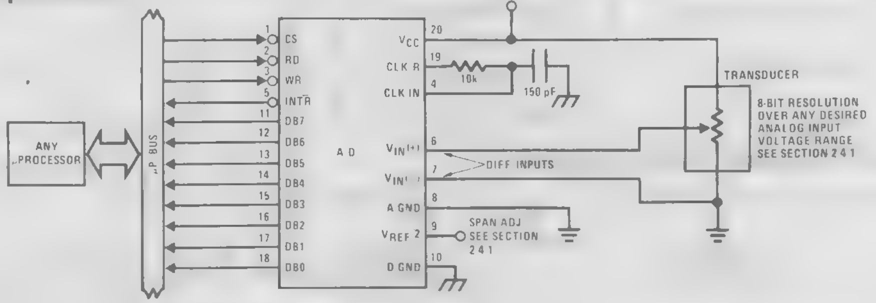
- Compatible with 8080 μP derivatives—no interfacing logic needed
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package

Key Specifications

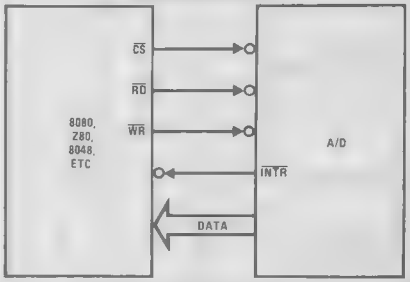
Resolution	8 bits
Total error	±1/4 LSB, ±1/2 LSB and ±1 LSB
Conversion time	100 μs
Access time	135 ns
Single supply	5 V_{DC}

- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Typical Applications



8080 Interface

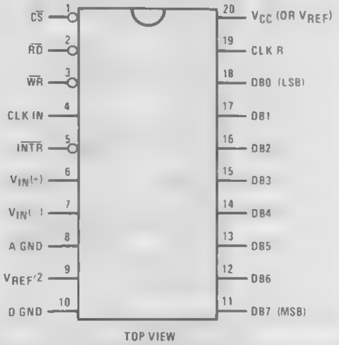


PART NUMBER	FULL SCALE ADJUSTED	$V_{REF}/2 = 2.500\ V_{DC}$ (NO ADJUSTMENTS)	$V_{REF}/2$ = NO CONNECTION (NO ADJUSTMENTS)
ADC0801	±1/4 LSB		
ADC0802		±1/2 LSB	
ADC0803	±1/2 LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

LINEARITY SPECIFICATION

Connection Diagram

ADC080X
Dual-In-Line Package



TOP VIEW

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02/03LD	$-55°C \leq T_A \leq +125°C$
ADC0801/02/03/04LCD	$-40°C \leq T_A \leq +85°C$
ADC0801/02/03/05LCN	$-40°C \leq T_A \leq +85°C$
ADC0804LCN	$0°C \leq T_A \leq +70°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC0801 Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/4	LSB
ADC0802 Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC} ($R_{SOURCE} \leq 20\Omega$)			±1/2	LSB
ADC0803 Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/2	LSB
ADC0804 Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC} ($R_{SOURCE} \leq 20\Omega$)			±1	LSB
ADC0805 Total Unadjusted Error	$V_{REF}/2$ – NC ($R_{SOURCE} \leq 20\Omega$)			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±1/8	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 6V, (Note 5)	100	640	1280	kHz
		V_{CC} = 5V	100	640	800	kHz
T_c	Conversion Time	(Note 6)	66		73	$1/f_{CLK}$
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz			8770	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	250	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_{T+}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 μA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 μA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{\text{INTR}}$						
V_{OUT}(0)	Logical "0" Output Voltage					
	Data Outputs	I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
	$\overline{\text{INTR}}$ Output	I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC}	−3			μA_{DC}
		V_{OUT} = 5 V_{DC}			3	μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{\text{CS}}$ = "1"				
		ADC0801/02/03		1.1	1.8	mA
		ADC0804 (Note 9)		1.9	2.5	mA

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With V_{CC} = 6V, the digital logic interfaces are no longer TTL compatible.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

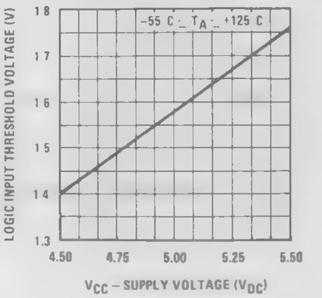
Note 7: The $\overline{\text{CS}}$ input is assumed to bracket the $\overline{\text{WR}}$ strobe input and therefore timing is dependent on the $\overline{\text{WR}}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{\text{WR}}$ pulse (see timing diagrams).

Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

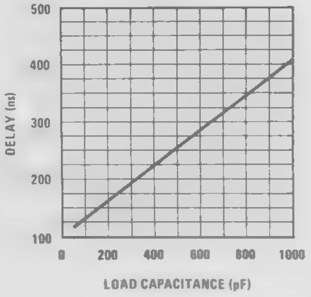
Note 9: For ADC0804LCD typical value of $V_{REF}/2$ input resistance is 8 kΩ and of I_{CC} is 1.1 mA.

Typical Performance Characteristics

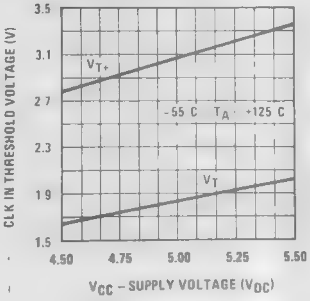
Logic Input Threshold Voltage vs. Supply Voltage



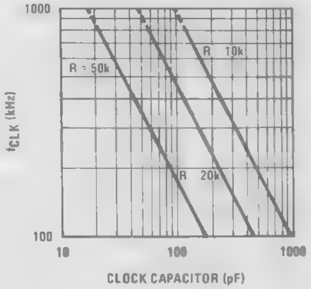
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



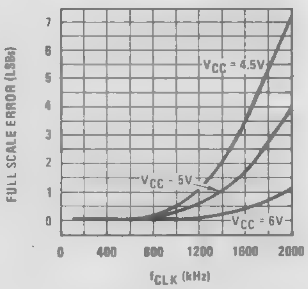
CLK IN Schmitt Trip Levels vs. Supply Voltage



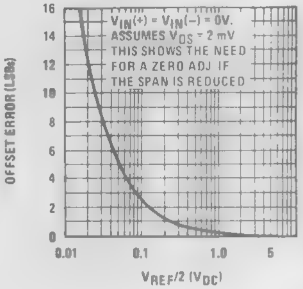
fCLK vs. Clock Capacitor



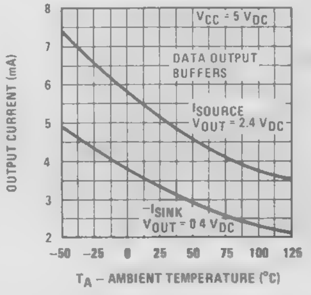
Full-Scale Error vs fCLK



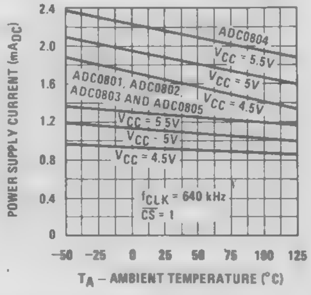
Effect of Unadjusted Offset Error vs. VREF/2 Voltage



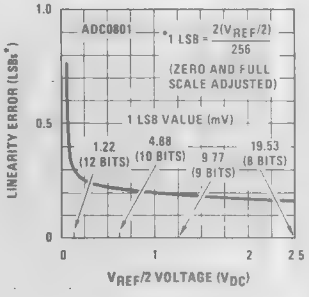
Output Current vs Temperature



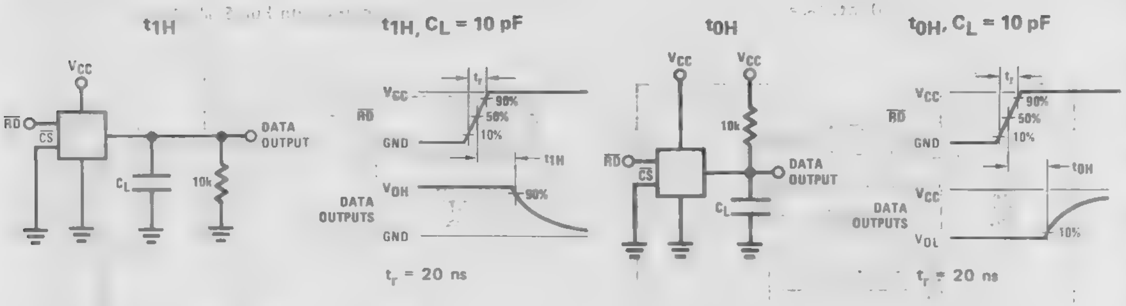
Power Supply Current vs Temperature (Note 9)



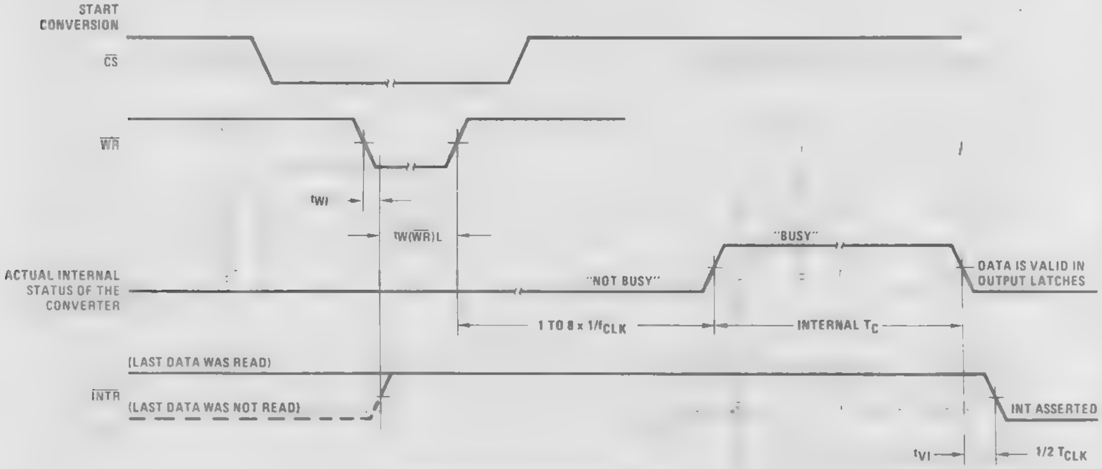
Linearity Error at Low VREF/2 Voltages



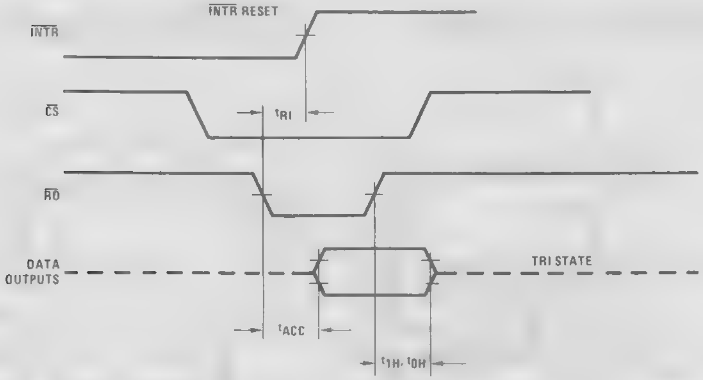
TRI-STATE® Test Circuits and Waveforms



Timing Diagrams



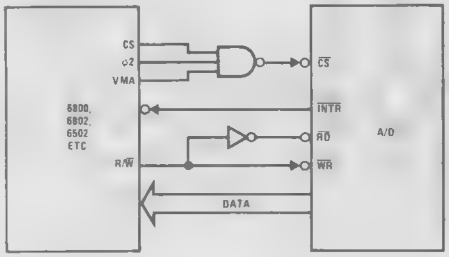
Output Enable and Reset INTR



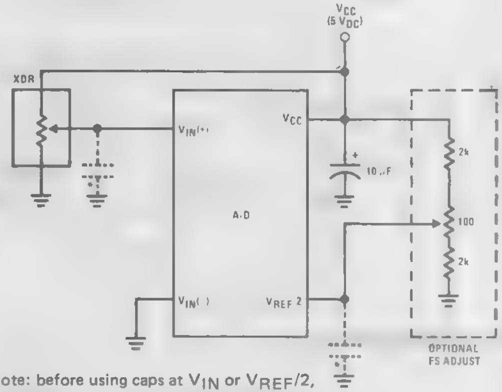
Note: All timing is measured from the 50% voltage points.

Typical Applications (Continued)

6800 Interface

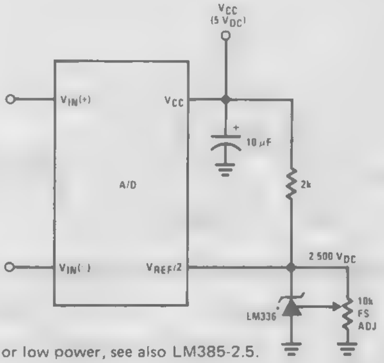


Ratiometric with Full-Scale Adjust



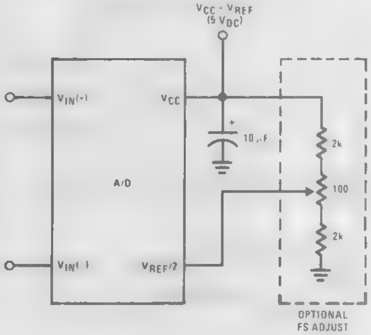
*Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

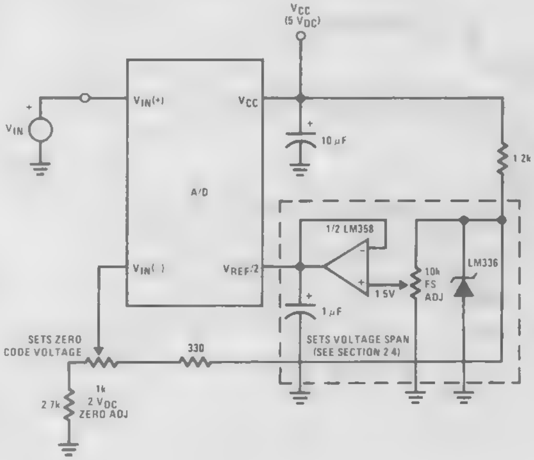


*For low power, see also LM385-2.5.

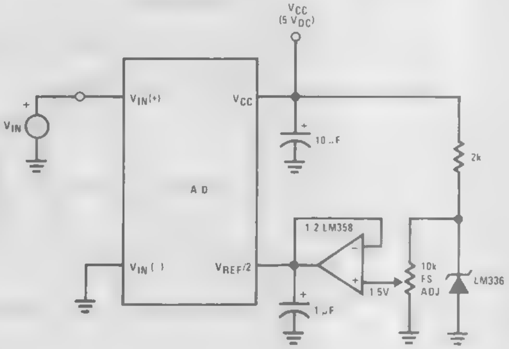
Absolute with a 5V Reference

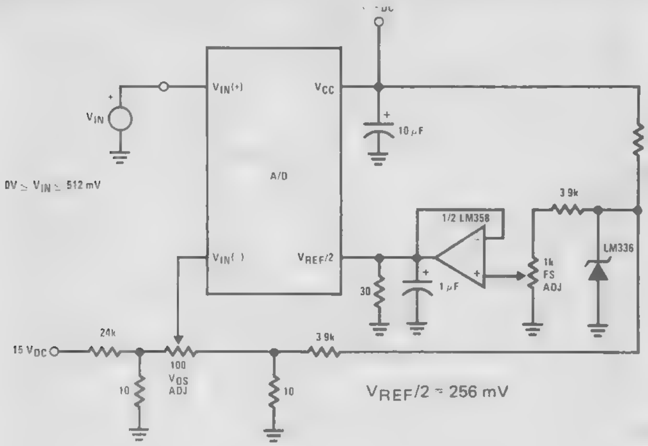


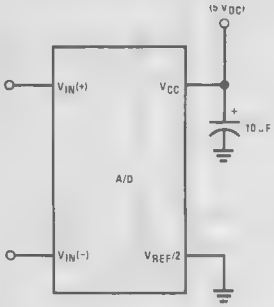
Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



Zero-Shift and Span Adjust: $0V \leq V_{IN} \leq 3V$

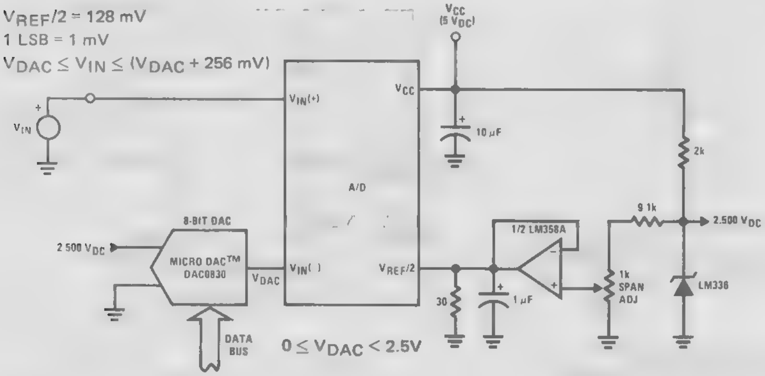




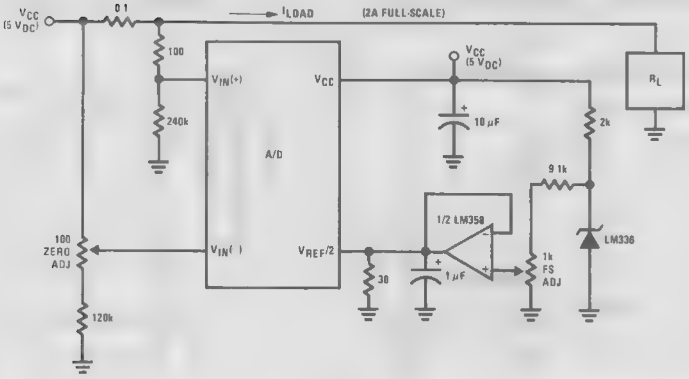


For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with µP Controlled Range

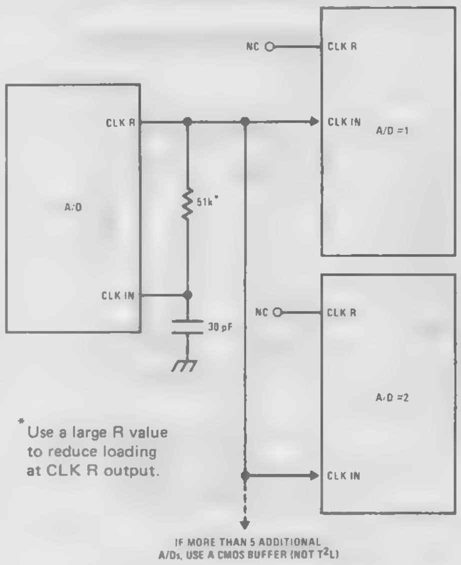


Digitizing a Current Flow



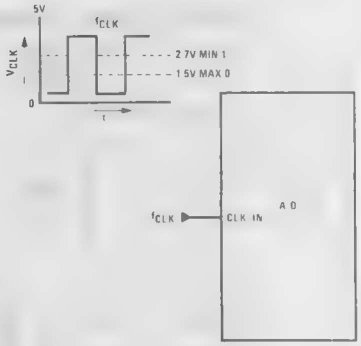
Typical Applications (Continued)

Self-Clocking Multiple A/Ds



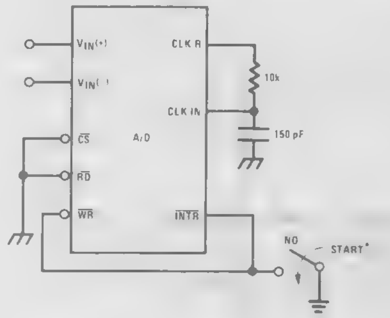
*Use a large R value to reduce loading at CLK R output.

External Clocking



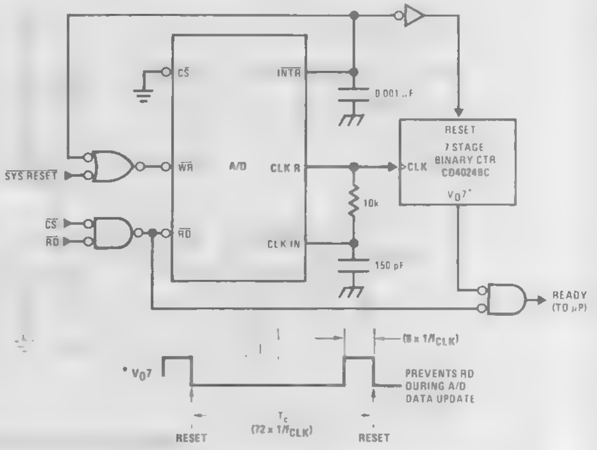
100 kHz ≤ f_{CLK} ≤ 800 kHz

Self-Clocking in Free-Running Mode

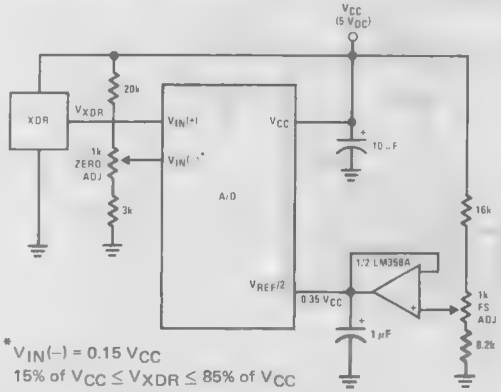


*After power-up, a momentary grounding of the WR input is needed to guarantee operation.

μP Interface for Free-Running A/D

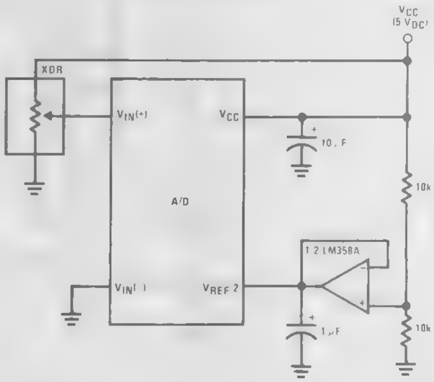


Operating with "Automotive" Ratiometric Transducers



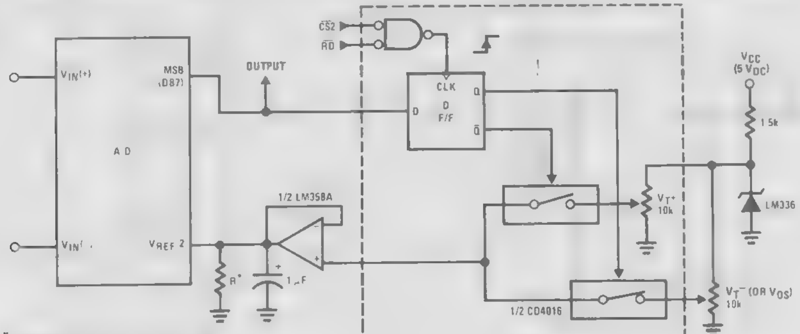
*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \le V_{XDR} \le$ 85% of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

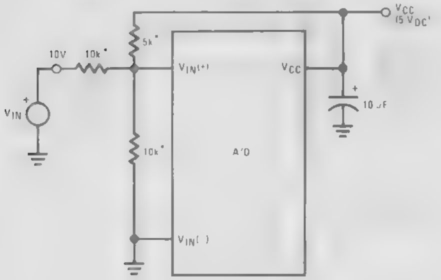


*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + 2 (V_{REF}/2)$

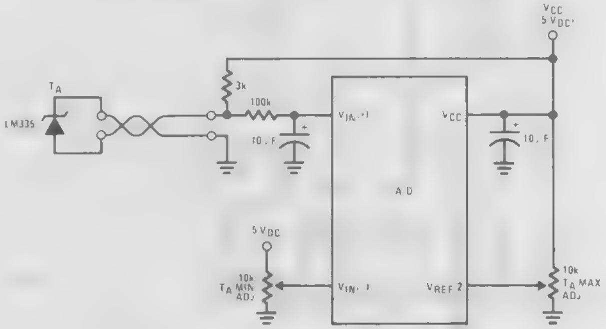
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

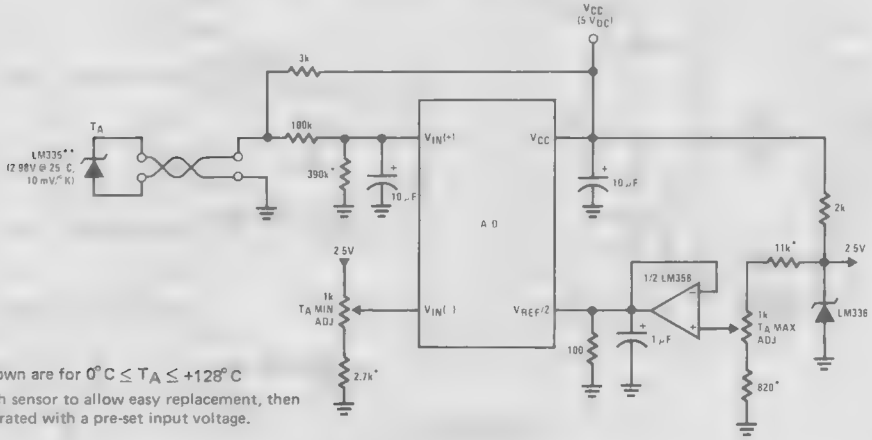


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

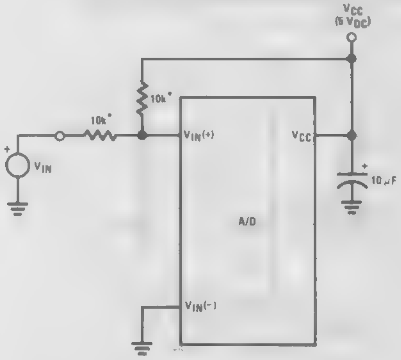


*Circuit values shown are for $0°C \le T_A \le +128°C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

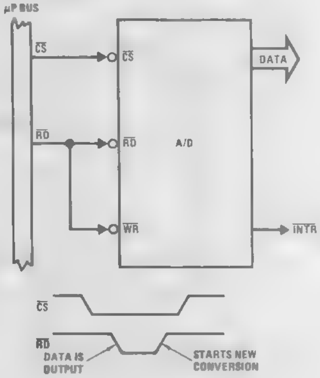
Typical Applications (Continued)

Handling ±5V Analog Inputs

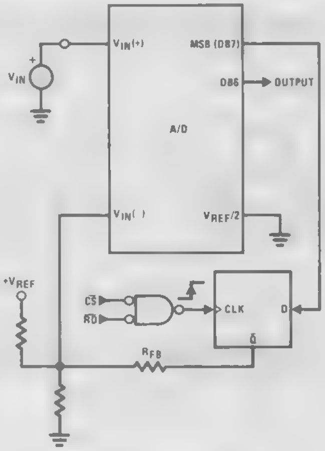


*Beckman Instruments #694-3-R10K resistor array

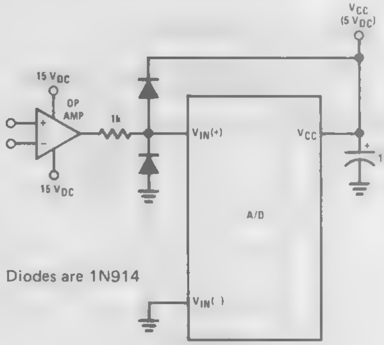
Read-Only Interface



µP Interfaced Comparator with Hysteresis

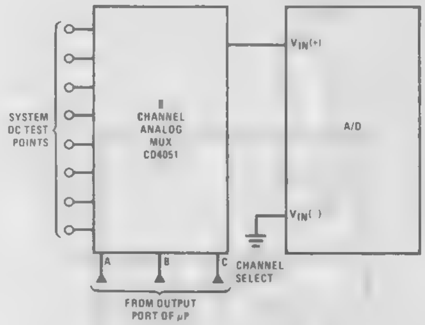


Protecting the Input

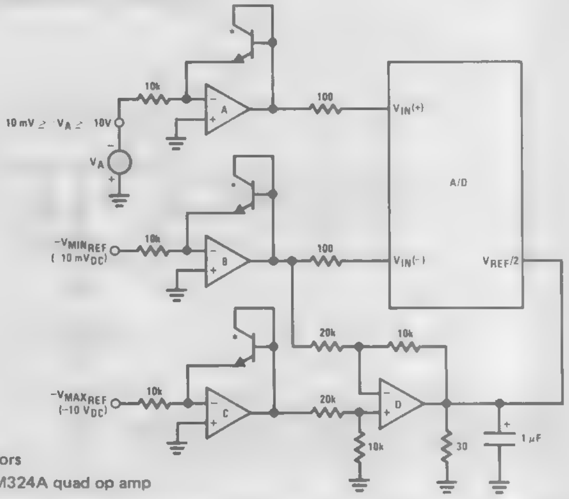


Diodes are 1N914

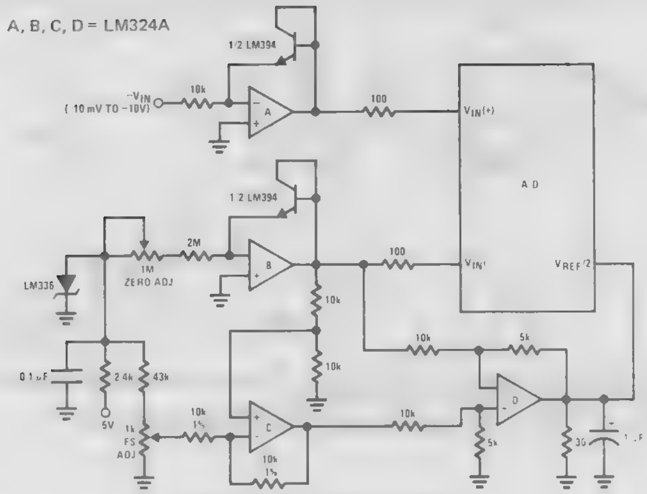
Analog Self-Test for a System



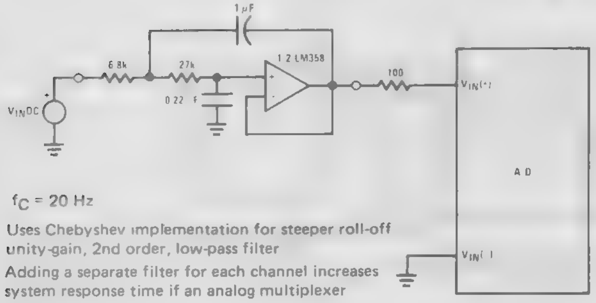
A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors
A, B, C, D = LM324A quad op amp



Noise Filtering the Analog Input

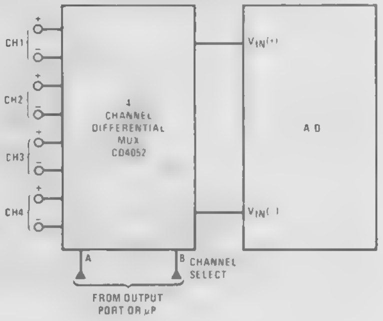


f_C = 20 Hz

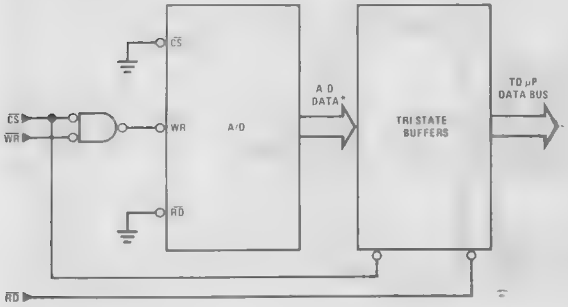
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

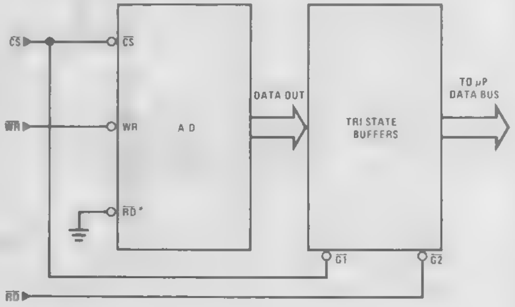


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of INTR

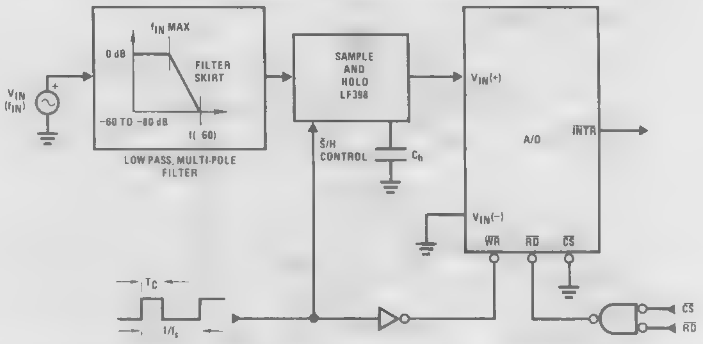
Increasing Bus Drive and/or Reducing Time on Bus



*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

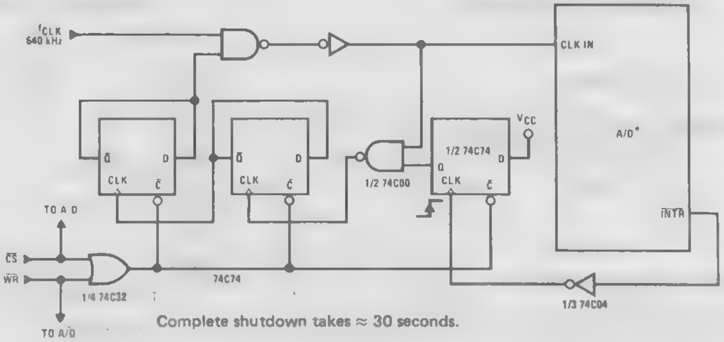
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

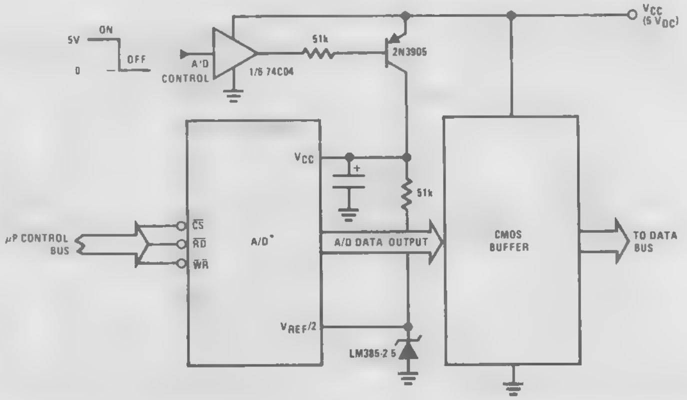
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



Complete shutdown takes ≈ 30 seconds.

Power Savings by A/D and V_{REF} Shutdown



*Use ADC0801, 02 or 03 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving outputs of A/D when in shutdown mode.

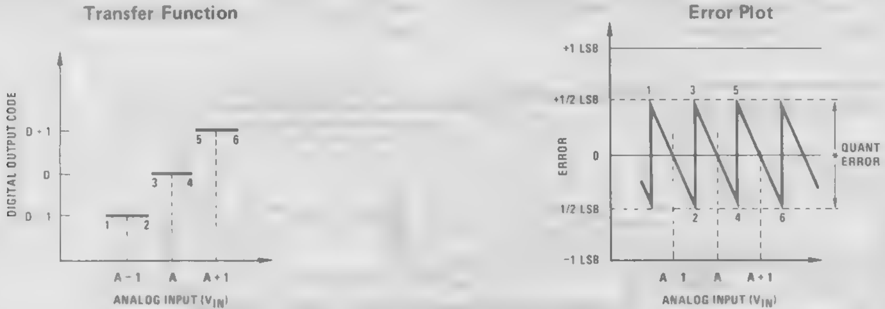
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a.* The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±1/4 LSB. In other words, if we apply an analog input equal to the center-value ±1/4 LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

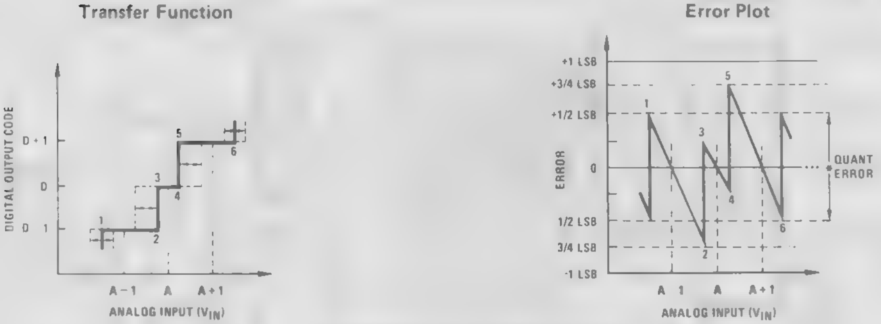
The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.


Transfer Function

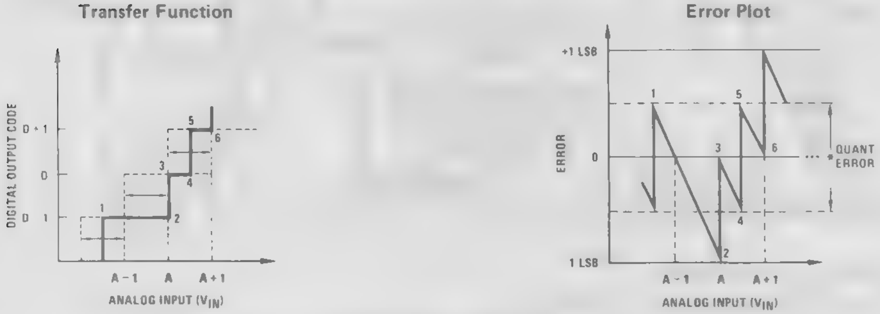
Error Plot

a) Accuracy = ±0 LSB A Perfect A/D


Transfer Function

Error Plot

b) Accuracy = ±1/4 LSB


Transfer Function

Error Plot

c) Accuracy = ±1/2 LSB

FIGURE 1. Clarifying the Error Specs of an A/D Converter

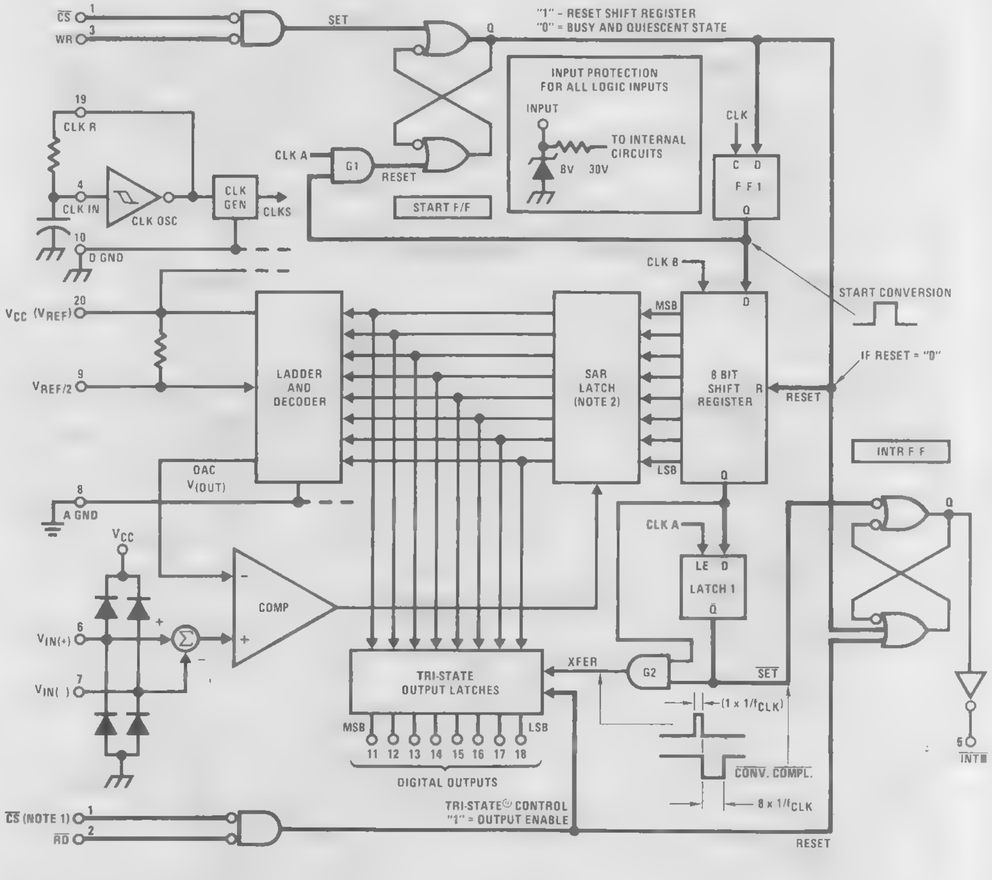
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{\text{INTR}}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{\text{INTR}}$ to the $\overline{\text{WR}}$ input with $\overline{\text{CS}}$ = 0. To insure start-up under all possible conditions, an external $\overline{\text{WR}}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{\text{WR}}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{\text{CS}}$ input and $\overline{\text{WR}}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2.* All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{\text{CS}}$ and $\overline{\text{WR}}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{\text{WR}}$ or $\overline{\text{CS}}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{\text{CS}}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{\text{INTR}}$ output signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ both held low), the $\overline{\text{INTR}}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{\text{INTR}}$ pin tied to $\overline{\text{WR}}$ and $\overline{\text{CS}}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{\text{Q}}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\text{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{\text{WR}}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\text{RD}}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(\text{MAX}) = (V_P)\ (2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_e(\text{MAX})\ (f_{CLK})]}{(2\pi f_{cm})\ (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\ (640 \times 10^3)}{(6.28)\ (60)\ (4.5)}$$

which gives

$$V_P \cong 1.9\text{V}.$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

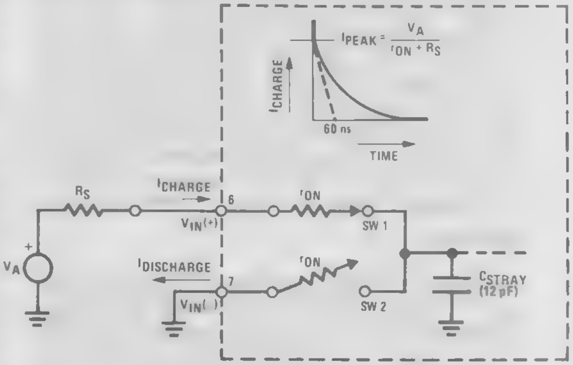
An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



r_{ON} of SW 1 and SW 2 $\cong$ 5 kΩ

$\tau = r_{ON}\,C_{STRAY} \cong 5\text{ k}\Omega \times 12\text{ pF} = 60\text{ ns}$

FIGURE 3. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source which is applied to the $V_{IN}(+)$ pin exceeds the allowed operating range of V_{CC} + 50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents could exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

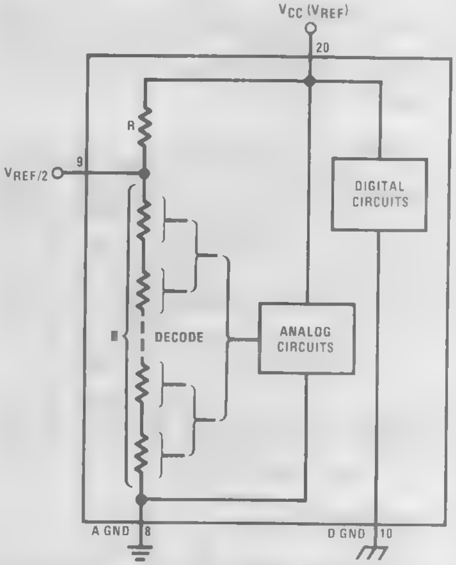
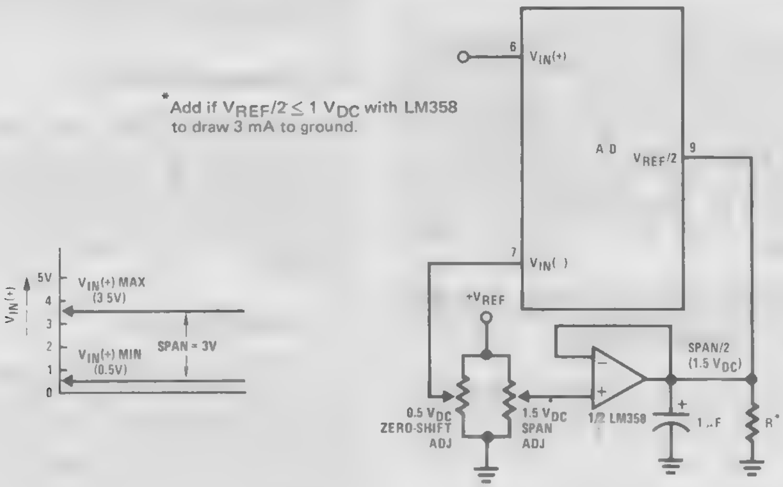


FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either 1/2 of the voltage which is applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to 1/2 of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.



*Add if $V_{REF}/2 \leq 1$ V_{DC} with LM358 to draw 3 mA to ground.

a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) is available which has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D V_{IN} (−) input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V (−) input and applying a small magnitude positive voltage to the V (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for $V_{REF}/2 = 2.500$ V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1-1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code which is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.

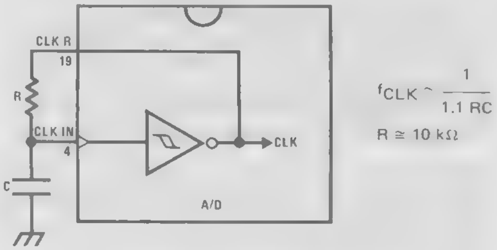


FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power T^2L buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard T^2L buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output also simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to insure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky is recommended such as the DM74LS240 series) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120 − 1 1/2 LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the decoded voltages which are obtained from the column: Input voltage value for a 2.560 $V_{REF}/2$ of both the MS and the LS groups, the value of the digital display can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in 2 digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A−C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

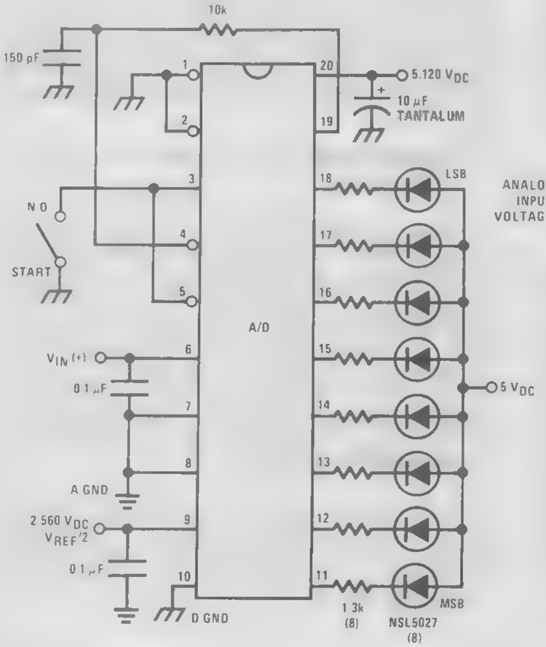


FIGURE 7. Basic A/D Tester

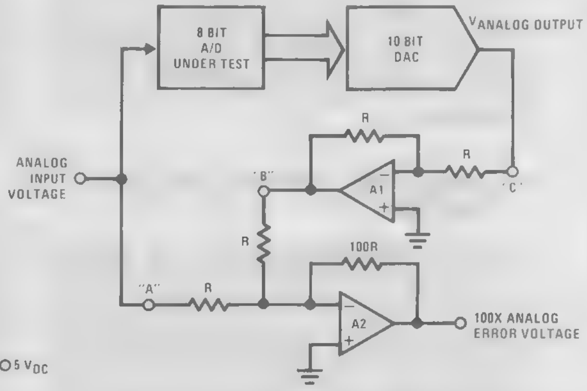


FIGURE 8. A/D Tester with Analog Error Output

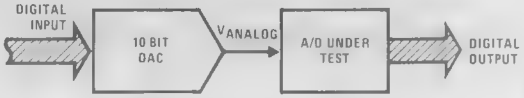


FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	5/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1.280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*V Display Output = VMS Group + VLS Group

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A, 6800 and SC/MP-II microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored at location 0200 to 020F. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

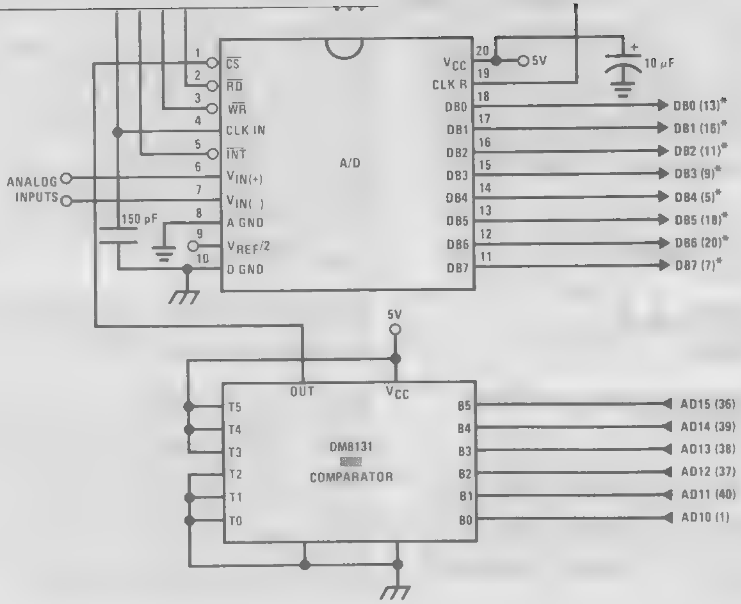
This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for CS and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

The standard control bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bidirectional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.



Note 1: *Pin numbers for the INS8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:              JMP    LD DATA
 .         .           .
 .         .           .
0100    21 00 02    START:              LXI H 0200H         ; HL pair will point to
                                                            ; data storage locations
0103    31 00 04    RETURN:             LXI SP 0400H        ; Initialize stack pointer (Note 1)
0106    7D                              MOV A, L            ; Test # of bytes entered
0107    FE OF                           CPI OF H            ; If # = 16. JMP to
0109    CA 13 01                        JZ CONT             ; user program
010C    D3 E0                           OUT E0 H            ; Start A/D
010E    FB                              EI                  ; Enable interrupt
010F    00          LOOP:               NOP                 ; Loop until end of
0110    C3 0F 01                        JMP LOOP            ; conversion
0113       .        CONT:                .
 .         .           .                 .
 .         .        (User program to     .
 .         .        process data)        .
 .         .           .                 .
 .         .           .                 .
0300    DB E0       LD DATA:            IN E0 H             ; Load data into accumulator
0302    77                              MOV M, A            ; Store data
0303    23                              INX H               ; Increment storage pointer
0304    C3 03 01                        JMP  RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All addresses used were arbitrarily chosen.

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 11*.

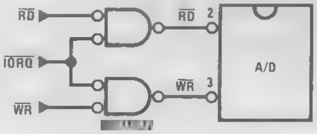


FIGURE 11. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 12* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

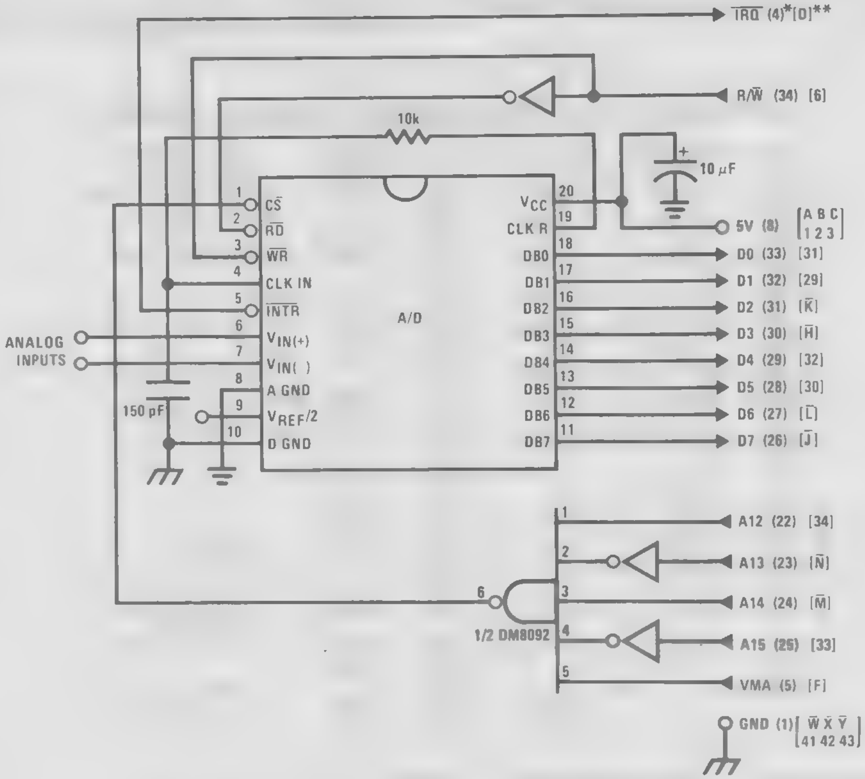
The following subroutine essentially performs the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 13* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

SAMPLE PROGRAM FOR *FIGURE 12* ADC0801–MC6800 CPU INTERFACE

```
0010    DF 36       DATAIN    STX     TEMP2      ; Save contents of X
0012    CE 00 2C              LDX     #$002C     ; Upon IRQ low CPU
0015    FF FF F8              STX     $FFF8      ; jumps to 002C
0018    B7 50 00              STAA    $5000      ; Starts ADC0801
001B    0E                    CLI
001C    3E          CONVRT    WAI                ; Wait for interrupt
001D    DE 34                 LDX     TEMP1
001F    8C 02 0F              CPX     #$020F     ; Is final data stored?
0022    27 14                 BEQ     ENDP
0024    B7 50 00              STAA    $5000      ; Restarts ADC0801
0027    08                    INX
0028    DF 34                 STX     TEMP1
002A    20 F0                 BRA     CONVRT
002C    DE 34       INTRPT    LDX     TEMP1
002E    B6 50 00              LDAA    $5000      ; Read data
0031    A7 00                 STAA    X          ; Store it at X
0033    3B                    RTI
0034    02 00       TEMP1     FDB     $0200      ; Starting address for
                                                 ; data storage
0036    00 00       TEMP2     FDB     $0000
0038    CE 02 00    ENDP      LDX     #$0200     ; Reinitialize TEMP1
003B    DF 34                 STX     TEMP1
003D    DE 36                 LDX     TEMP2
003F    39                    RTS                ; Return from subroutine
                                                 ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 12. ADC0801–MC6800 CPU Interface

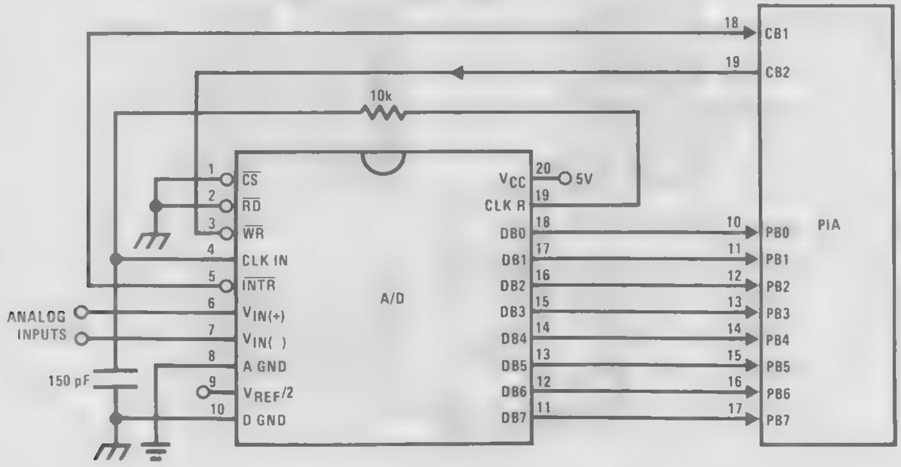


FIGURE 13. ADC0801–MC6820 PIA Interface

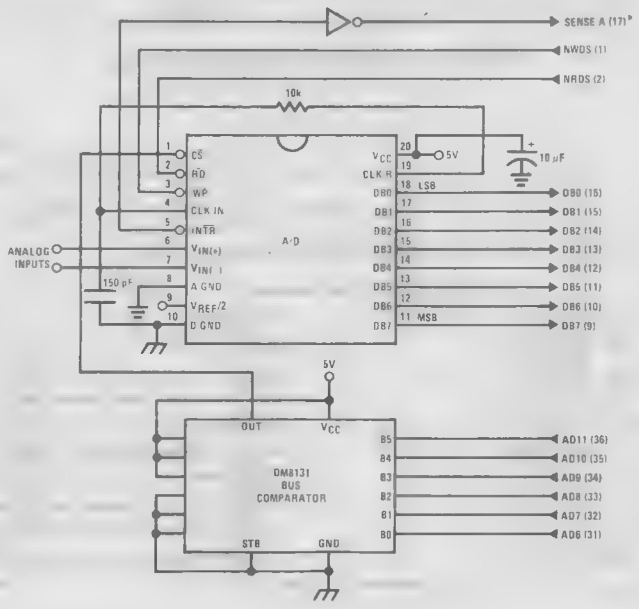
A sample interface program equivalent to the previous one, is shown below. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

4.4 Interfacing the INS8060–SC/MP-II

The SC/MP-II interface technique with the ADC0801 series *Figure 14*, is similar to the 8080A CPU interface.

SAMPLE PROGRAM FOR *FIGURE 13* ADC0801–MC6820 PIA INTERFACE

```
0010    CE 00 38    DATAIN    LDX     #$0038     ; Upon IRQ low CPU
0013    FF FF F8              STX     $FFF8      ; jumps to 0038
0016    B6 80 06              LDAA    PIAORB     ; Clear possible IRQ flags
0019    4F                    CLRA
001A    B7 80 07              STAA    PIACRB
001D    B7 80 06              STAA    PIAORB     ; Set Port B as input
0020    0E                    CLI
0021    C6 34                 LDAB    #$34
0023    86 3D                 LDAA    #$3D
0025    F7 80 07    CONVRT    STAB    PIACRB     ; Starts ADC0801
0028    B7 80 07              STAA    PIACRB
002B    3E                    WAI                ; Wait for interrupt
002C    DE 40                 LDX     TEMP1
002E    8C 02 0F              CPX     #$020F     ; Is final data stored?
0031    27 0F                 BEQ     ENDP
0033    08                    INX
0034    DF 40                 STX     TEMP1
0036    20 ED                 BRA     CONVRT
0038    DE 40       INTRPT    LDX     TEMP1
003A    B6 80 06              LDAA    PIAORB     ; Read data in
003D    A7 00                 STAA    X          ; Store it at X
003F    3B                    RTI
0040    02 00       TEMP1     FDB     $0200      ; Starting address for
                                                 ; data storage
0042    CE 02 00    ENDP      LDX     #$0200     ; Reinitialize TEMP1
0045    DF 40                 STX     TEMP1
0047    39                    RTS                ; Return from subroutine
                    PIAORB    EQU     $8006      ; To user's program
                    PIACRB    EQU     $8007
```



*Pin numbers in parentheses are for the SC/MP CPU.

FIGURE 14. ADC0801–SC/MP-II Microprocessor Interface

The A/D is treated as a peripheral and it is mapped into the memory space of the SC/MP-II system. An address, 0D00, is assigned to the A/D and the $\overline{CS}$ signal is shown to be decoded by a bus comparator, DM8131. The $\overline{RD}$ and $\overline{WR}$ pins of the A/D are tied directly to the Write Data Strobe, NWRS, and Read Data Strobe, NRDS, pins of the SC/MP-II CPU. Notice that the $\overline{INTR}$ signal should be inverted before being tied to the SENSE A pin of the SC/MP-II. A sample interface program is shown below.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor which is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 15.*

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801–SC/MP-II MICROPROCESSOR INTERFACE

```
0100       08                  NOP
0101    C4 02                  LDI02
0103       35                  XPAH(P1)
0104    C4 0D                  LDI0D
0106       36                  XPAH(P2)
0107    C4 03                  LDI03
0109       37                  XPAH(P3)
010A    C4 00                  LDI00
010C       31                  XPAL(P1)      ; P1=0200, P1 points to 1st byte address
010D    C4 00                  LDI00
010F    C9 11                  ST(P1+11)     ; Zero the byte count in address 0211
0112       32                  XPAL(P2)      ; P2=0D00, P2 points to A/D
0113    CA 00     START:       ST(P2)        ; START the A/D
0115    C4 00                  LDI00
0117       33                  XPAL(P3)      ; P3=0300, P3 points to DATA in sub.
0118       05                  IEN           ; starting address
0119       08     LOOP:        NOP
011A    90 FE                  JMP(LOOP)
                  User's Program
011C              USER         NOP
011D                           NOP
                                .
                                .
                                .
0300    C2 00     DATA IN:     LD(P2)        ; Load A/D data into accumulator
0302    CD 01                  ST@1(P1)      ; Store A/D data and increment byte
                                             ; address
0304    A9 11                  1LD(P1+11)    ; Increment byte count
0306    C4 0F                  LDI0F
0308       03                  SCL
0309    F9 11                  CAD(P1+11)    ; 0F–(P1+11): Is byte count = 16?
030B    9B 03                  JZ(USER)      ; If byte count = 16 jump to user's
                                             ; program
030D    C4 13                  LDI13
030F       33                  XPAL(P3)      ; P3=0113
0310       3F                  XPPC(P3)      ; Go to START and do another conversion
```

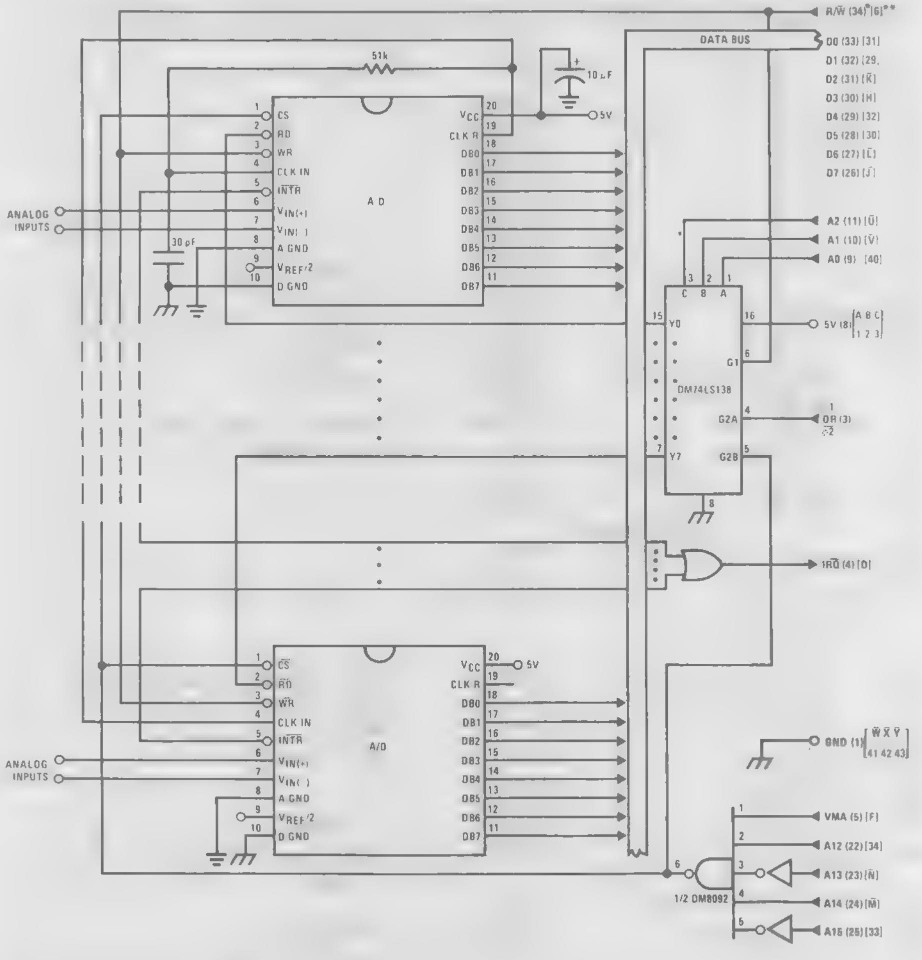
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. Interfacing Multiple A/Ds in an MC6800 System

PROGRAM FOR *FIGURE 15* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

```
ADDRESS   HEX CODE              MNEMONICS                   COMMENTS

 0010     DF 44       DATAIN   STX    TEMP      ;Save Contents of X
 0012     CE 00 2A             LDX    #$002A    ;Upon IRQ LOW CPU
 0015     FF FF F8             STX    $FFF8     ;Jumps to 002A
 0018     B7 50 00             STAA   $5000     ;Starts all A/D's
 001B     0E                   CLI
 001C     3E                   WAI              ;Wait for interrupt
 001D     CE 50 00             LDX    #$5000
 0020     DF 40                STX    INDEX1    ;Reset both INDEX
 0022     CE 02 00             LDX    #$0200    ;1 and 2 to starting
 0025     DF 42                STX    INDEX2    ;addresses
 0027     DE 44                LDX    TEMP
 0029     39                   RTS              ;Return from subroutine
 002A     DE 40       INTRPT   LDX    INDEX1    ;INDEX1 → X
 002C     A6 00                LDAA   X         ;Read data in from A/D at X
 002E     08                   INX              ;Increment X by one
 002F     DF 40                STX    INDEX1    ;X → INDEX1
 0031     DE 42                LDX    INDEX2    ;INDEX2 → X
 0033     A7 00                STAA   X         ;Store data at X
 0035     8C 02 07             CPX    #$0207    ;Have all A/D's been read?
 0038     27 05                BEQ    RETURN    ;Yes:  branch to RETURN
 003A     08                   INX              ;No:  increment X by one
 003B     DF 42                STX    INDEX2    ;X → INDEX2
 003D     20 EB                BRA    INTRPT    ;Branch to 002A
 003F     3B          RETURN   RTI
 0040     50 00       INDEX1   FDB    $5000     ;Starting address for A/D
 0042     02 00       INDEX2   FDB    $0200     ;Starting address for data storage
 0044     00 00       TEMP     FDB    $0000
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

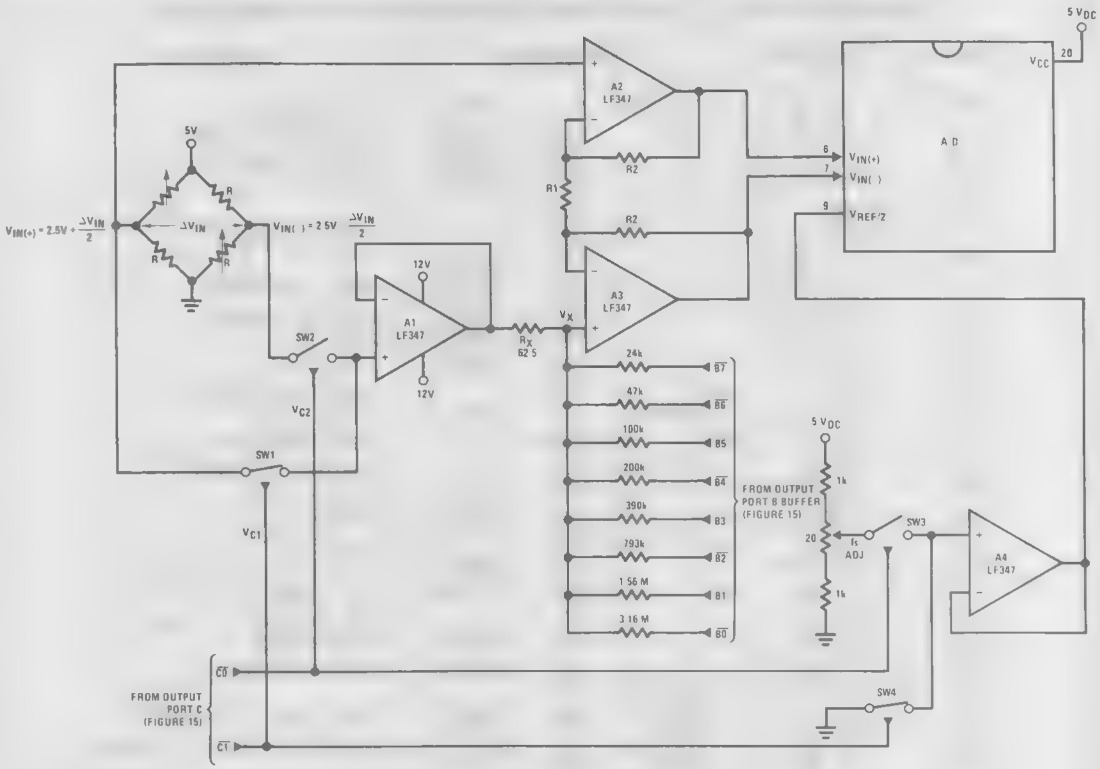
For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 16* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for 1/4 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_o = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} + \underbrace{(V_{os2} - V_{os1} - V_{os3} \pm I_x R_x)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_x is the current through resistor R_x. All of the offset error terms can be cancelled by making $\pm I_x R_x = V_{os1} + V_{os3} - V_{os2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 17*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by insuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_x thus raising the voltage at V_x and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_x and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_x can move ±12 mV with a resolution of 50 μV which will null the offset error term to 1/4 LSB of full-scale for the ADC0801. It is important that the voltage levels which drive the autozero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 1: R2 = 49.5 R1

Note 2: Switches are CD4066BC CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 16. Gain of 100 Differential Transducer Preamp

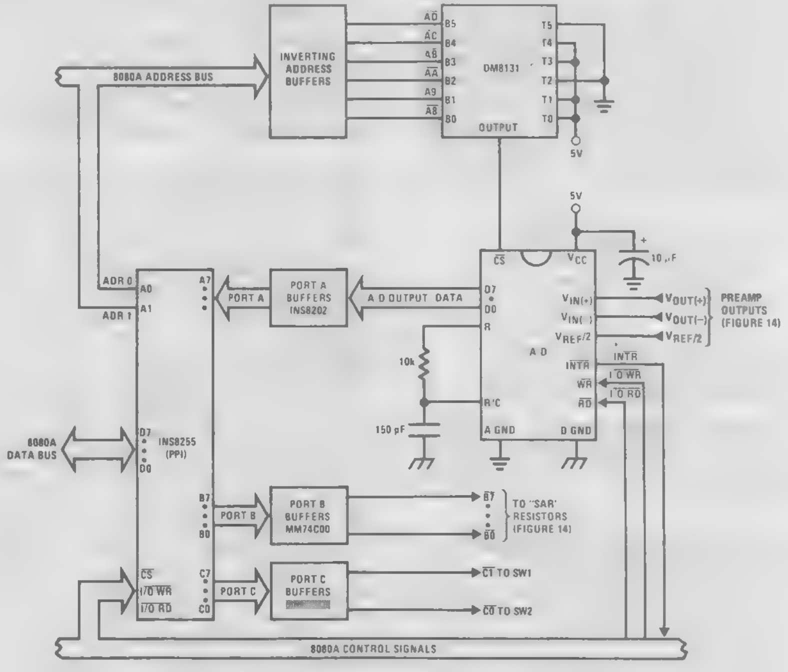


FIGURE 17. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 18*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input $[V_{IN}(-) \geq V_{IN}(+)]$. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_x more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_x more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 19*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4
Port B is at port address E5
Port C is at port address E6
PPI control word port is at port address E7
Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 20* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{\text{INTR}}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{\text{INTR}}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

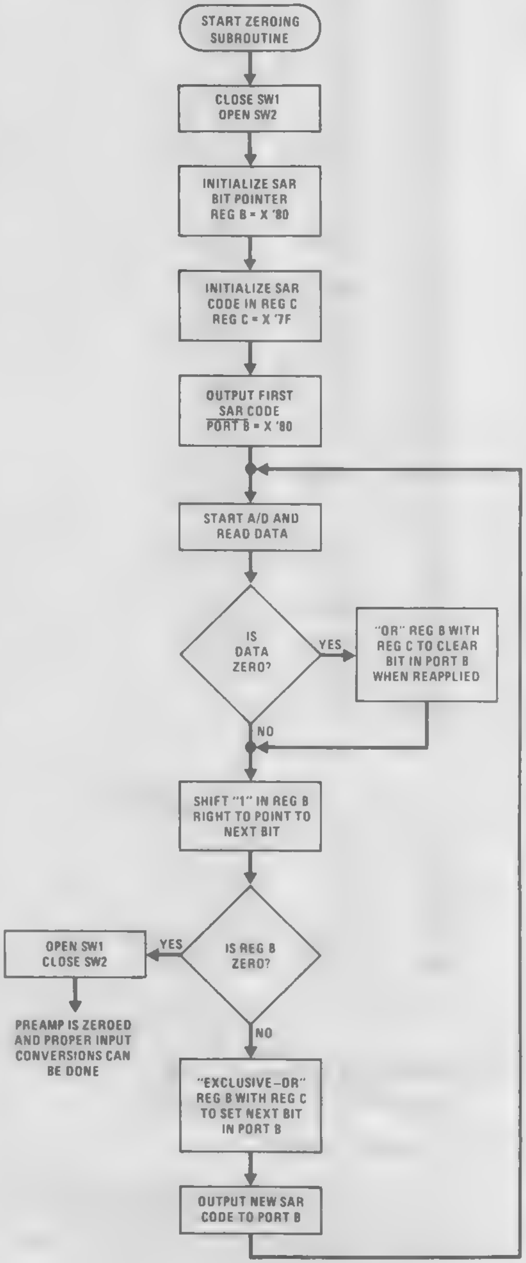

START ZEROING SUBROUTINE
CLOSE SW1 OPEN SW2
INITIALIZE SAR BIT POINTER REG B = X '80
INITIALIZE SAR CODE IN REG C REG C = X '7F
OUTPUT FIRST SAR CODE PORT B = X '80
START A/D AND READ DATA
IS DATA ZERO?
YES
"OR" REG B WITH REG C TO CLEAR BIT IN PORT B WHEN REAPPLIED
NO
SHIFT "1" IN REG B RIGHT TO POINT TO NEXT BIT
IS REG B ZERO?
YES
OPEN SW1 CLOSE SW2
PREAMP IS ZEROED AND PROPER INPUT CONVERSIONS CAN BE DONE
NO
"EXCLUSIVE-OR" REG B WITH REG C TO SET NEXT BIT IN PORT B
OUTPUT NEW SAR CODE TO PORT B

FIGURE 18. Flow Chart for Auto-Zero Routine

```
3D00    3E90      MVI 90
3D02    D3E7      Out Control Port                                     ; Program PPI
3D04    2601      MVI H 01              Auto-Zero Subroutine
3D06    7C        MOV A,H
3D07    D3E6      OUT C                                                ; Close SW1, open SW2
3D09    0680      MVI B 80                                             ; Initialize SAR bit pointer
3D0B    3E7F      MVI A 7F                                             ; Initialize SAR code
3D0D    4F        MOV C,A               Return
3D0E    D3E5      OUT B                                                ; Port B = SAR code
3D10    31AA3D    LXI SP 3DAA           Start                          ; Dimension stack pointer
3D13    D3E4      OUT A                                                ; Start A/D
3D15    FB        IE
3D16    00        NOP                   Loop                           ; Loop until INT asserted
3D17    C3163D    JMP Loop
3D1A    7A        MOV A,D               Auto-Zero
3D1B    C600      ADI 00
3D1D    CA2D3D    JZ Set C                                             ; Test A/D output data for zero
3D20    78        MOV A,B               Shift B
3D21    F600      ORI 00                                               ; Clear carry
3D23    1F        RAR                                                  ; Shift "1" in B right one place
3D24    FE00      CPI 00                                               ; Is B zero? If yes last
3D26    CA373D    JZ Done                                              ; approximation has been made
3D29    47        MOV B,A
3D2A    C3333D    JMP New C
3D2D    79        MOV A,C               Set C
3D2E    B0        ORA B                                                ; Set bit in C that is in same
3D2F    4F        MOV C,A                                              ; position as "1" in B
3D30    C3203D    JMP Shift B
3D33    A9        XRA C                 New C                          ; Clear bit in C that is in
3D34    C30D3D    JMP Return                                           ; same position as "1" in B
3D37    47        MOV B,A               Done                           ; then output new SAR code.
3D38    7C        MOV A,H                                              ; Open SW1, close SW2 then
3D39    EE03      XRI 03                                               ; proceed with program. Preamp
3D3B    D3E6      OUT C                                                ; is now zeroed.
3D3D                  .                 Normal
                      .
                      .
                  Program for processing
                  proper data values
3C3D    DBE4      IN A                  Read A/D Subroutine            ; Read A/D data
3C3F    EEFF      XRI FF                                               ; Invert data
3C41    57        MOV D,A
3C42    78        MOV A,B                                              ; Is B Reg = 0? If not stay
3C43    E6FF      ANI FF                                               ; in auto zero subroutine
3C45    C21A3D    JNZ  Auto-Zero
3C48    C33D3D    JMP  Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 19. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

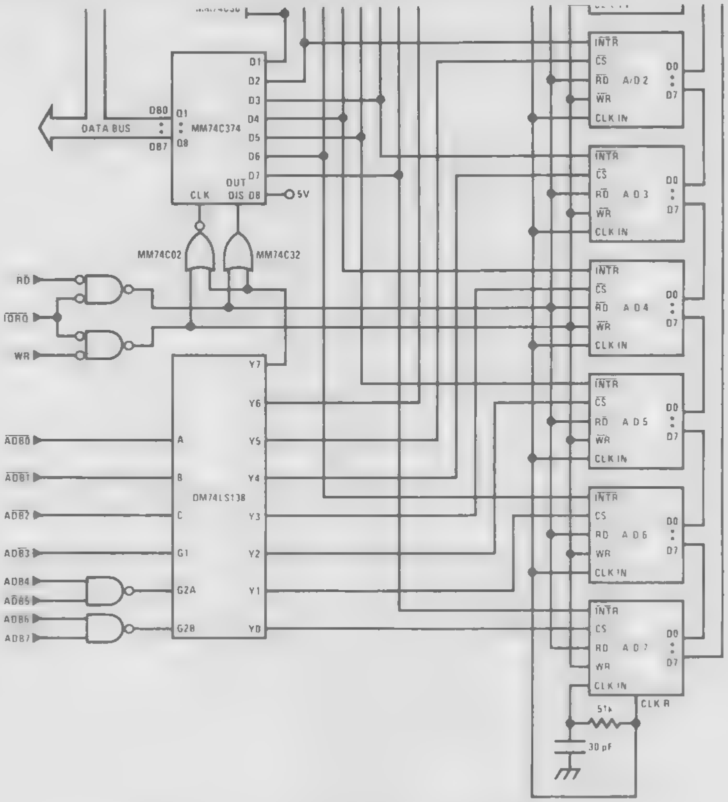


FIGURE 20. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

```
                                SOURCE
LOC     OBJ CODE                STATEMENT               COMMENT
0038    E5                      PUSH HL         ; Save contents of all registers affected by
0039    C5                      PUSH BC         ; this subroutine.
003A    F5                      PUSH AF         ; Assumed INT mode 1 earlier set.
003B    21 00 3E                LD (HL),X3E00   ; Initialize memory pointer where data will.be stored
003E    0E 01                   LD C,X01        ; C register will be port ADDR of A/D converters
0040    D300                    OUT X00,A       ; Load peripheral status word into 8-bit latch
0042    DB00                    IN A, X00       ; Load status word into accumulator
0044    47                      LD B,A          ; Save the status word
0045    79          TEST        LD A,C          ; Test to see if the status of all A/D's have
0046    FE 08                   CP, X08         ; been checked. If so, exit subroutine
0048    CA 60 00                JPZ, DONE
004B    78                      LD A,B          ; Test a single bit in status word by looking for
004C    1F                      RRA             ; a "1" to be rotated into the CARRY (an INT
004D    47                      LD B,A          ; is loaded as a "1"). If CARRY is set then load
004E    DA 5500                 JPC, LOAD       ; contents of A/D at port ADDR in C register.
0051    0C          NEXT        INC C           ; If CARRY is not set, increment C register to point
0052    C3 4500                 JP,TEST         ; to next A/D, then test next bit in status word.
0055    ED 78       LOAD        IN A, (C)       ; Read data from interrupting A/D and invert
0057    EE FF                   XOR FF          , the data
0059    77                      LD (HL),A       ; Store the data
005A    2C                      INC L
005B    71                      LD (HL),C       ; Store A/D identifier (A/D port ADDR)
005C    2C                      INC L
005D    C3 51 00                JP,NEXT         ; Test next bit in status word.
0060    F1          DONE        POP AF          ; Re-establish all registers as they were
0061    C1                      POP BC          ; before the interrupt.
0062    E1                      POP HL
0063    C9                      RET             ; Return to original program.
```

Section 4

CMOS Memory

National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different that the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

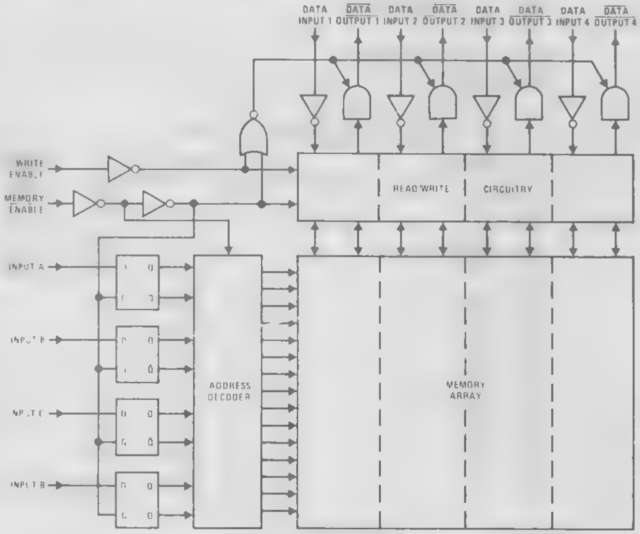
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

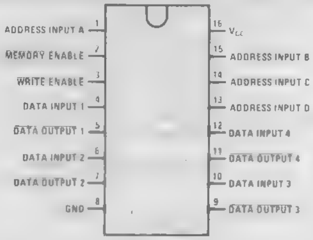
Features

Wide supply voltage range	3.0V to 15V
Guaranteed noise margin	1.0V
High noise immunity	0.45 V_{CC} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L
Low power consumption	100 nW/package (typ.)
Fast access time	130 ns (typ.) at V_{CC} = 10V
TRI-STATE output	

TRI-STATE is a registered trademark of National Semiconductor Corp.

Logic and Connection Diagrams





TOP VIEW

Order Number MM54C89D or MM74C89D
See Package 3
Order Number MM74C89N
See Package 15

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C89	$-55°C$ to $+125°C$
MM74C89	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		−0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
	Output Current in High Impedance State	$V_{CC}=15V$, $V=15V$		0.005	1.0	μA
		$V_{CC}=15V$, $V_O=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=+360\mu A$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50\,pF$, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay from Memory Enable	$V_{CC}=5.0V$		270	500	ns
		$V_{CC}=10V$		100	220	ns
t_{ACC}	Access Time from Address Input	$V_{CC}=5.0V$		350	650	ns
		$V_{CC}=10V$		130	280	ns
t_{SA}	Address Setup Time	$V_{CC}=5.0V$	150			ns
		$V_{CC}=10V$	60			ns
t_{HA}	Address Hold Time	$V_{CC}=5.0V$	60			ns
		$V_{CC}=10V$	40			ns
t_{ME}	Memory Enable Pulse Width	$V_{CC}=5.0V$	400	250		ns
		$V_{CC}=10V$	150	90		ns
t_{ME}	Memory Enable Pulse Width	$V_{CC}=5.0V$	400	200		ns
		$V_{CC}=10V$	150	70		ns

AC Electrical Characteristics (Cont'd.)

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{SR}	Write Enable Setup Time	$V_{CC} = 5.0V$	0			ns
	for a Read	$V_{CC} = 10V$	0			ns
t_{WS}	Write Enable Setup Time	$V_{CC} = 5.0V$			t_{ME}	ns
	for a Write	$V_{CC} = 10V$			t_{ME}	ns
t_{WE}	Write Enable Pulse Width	$V_{CC} = 5.0V, t_{WS} = 0$	300	160		ns
		$V_{CC} = 10V, t_{WS} = 0$	100	60		ns
t_{HD}	Data Input Hold Time	$V_{CC} = 5.0V$	50			ns
		$V_{CC} = 10V$	25			ns
t_{SD}	Data Input Setup	$V_{CC} = 5.0V$	50			ns
		$V_{CC} = 10V$	25			ns
t_{IH}, t_{OH}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	$V_{CC} = 5.0V, C_L = 5.0pF, R_L = 10k$		180	300	ns
		$V_{CC} = 10V, C_L = 5.0pF, R_L = 10k$		85	120	ns
t_{IH}, t_{OH}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	$V_{CC} = 5.0V, C_L = 5.0pF, R_L = 10k$		180	300	ns
		$V_{CC} = 10V, C_L = 5.0pF, R_L = 10k$		85	120	ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity	Any Output (Note 2)		6.5		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics (Guaranteed across the specified temperature range, $C_L = 50pF$) (cont'd)

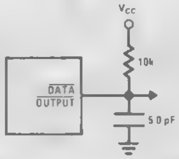
Parameter	Conditions	MM54C89 $T_A = 55°C$ to $+125°C$		MM74C89 $T_A = -45°C$ to $+85°C$		Units
		Min.	Max.	Min.	Max.	
t_{PD}	$V_{CC} = 5.0V$		700		600	ns
	$V_{CC} = 10V$		310		265	ns
	$V_{CC} = 15V$		250		210	ns
t_{ACC}	$V_{CC} = 5.0V$		910		780	ns
	$V_{CC} = 10V$		400		345	ns
	$V_{CC} = 15V$		320		270	ns
t_{SA}	$V_{CC} = 5.0V$	210		180		ns
	$V_{CC} = 10V$	90		80		ns
	$V_{CC} = 15V$	70		60		ns
t_{HA}	$V_{CC} = 5.0V$	80		70		ns
	$V_{CC} = 10V$	55		50		ns
	$V_{CC} = 15V$	45		40		ns
t_{ME}	$V_{CC} = 5.0V$	560		480		ns
	$V_{CC} = 10V$	210		180		ns
	$V_{CC} = 15V$	170		150		ns
t_{ME}	$V_{CC} = 5.0V$	560		480		ns
	$V_{CC} = 10V$	210		180		ns
	$V_{CC} = 15V$	170		150		ns
t_{WE}	$V_{CC} = 5.0V$	420		360		ns
	$V_{CC} = 10V$	140		120		ns
	$V_{CC} = 15V$	110		100		ns
t_{HD}	$V_{CC} = 5.0V$	70		60		ns
	$V_{CC} = 10V$	35		30		ns
	$V_{CC} = 15V$	30		25		ns
t_{SA}	$V_{CC} = 5.0V$	70		60		ns
	$V_{CC} = 10V$	35		30		ns
	$V_{CC} = 15V$	30		25		ns
t_{IH}, t_{OH}	$V_{CC} = 5.0V$		420		360	ns
	$V_{CC} = 10V, C_L = 5.0pF$		170		145	ns
	$V_{CC} = 15V, R_L = 10k\Omega$		135		115	ns

Truth Table

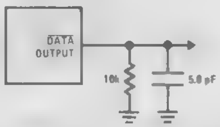
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE®
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE®
H	H	Inhibit, Storage	TRI-STATE®

AC Test Circuit

t_{0H}

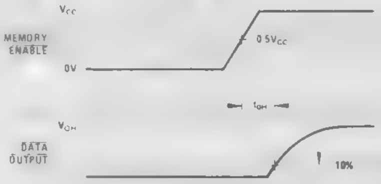


t_{1H}

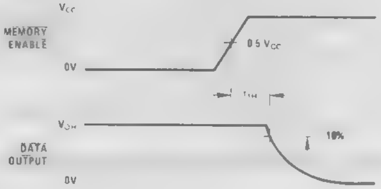


Switching Time Waveforms

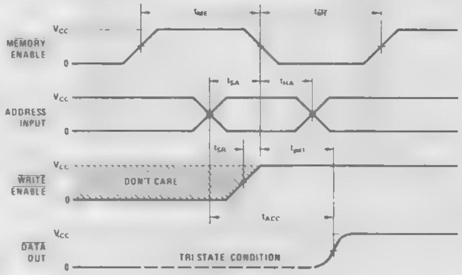
t_{0H}



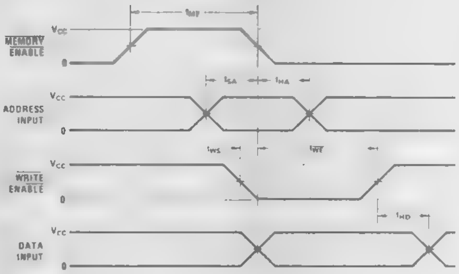
t_{1H}



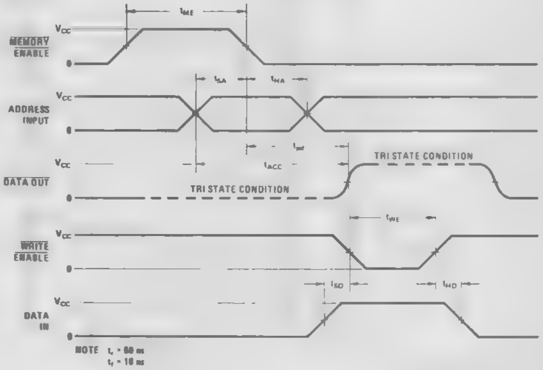
Read Cycle



Write Cycle



Read Modify Write Cycle



National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE® data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

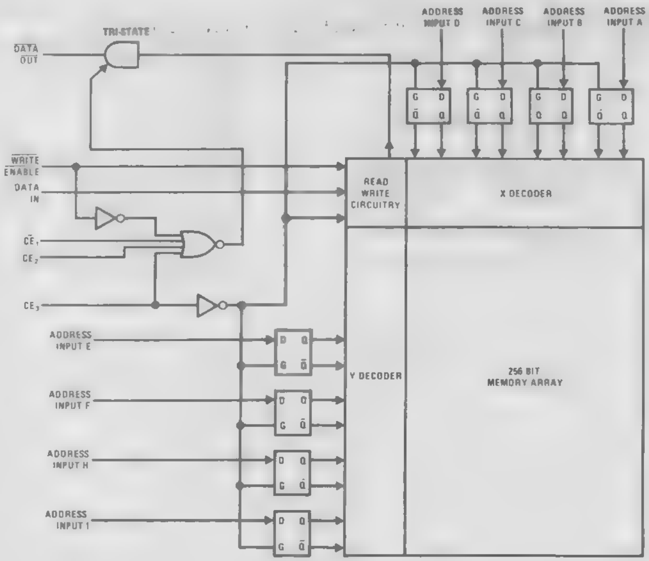
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

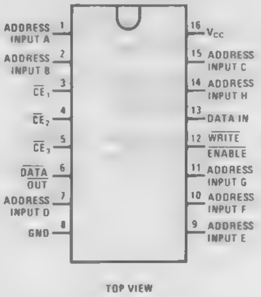
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	$0.45\ V_{CC}$ (typ.)
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW (typ.)
■ Internal address register	

TRI-STATE is a registered trademark of National Semiconductor Corp.

Logic and Connection Diagrams





Order Number MM54C200D or MM74C200D
See Package 3
Order Number MM74C200N
See Package 15

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC} + 0.3\,V$
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min./max. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$	3.5			V
		$V_{CC} = 10\,V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$			1.5	V
		$V_{CC} = 10\,V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\,\mu A$	4.5			V
		$V_{CC} = 10\,V$, $I_O = -10\,\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = +10\,\mu A$			0.5	V
		$V_{CC} = 10\,V$, $I_O = +10\,\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.10	600	μA
	CMOS/TTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$	$V_{CC} - 1.5$			V
		74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$			0.8	V
		74C $V_{CC} = 4.75\,V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -1.6\,mA$	2.4			V
		74C $V_{CC} = 4.75$, $I_O = -1.6\,mA$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 1.6\,mA$				
		74C $V_{CC} = 4.75$, $I_O = 1.6\,mA$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = 0\,V$	−4.0	−6.0		mA
		$T_A = 25°C$	−1.8			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10\,V$, $V_{OUT} = 0\,V$	−16.0	−25		mA
		$T_A = 25°C$	−1.5			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	5.0	8.0		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10\,V$, $V_{OUT} = V_{CC}$ $T_A = °C$	20	30		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{ACC}	Access Time from Address	$V_{CC} = 5.0V$		450	900	ns
		$V_{CC} = 10V$		200	400	ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5.0V$		360	700	ns
		$V_{CC} = 10V$		120	300	ns
t_{pCE1}	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5.0V$		250	700	ns
		$V_{CC} = 10V$		85	200	ns
t_{SA}	Address Setup Time	$V_{CC} = 5.0V$	200	80		ns
		$V_{CC} = 10V$	100	30		ns
t_{HA}	Address Hold Time	$V_{CC} = 5.0V$	50	15		ns
		$V_{CC} = 10V$	25	5.0		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5.0V$	300	160		ns
		$V_{CC} = 10V$	150	70		ns
t_{CE}	$\overline{CE}_3$ Pulse Widths	$V_{CC} = 5.0V$	400	200		ns
		$V_{CC} = 10V$	160	80		ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity in TRI-STATE®	(Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		400		pF

$C_L = 50\,pF$

Parameter		Conditions	MM54C200 $T_A = -55°C$ to $+125°C$		MM74C200 $T_A = -45°C$ to $+85°C$		Units
			Min.	Max.	Min.	Max.	
t_{ACC}	Access Time from Address	$V_{CC} = 5.0V$		1200		1100	ns
		$V_{CC} = 10V$		520		480	ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5.0V$		950		850	ns
		$V_{CC} = 10V$		400		360	ns
$t_{pd\overline{CE1}}$	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5.0V$		650		600	ns
		$V_{CC} = 10V$		300		275	ns
t_{SA}	Address Setup Time	$V_{CC} = 5.0V$	250		250		ns
		$V_{CC} = 10V$	120		120		ns
t_{HA}	Address Hold Time	$V_{CC} = 5.0V$	100		100		ns
		$V_{CC} = 10V$	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5.0V$	450		400		ns
		$V_{CC} = 10V$	225		200		ns
t_{CE}	Disable Pulse Width	$V_{CC} = 5.0V$	500		460		ns
		$V_{CC} = 10V$	250		230		ns
t_{HD}	Data Hold Time	$V_{CC} = 5.0V$	50		50		ns
		$V_{CC} = 10V$	25		25		ns

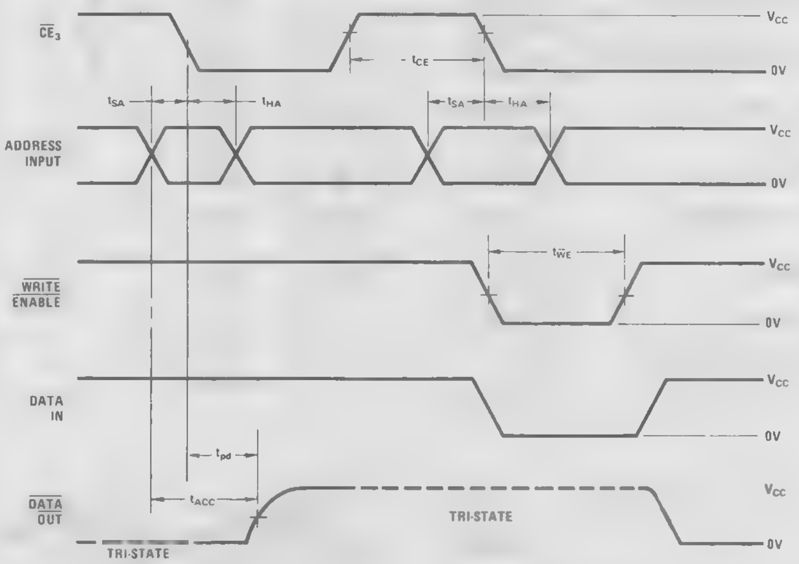
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

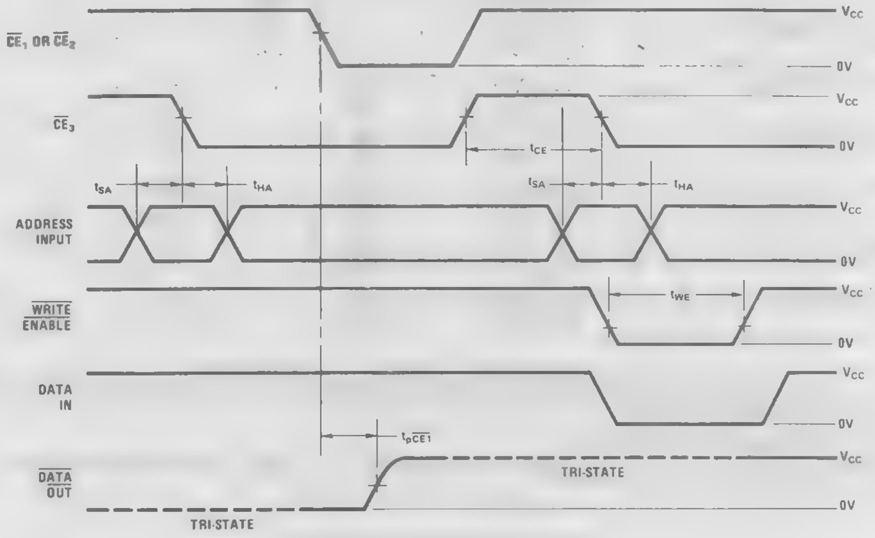
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Switching Time Waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

National Semiconductor

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE® outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

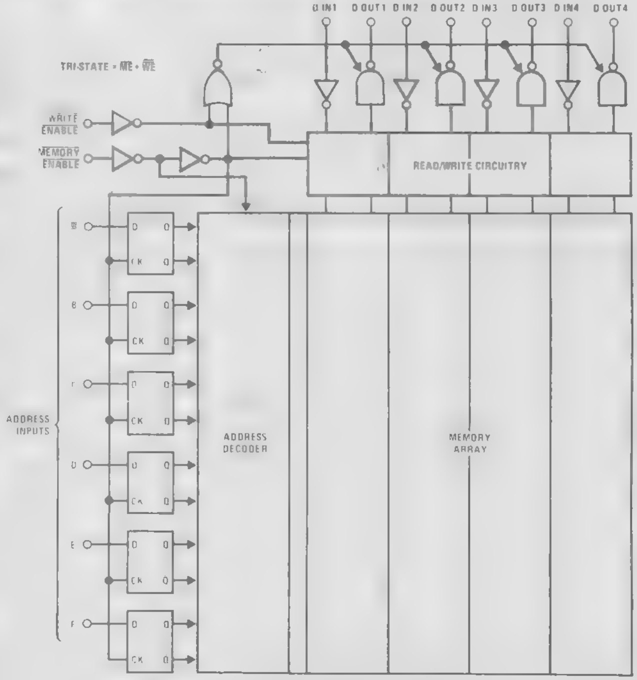
TRI-STATE is a registered trademark of National Semiconductor Corp.

Outputs are in the TRI-STATE® (Hi-Z) condition when the device is writing or disabled.

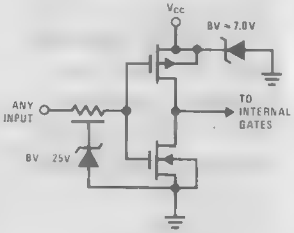
Features

Supply voltage range	3.0 V to 5.5 V
High noise immunity	0.45 V_{CC} (typ.)
TTL compatible fan out	1 TTL load
Input address register	
Low power consumption	250 nW/package (typ.) (chip enabled or disabled)
Fast access time	250 ns (typ.) at 5.0 V
TRI-STATE outputs	
High voltage inputs	

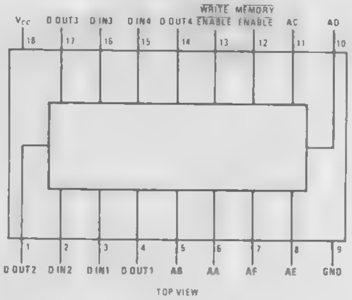
Logic and Connection Diagram



Input Protection



Dual-In-Line Package



Absolute Maximum Ratings (Note 1)

Voltage at any Output Pin	−0.3 V to V_{CC} + 0.3 V
Voltage at any Input Pin	−0.3 V to +15 V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 5.5 V
Standby V_{CC} Range	1.5 V to 5.5 V
Absolute Maximum V_{CC}	6.0 V
Lead Temperature (Soldering, 10 seconds(	300°C

Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

DC Electrical Characteristics

Min./max. limits apply across the temperature and power supply range indicated

Parameter		Conditions	Min.	Typ.	Max.	Units
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15 V V_{IN} = 5.0 V		0.005 0.005	2.0 1.0	μA μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0 V	−1.0	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150 μA I_O = −400 μA	V_{CC} − 0.5 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
	Output Current in High Impedance State	V_O = 5.0 V V_O = 0 V	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	V_{CC} = 5.0 V		5.0	300	μA

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0 V$, $C_L = 50 pF$

Parameter			Min.	Typ.	Max.	Units
t_{ACC}	Access Time from Address			250	500	ns
t_{pd}	Propagation Delay from $\overline{ME}$			180	360	ns
t_{SA}	Address Input Set-Up Time		140	70		ns
t_{HA}	Address Input Hold Time		20	10		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width		200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width		400	200		ns
t_{SD}	Data Input Set-Up Time		0			ns
t_{HD}	Data Input Hold Time		30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width		140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE® (Note 4)			100	200	ns
	Capacitance					
C_{IN}	Input Capacity Any Input (Note 2)			5.0		pF
C_{OUT}	Output Capacity Any Output (Note 2)			9.0		pF
C_{PD}	Power Dissipation Capacity (Note 3)			350		pF

AC Electrical Characteristics (cont'd) $C_L = 50\,pF$

Parameter		MM54C910 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5\,V$ to $5.5\,V$		MM74C910 $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.75\,V$ to $5.25\,V$		Units
		Min.	Max.	Min.	Max.	
t_{ACC}	Access Time from Address		860		700	ns
t_{pd1}, t_{pd0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE® (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

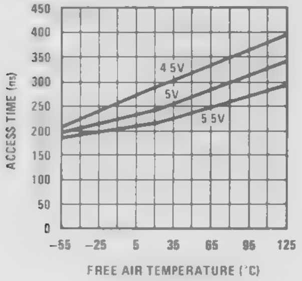
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Note 4: See AC test circuit for t_{1H}, t_{0H}.

Typical Performance Characteristics

Typical Access Time vs Ambient Temperature

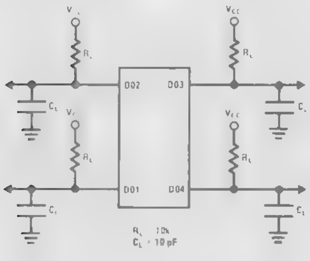


Truth Table

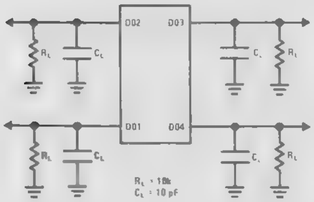
$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

AC Test Circuit

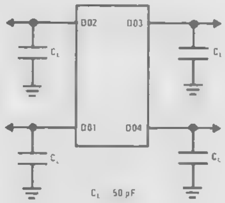
t_{0H}



t_{1H}

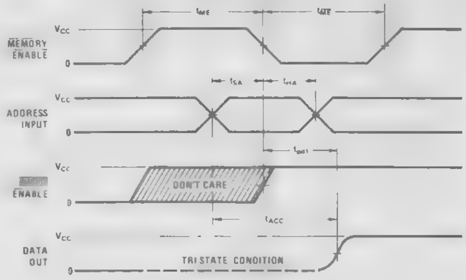


All Other AC Tests

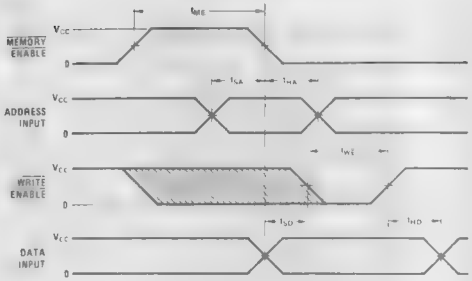


Switching Time Waveforms

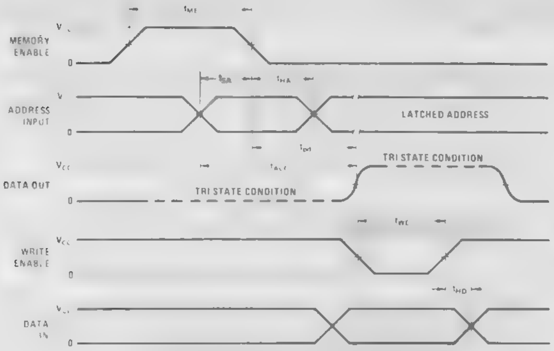
Read Cycle
(See Note 1)



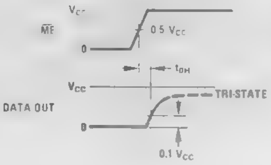
Write Cycle
(See Note 1)



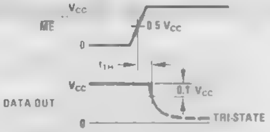
Read Modify Write Cycle
(See Note 1)



t_{0H}



t_{1H}



Note 1. $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} nanoseconds between every address change

Note 2. $t_r = t_f = 20$ ns for all inputs

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

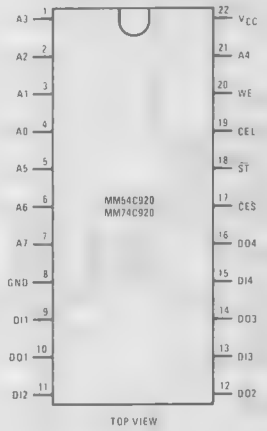
Complete address decoding as well as 2-chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

Features

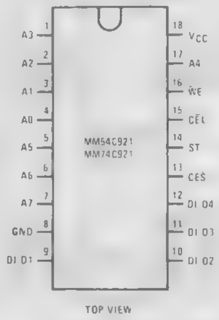
- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C920-3, MM74C921-3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V_{CC} as low as 2V

Connection Diagrams

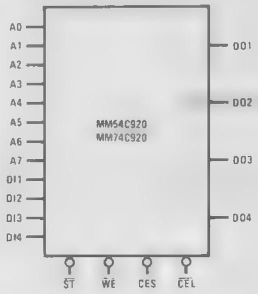
Dual-In-Line Package

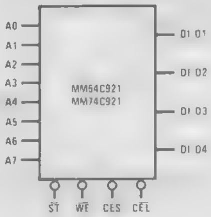


Dual-In-Line Package



Logic Symbols





Functional Description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1.* Input addresses and $\overline{\text{CES}}$ are clocked into the input latches by the falling edge of $\overline{\text{STROBE}}$. Input set-up and hold times must be observed on these signals (see timing diagrams). The true-and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

The addressed word (4 bits) is fed to 4 sense amplifiers through the column decoders. The information from the sense amplifiers is latched into the output register when $\overline{\text{STROBE}}$ rises. The register drives the TRI-STATE® output buffers.

Chip select inputs, $\overline{\text{CEL}}$ and $\overline{\text{CES}}$, have identical functions except that $\overline{\text{CES}}$ (Chip Enable Stored) is clocked into a latch on the falling edge of $\overline{\text{STROBE}}$; $\overline{\text{CEL}}$ (Chip Enable Level) is not.

Note that set-up and hold times must be observed on $\overline{\text{CES}}$. Because $\overline{\text{CEL}}$ is not clocked by $\overline{\text{STROBE}}$, it may fall after $\overline{\text{STROBE}}$ has fallen without affecting access time provided that the t_{OE} requirement is met.

The outputs are in a high impedance state when the chip is not selected ($\overline{\text{CES}}$ or $\overline{\text{CEL}}$ high) or when writing ($\overline{\text{WE}}$ low). Note that the information stored in the output latches will be changed whenever $\overline{\text{STROBE}}$ falls, regardless of the logic states of $\overline{\text{WE}}$, $\overline{\text{CEL}}$ or $\overline{\text{CES}}$.

The switching time waveforms in *Figures 2, 3 and 4* define the read, write, and output enable/disable parameters respectively.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, $\overline{\text{ST}}$ logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*

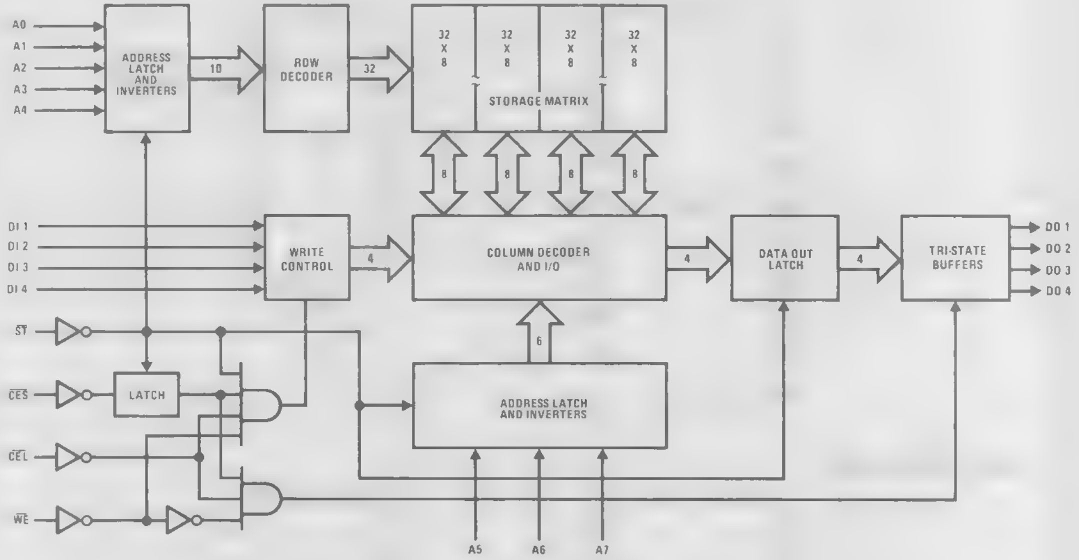


FIGURE 1. MM54C920/MM74C920

*The logic diagram for the MM54C921/MM74C921 is identical to this except that data inputs (DI1–DI4) are connected to data outputs (DO1–DO4).

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C920, MM54C921	4.5	5.5	V
MM74C920, MM74C921	4.5	5.5	V
MM74C920-3, MM74C921-3	4.75	5.25	V
Ambient Temperature (T_A)			
MM54C920, MM54C921	−55	+125	°C
MM74C920, MM74C921	−40	+85	C
MM74C920-3, MM74C921-3	0	+70	C

DC Electrical Characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920–3, MM74C921-3		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC} 2.0	V_{CC}	V_{CC} 2.0	V_{CC}	V_{CC} 1.5	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC} 0.1		V_{CC} 0.1		V_{CC} 0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	-1.0	1.0	1.0	1.0	1.0	1.0	µA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, CEL V_{CC}	-1.0	1.0	1.0	1.0	-1.0	1.0	µA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, V_O = 0V		20		10		100	µA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	$\overline{CEL} = V_{CC}$ = 2V, Typical at 25°C		0.01 (typ)		0.01 (typ)		0.1 (typ)	µA

Capacitance (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		4	7	pF
C_O	Output Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values above which the device may be permanently damaged. They do not mean the device may be operated at these values.

Note 2: These limits apply over the entire operating range specified in the "Operating Conditions" unless otherwise stated.

Note 3: $\overline{CEL} = V_{CC}$ − 2V or = 2V, whichever is greater.

Note 4: Capacitance is guaranteed by periodic testing.

Truth Table

$\overline{ST}$	$\overline{CES}$*	$\overline{CEL}$	$\overline{WE}$	DI*	FUNCTION
X	X	1	X	X	Output in Hi-Z state
0	1	X	X	X	Output in Hi-Z state
X	X	X	0	X	Output in Hi-Z state
0	0	0	0	0	Write "0", output in Hi-Z state
0	0	0	0	1	Write "1", output in Hi-Z state
0	0	0	1	X	Read data, output enabled

*Set-up and hold times must be met

X = don't care

AC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920–3 MM74C921–3		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		275		250		325	ns
t_{ACS}	Access Time From Strobe		250		225		300	ns
t_{AS}	Address Set-Up Time	25		25		25		ns
t_{AH}	Address Hold Time	25		25		25		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150		130		165		ns
t_{ST}	ST Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time	100		90		90		ns
t_{DH}	Data Hold Time	60		60		60		ns

Note 5: These limits apply over the operating range specified in the "Operating Conditions" with $t_{RISE} = t_{FALL} = 5$ ns, load = 1 TTL gate + 50 pF.

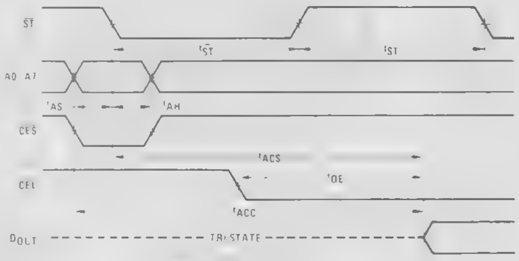
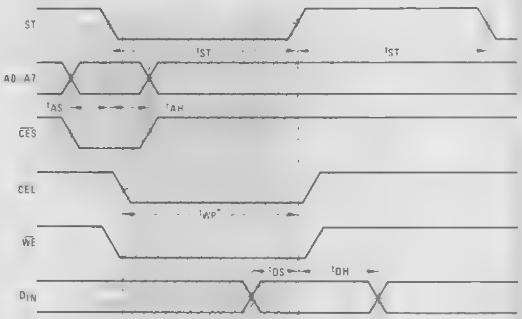


FIGURE 2. Read Cycle ($\overline{WE} = V_{IH}$)



*t_{WP} (the Write Pulse Width) is the time $\overline{ST}$, $\overline{CEL}$ and $\overline{WE}$ are coincidentally low

FIGURE 3. Write Cycle

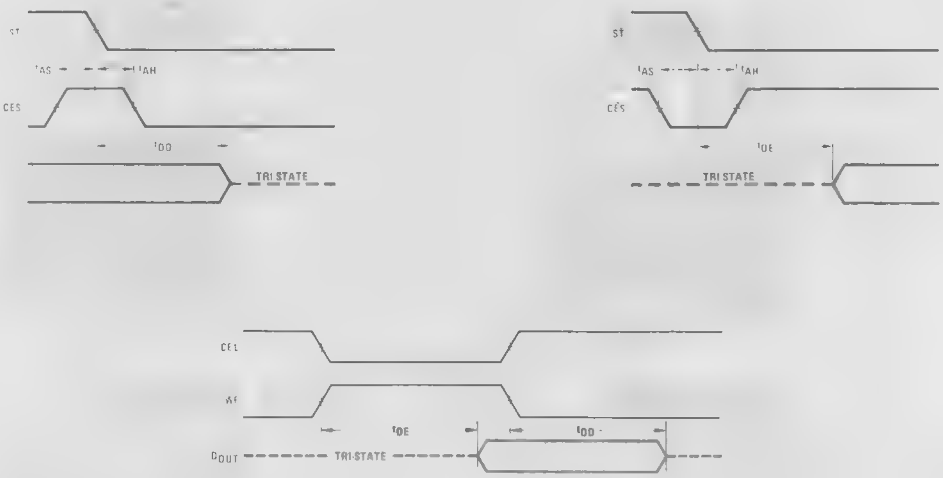
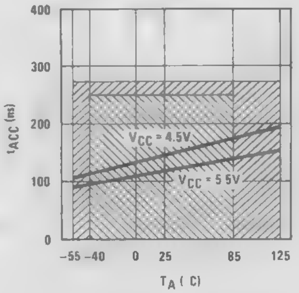


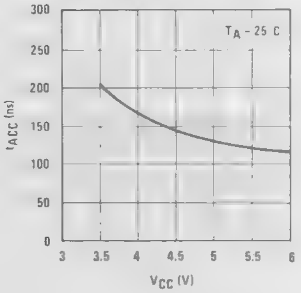
FIGURE 4. Output Enable/Disable

Typical Performance Characteristics

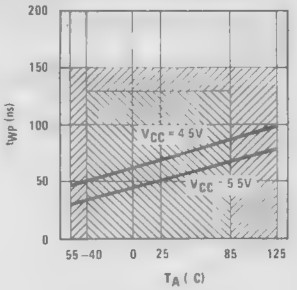
Access Time vs Ambient Temperature



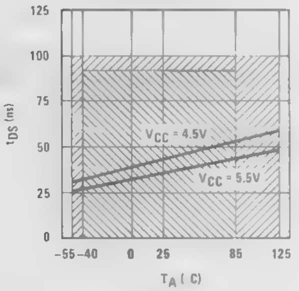
Access Time vs Power Supply Voltage



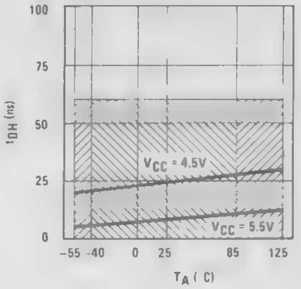
Minimum Write Pulse Width vs Ambient Temperature



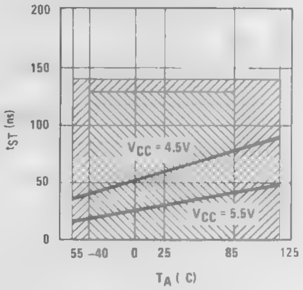
Data-In Setup Time vs Ambient Temperature



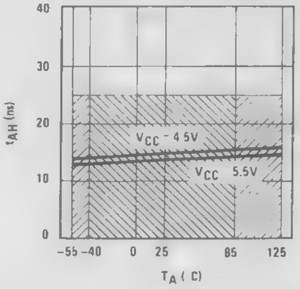
Data In Hold Time vs Ambient Temperature



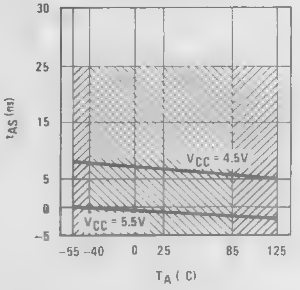
Minimum ST Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

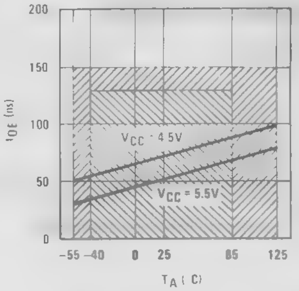


Address Setup Time vs Ambient Temperature

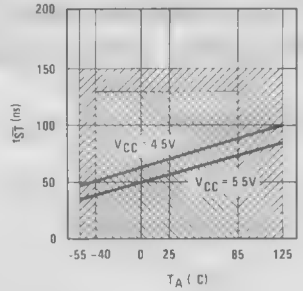


Typical Performance Characteristics (Continued)

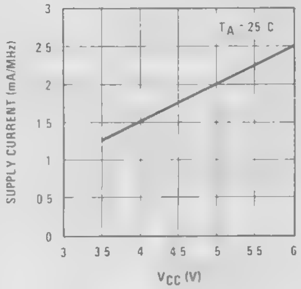
Output Enable Time vs Ambient Temperature



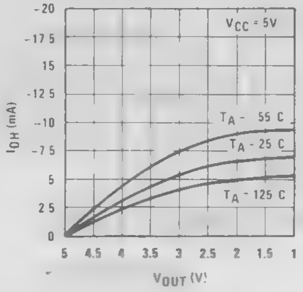
Minimum $\overline{ST}$ Pulse Width (Negative) vs Ambient Temperature



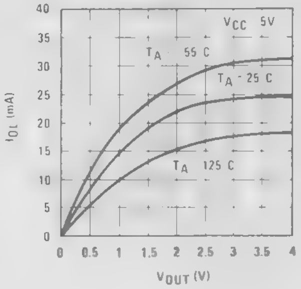
Dynamic Current vs Power Supply Voltage (V_{IH} = V_{CC}, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



▨ Test Limit MM54C920, MM54C921

▨ Test Limit MM74C920, MM74C921

National Semiconductor

MM54C929/MM74C929, MM54C930/MM74C930 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 x 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{\text{CS1}}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{\text{CS1}}$, $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ are internally connected together, providing a single chip-select input $\overline{\text{CS}}$.

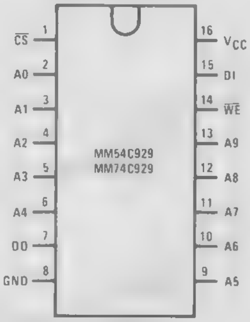
Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, minicomputer and main-frame-memory applications.

Features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10 μA max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

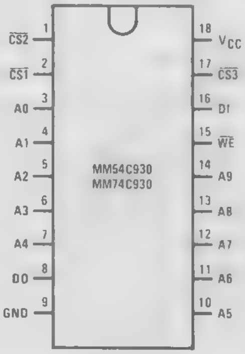
Connection Diagrams

Dual-In-Line Package



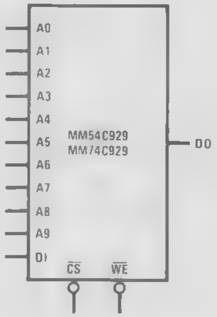
TOP VIEW

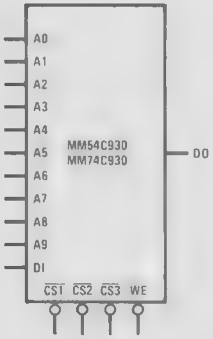
Dual-In-Line Package



TOP VIEW

Logic Symbols





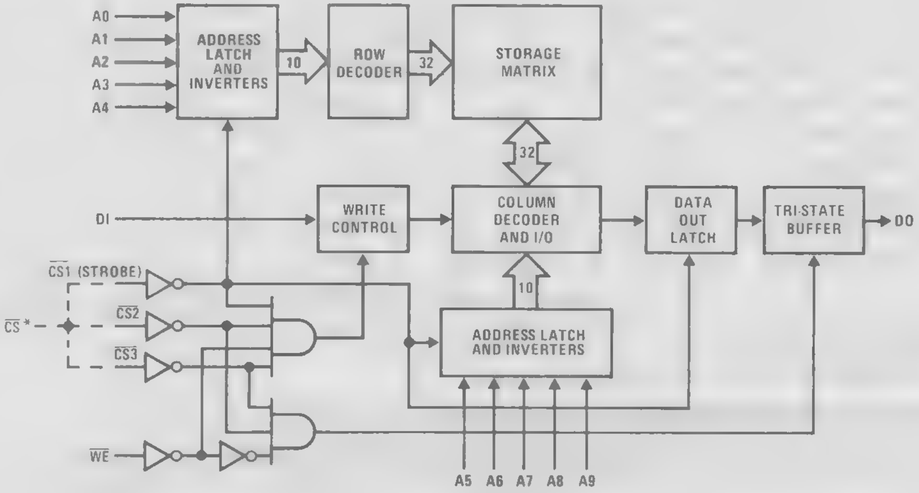
Functional Description

Address inputs are clocked into the input latches by the falling edge of chip strobe $\overline{\text{CS1}}$; set-up and hold times must be observed on these input signals (see timing diagram). The true and complement address information is fed to the row and column decoders which select one of the 1024-bit locations. The addressed bit is fed, via a sense amplifier, to the output register and TRI-STATE® buffer. The information is latched into the output register on the rising edge of chip strobe $\overline{\text{CS1}}$. The output is in a high impedance state when the chip is not selected ($\overline{\text{CS2}}$ or $\overline{\text{CS3}}$ high) or when writing ($\overline{\text{WE}}$ low). Output buffer control is independent of chip strobe $\overline{\text{CS1}}$.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, strobe ($\overline{\text{CS}}$ for the MM74C929 and $\overline{\text{CS1}}$ for the MM74C930) logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*



*The MM74C930 has 3 chip selects $\overline{\text{CS1}}$, $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$. The MM74C929 has these internally connected together providing a single chip select input $\overline{\text{CS}}$.

FIGURE 1

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	–0.3V to V_{CC} + 0.3V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
MM54C929, MM54C930	–55°C to +125°C
MM74C929, MM74C930	–40°C to +85°C
MM74C929-3, MM74C930-3	0°C to +70°C
Package Dissipation	500 mW
Lead Temperature (Soldering 10 seconds)	300°C

DC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		$V_{CC}-2.0$	V_{CC}	V_{CC} 2.0	V_{CC}	V_{CC} 2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = 1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	$V_{CC}-0.1$		$V_{CC}-0.1$		$V_{CC}-0.1$		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2.0 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	1.0	1.0	1.0	1.0	1.0	1.0	µA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, (Note 2)	-1.0	1.0	–1.0	1.0	1.0	1.0	µA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, V_O = 0V		20		10		100	µA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	V_{CC} = 2V, T_A = 25°C, (Note 2)		0.01 (typ)		0.01 (typ)		0.1 (typ)	µA

Note 1: V_{CC} = 5V ±5%.

Note 2: $\overline{CS2} = \overline{CS3} = V_{CC}$ or $\overline{CS} = V_{CC}$.

Note 3: $\overline{CS2}$ or $\overline{CS3}$ or $\overline{CS} = V_{CC} - 2V$ or = 2V, whichever is greater.

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

TTL Interface ($V_{IH} = V_{CC} - 2V$, V_{IL} = 0.8V, Input $t_{RISE} = t_{FALL}$ = 5 ns, Load = 1 TTL Gate + 50 pF)

SYMBOL	PARAMETER	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		265		240		315	ns
t_{ACS}, t_{ACS1}	Access Time From $\overline{CS}$, $\overline{CS1}$		250		225		300	ns
t_{AS}	Address Set-Up Time	15		15		15		ns
t_{AH}	Address Hold Time	50		50		50		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{CS}}, t_{\overline{CS1}}$ (Note 4)	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Negative)	150		130		165		ns
t_{CS}, t_{CS1}	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time, (Note 5)	150		140		140		ns
t_{DH}	Data Hold Time, (Note 5)	0		0		0		ns

Note 4: Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation.

Note 5: t_{DS} and t_{DH} are referenced to the low-to-high transition of $\overline{CS1}$ or $\overline{CS2}$ or $\overline{CS3}$ or $\overline{WE}$, whichever switches first, for the MM54C930/MM74C930 and are referenced to the $\overline{CS}$ or $\overline{WE}$ low-to-high transition, whichever switches first, for the MM54C929/MM74C929.

Capacitance (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
C_{IN}	Input Capacitance	$V_{IN} = 0$, f = 1 MHz, $T_A = 25°C$	4	7	pF
C_O	Output Capacitance	$V_{IN} = 0$, f = 1 MHz, $T_A = 25°C$	6	9	pF
$C_{\overline{CS}}$	Chip Select Capacitance	MM54C929/MM74C929, MM74C929-3	8	12	pF

Note 6: Capacitance maximum is guaranteed by periodic testing.

Truth Tables

MM54C929/MM74C929

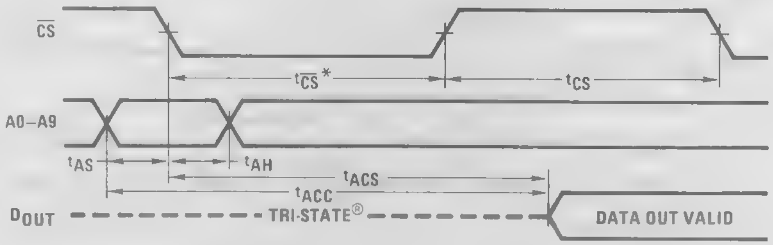
$\overline{CS}$	$\overline{WE}$	DI	FUNCTION
1	X	X	Output in Hi-Z State
X	0	X	Output in Hi-Z State
0	0	0	Write "0," Output in Hi-Z State
0	0	1	Write "1," Output in Hi-Z State
0	1	X	Read Data, Output Enabled

X = Don't care

MM54C930/MM74C930

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	DI	FUNCTION
X	1	X	X	X	Output in Hi-Z State
X	X	1	X	X	Output in Hi-Z State
X	X	X	0	X	Output in Hi-Z State
0	0	0	0	0	Write "0," Output in Hi-Z State
0	0	0	0	1	Write "1," Output in Hi-Z State
0	0	0	1	X	Read Data, Output Enabled

Switching Time Waveforms



*Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation, *(Figure 4a)*.

FIGURE 2a. MM54C929/MM74C929 Read Cycle

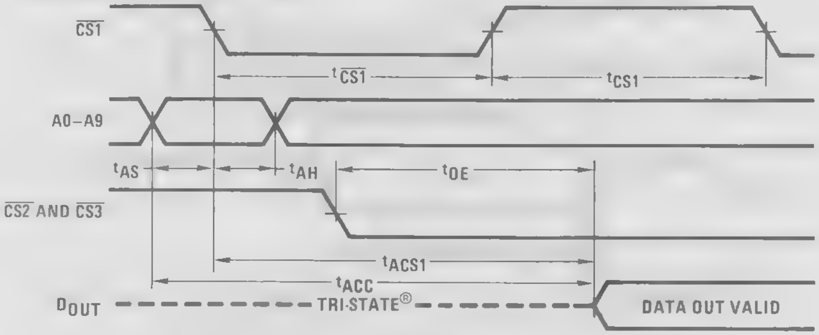
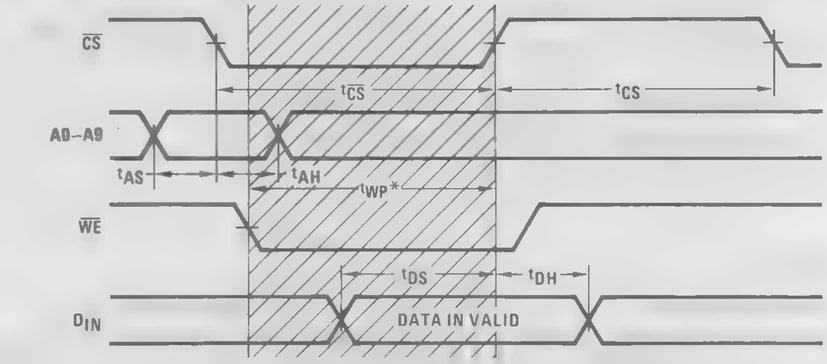


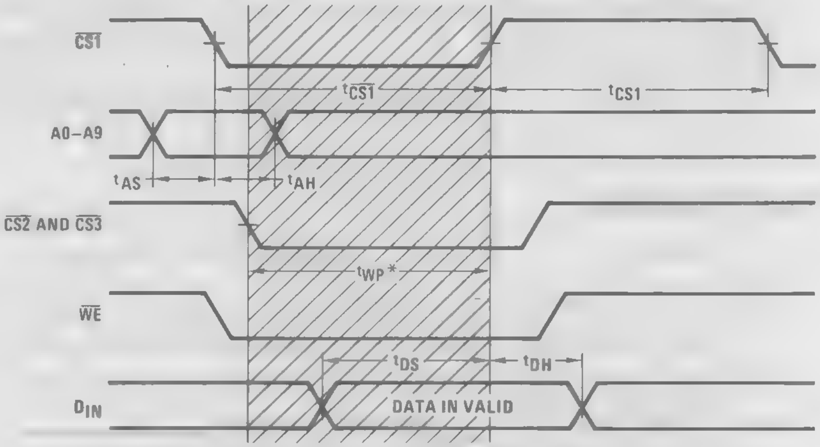
FIGURE 2b. MM54C930/MM74C930 Read Cycle

Switching Time Waveforms (Continued)



*tWP (the Write Pulse width) is the time CS and WE are coincidentally low

FIGURE 3a. MM54C929/MM74C929 Write Cycle



*tWP (the Write Pulse width) is the time CS1, CS2, CS3 and WE are coincidentally low

FIGURE 3b. MM54C930/MM74C930 Write Cycle

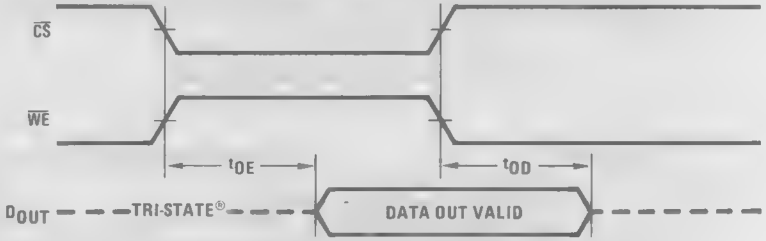


FIGURE 4a. MM54C929/MM74C929

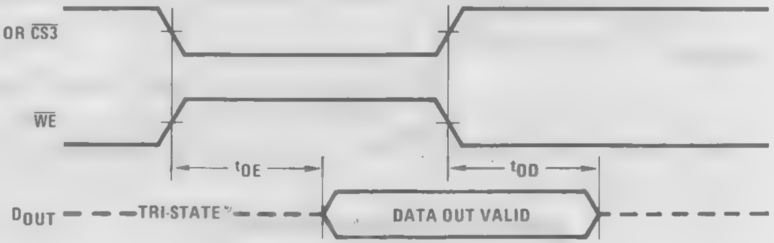
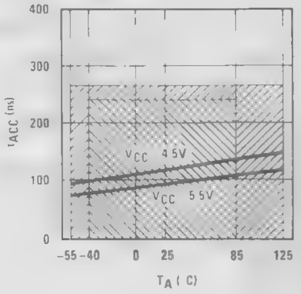
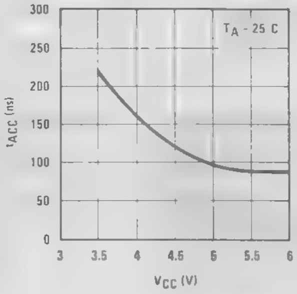
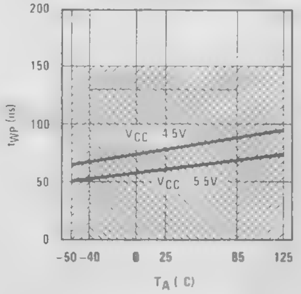


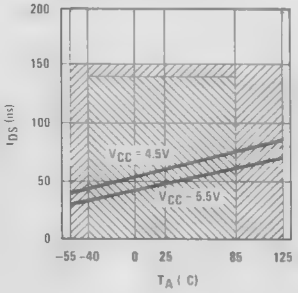
FIGURE 4b. MM54C930/MM74C930

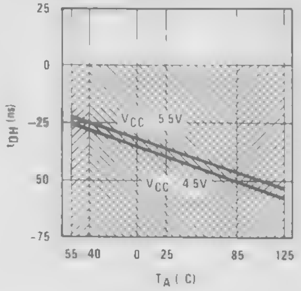
Typical Performance Characteristics

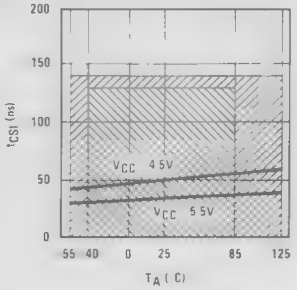

Access Time vs Ambient Temperature

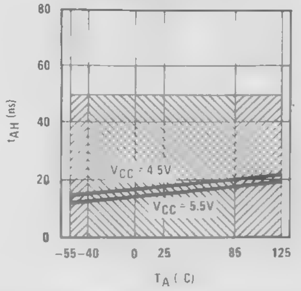

Access Time vs Power Supply Voltage

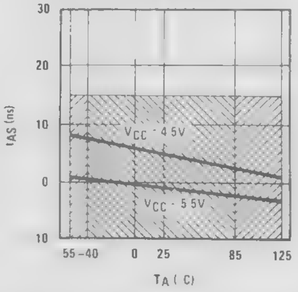

Minimum Write Pulse Width vs Ambient Temperature


Data-In Set-Up Time vs Ambient Temperature


Data-In Hold Time vs Ambient Temperature

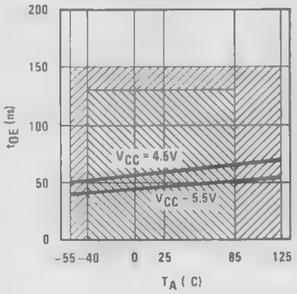

Minimum $\overline{CSI}$ Pulse Width (Positive) vs Ambient Temperature


Address Hold Time vs Ambient Temperature

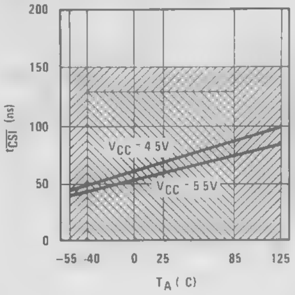

Address Set-Up Time vs Ambient Temperature

Typical Performance Characteristics (Continued)

Output Enable Time vs Ambient Temperature



Minimum $\overline{CS1}$ Pulse Width (Negative) vs Ambient Temperature



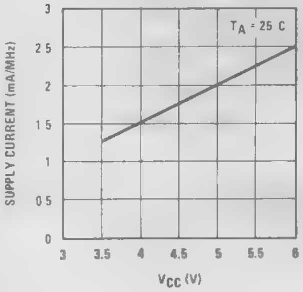
Test Limit MM54C929, MM54C930

▨

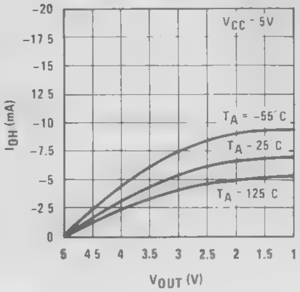
Test Limit MM74C929, MM74C930

▨

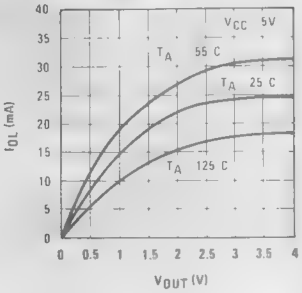
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



National Semiconductor

MM54C989/MM74C989 64-Bit (16 × 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines, a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note. The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

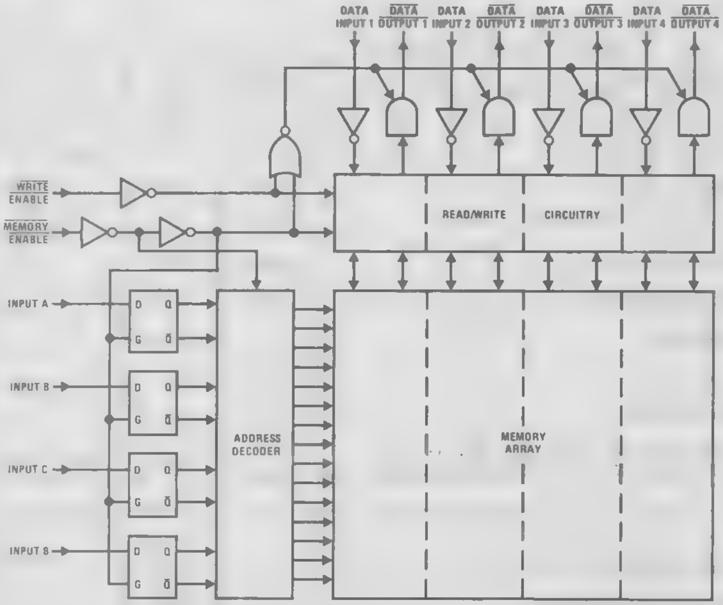
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE® (Hi-Z) condition.

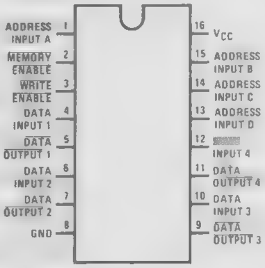
Features

■ Wide supply voltage range	3.0V to 5.5V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Input address register	
■ Low power consumption	250 nW/package (typ.) @ V_{CC} = 5V
■ Fast access time	140 ns (typ.) at V_{CC} = 5V
■ TRI-STATE output	

Logic and Connection Diagrams



Dual-in-Line Package



TOP VIEW

Order Number MM54C989J
or MM74C989J
See NS Package J16A

Order Number MM74C989N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3\text{V}$
Package Dissipation	500 mW
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C
Operating V_{CC} Range			3.0V to 5.5V
Standby V_{CC} Range			1.5V to 5.5V

DC Electrical Characteristics MM54C989/MM74C989

(Min/max limits apply across the temperature and power supply range indicated).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5\text{V}$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0$	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\,\mu\text{A}$	2.4			V
		$I_O = -150\,\mu\text{A}$	$V_{CC}-0.5$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 360\,\mu\text{A}$			0.4	V
	Output Current in High Impedance State	$V_O = 5\text{V}$		0.005	1	μA
		$V_O = 0$	−1	−0.005		μA
I_{CC}	Supply Current (Active)	$\overline{ME} = 0$, $V_{CC} = 5\text{V}$		0.05	150	μA
	Supply Current (Stand-By)	$\overline{ME} = 5\text{V}$			3	μA

AC Electrical Characteristics MM54C989/MM74C989

$T_A = 25°\text{C}$, $V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$

PARAMETER		MIN	TYP	MAX	UNITS
t_{ACC}	Access Time From Address		140	500	ns
t_{PD}	Propagation Delay From $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	80		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE®, $C_L = 5\text{ pF}$, $R_L = 10\text{k}$, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

AC Electrical Characteristics

	PARAMETER	MM54C989		MM74C989		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time From Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay From $\overline{ME}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE®, (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

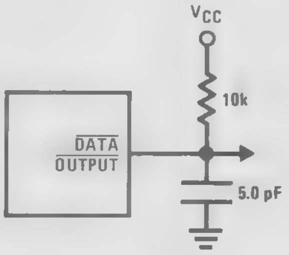
Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

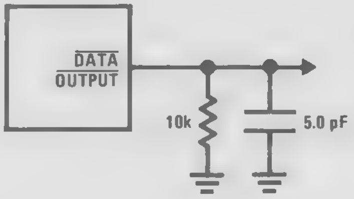
$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

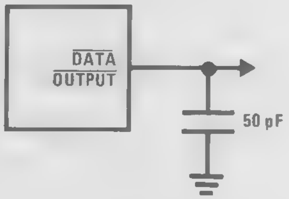
t_{0H}



t_{1H}

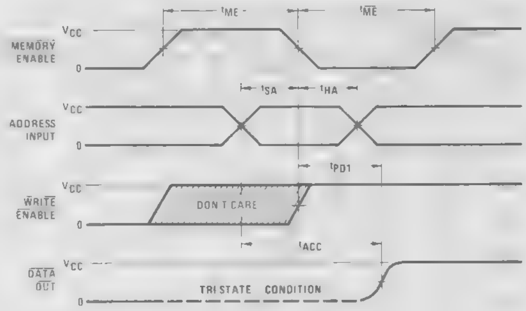


All Other AC Tests

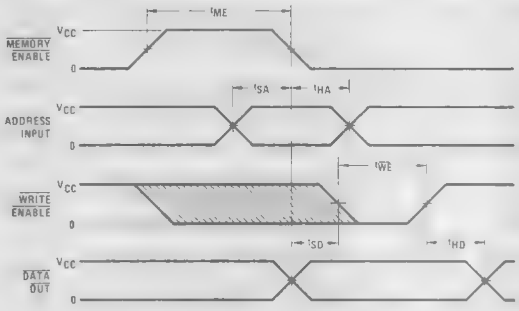


Switching Time Waveforms

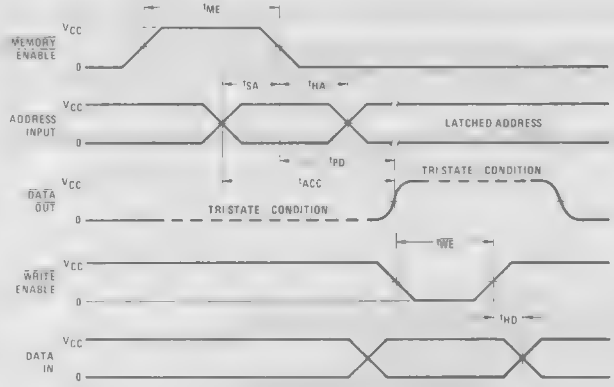
Read Cycle (Note 1)



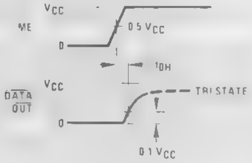
Write Cycle (Note 1)



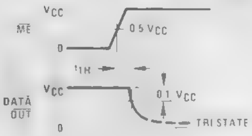
Read-Modify-Write Cycle (Note 1)



t_{0H}



t_{1H}



Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

ADVANCE INFORMATION

NMC27C16 16,384-Bit (2048 × 8) UV Erasable CMOS PROM

Max Access/Current	NMC27C16-1	NMC27C16-2	NMC27C16
Access (TAVQV-ns)	350	390	450
Active Current (ICC-mA/MHz)	25	25	25
Standby Current (ICC-μA)	100	100	100

General Description

The NMC27C168 is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

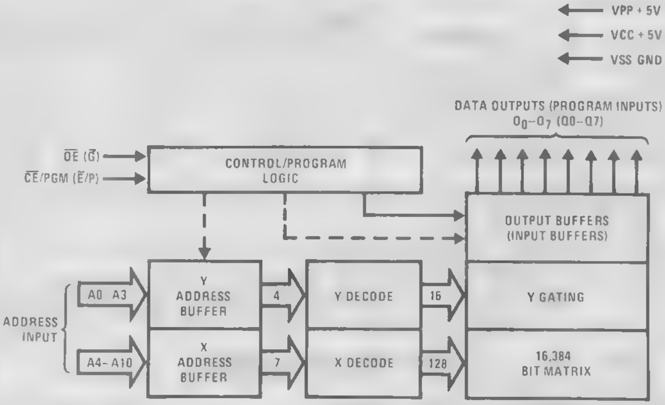
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, CMOS silicon gate technology.

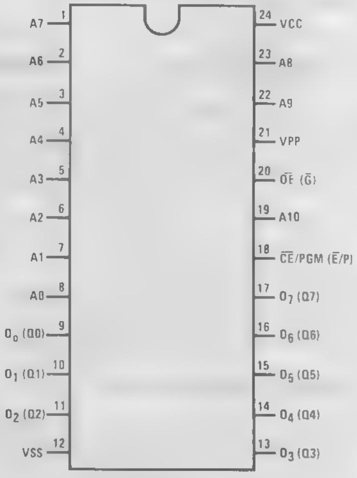
Features

- 2048 × 8 organization
- Low power during programming
- Access time down to 350 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output
- CMOS power consumption

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Pin Connection During Read or Program

Mode	Pin Name/Number				
	$\overline{\text{CE}}$/PGM ($\overline{\text{E}}$/P) 18	$\overline{\text{OE}}$ ($\overline{\text{G}}$) 20	VPP 21	VCC 24	Outputs 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0–A10	Address Inputs
O_0–O_7(Q0–Q7)	Data Outputs
$\overline{\text{CE}}$/PGM($\overline{\text{E}}$/P)	Chip Enable/Program
$\overline{\text{OE}}$(G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power 5V
VSS	Ground

* Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V
Input Voltages with Respect to VSS (except VPP) (Note 6)	6V to −0.3V
Output Voltages with Respect to VSS	VCC + 0.3V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC Operating Characteristics TA = 0°C to +70°C, VCC = 5V ±5%, VPP = VCC ± 0.6V (Note 3), VSS = 0V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Current	VIN = 5.25V or VIN = VIL			10	μA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = 5V			10	μA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC + 1	V
VOL1	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH1	Output High Voltage	IOH = −400 μA	2.4			V
VOL2	Output Low Voltage	IOL = 0 μA			GND + 0.01	V
VOH2	Output High Voltage	IOH = 0 μA	VCC − 0.1			V
IPP1	VPP Supply Current	VPP = 5.85V			10	μA
ICC1	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL (Note 5)			25	mA/MHz
ICC2	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL			100	μA

AC Characteristics (Note 2) TA = 0°C to +70°C, VCC = 5V ±5%, VPP = VCC ± 0.6V (Note 3), VSS = 0V, unless otherwise noted.

Symbol		Parameter	Conditions	NMC27C16		NMC27C16-1		NMC27C16-2		Units
Alternate	Standard			Min	Max	Min	Max	Min	Max	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		450		350		390	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL		450		350		390	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		120		120		120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		0		0		ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	0	100	0	100	ns

Capacitance (Note 4) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

AC Test Conditions

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times:	≤ 20 ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical conditions are for operation at: TA = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

Note 3: VPP may be connected to VCC except during program. The ±0.6V tolerance allows a circuit to switch VPP between the read voltage and the program voltage.

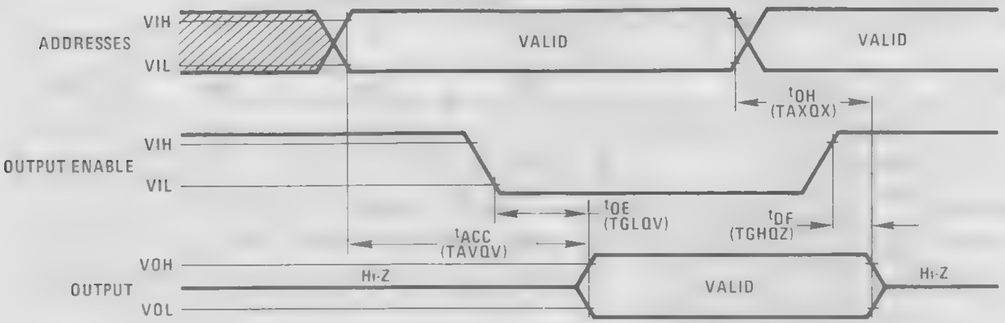
Note 4: Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.

Note 5: ICC increases for input voltage V_I: (VCC − 0.3V) > V_I > +0.3V unless in standby mode. During standby, all inputs except $\overline{CE}$ are disabled and draw no ICC for any V_I.

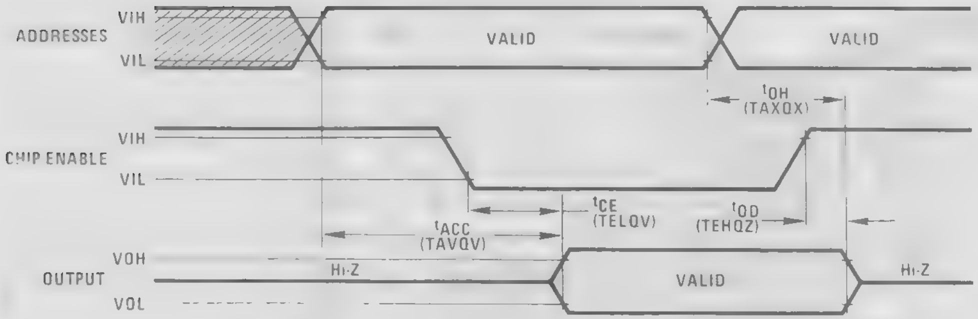
Note 6: The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V to −0.3V.

Switching Time Waveforms*

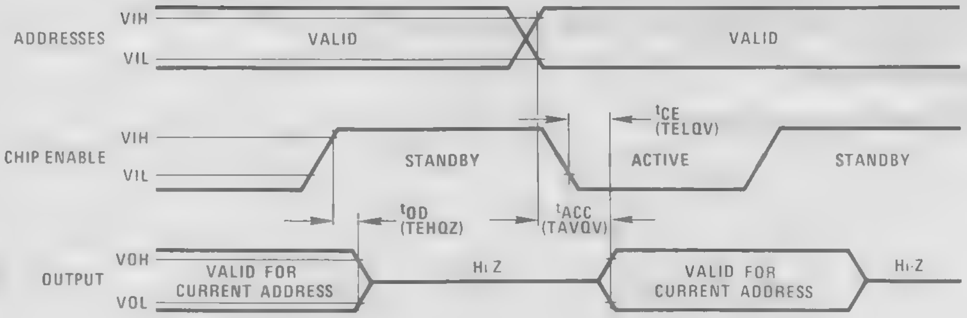
Read Cycle ($\overline{\text{CE}}$/PGM = VIL)



Read Cycle ($\overline{\text{OE}}$ = VIL)



Standby Power-Down Mode ($\overline{\text{OE}}$ = VIL)



* Symbols in parentheses are proposed industry standard.

PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions

(Notes 1 and 2) (TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

Symbol	Parameter	Min	Typ	Max	Units
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	– 0.1		0.8	V
VIH	Input High Level	2.0		VCC + 1	V
ICC	VCC Power Supply Current			100	μA
IPP1	VPP Supply Current (Note 4)			10	μA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions

(Notes 1, 2, and 6) (TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

Symbol		Parameter	Min	Typ	Max	Units
Alternate	Standard					
t_{AS}	TAVPH	Address Set-up Time	2			μs
t_{OS}	TGHPH	$\overline{OE}$ Set-up Time	2			μs
t_{DS}	TDVPH	Data Set-up Time	2			μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			μs
t_{DH}	TPLDX	Data Hold Time	2			μs
t_{DF}	TGHQZ	Output Disable to Output TRI-STATE Delay (Note 4)	0		100	ns
t_{OE}	TGLQV	Output Enable to Output Delay (Note 4)			120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to + 25V.

Note 3: 0.45V ≤ VIN ≤ 5.25V

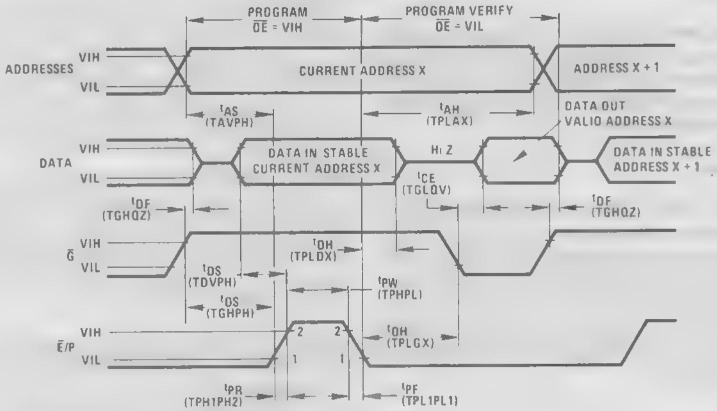
Note 4: $\overline{CE}$/PGM = VIL, VPP = VCC

Note 5: VPP = 26V

Note 6: Transition times ≤ 20 ns unless noted otherwise.

Timing Diagram*

Program Mode



Functional Description

DEVICE OPERATION

The NMC27C16 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The NMC27C16 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The NMC27C16 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more NMC27C16s for memory expansion.

Standby Mode (Power Down)

The NMC27C16 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 0.4% (500 μW max) of the normal operating power. VCC must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The NMC27C16 is shipped from National completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

Program Mode

The NMC27C16 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

> With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. NMC27C16s may be programmed in parallel with the same data in this mode.

TABLE I. OPERATING MODES (VCC = 5V)

Mode	Pin Name/Number		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ (G) 20	Outputs 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

Mode	Pin Name/Number			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ (G) 20	VPP 21	Outputs Q 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

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* Symbols in parentheses are proposed industry standard.

Functional Description (Continued)

Program Verify Mode

The programming of the NMC27C16 may be verified either 1 word at a time during the programming (as shown in the Timing Diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case.

Program Inhibit Mode

The program inhibit mode allows programming several NMC27C16s simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the NMC27C16 may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The NMC27C16 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the NMC27C16 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm^2 power rating is used. The NMC27C16 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

NMC6504 4096-Bit (4096 × 1) Static RAM

General Description

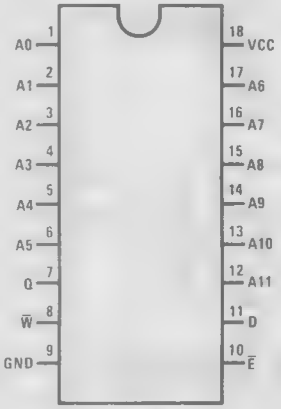
The NMC6504 is a static CMOS random access read/write memory organized as 4096 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible to the TTL environment. Synchronous operation is provided by on-chip address, data, and write latches. The ENABLE input serves as the device strobe controlling the latching functions. The TRI-STATE® output, in conjunction with the ENABLE input, allows easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging
- Output data latches
- Input data latches
- Select latch for microprocessor interface

Connection Diagram

Dual-In-Line Package

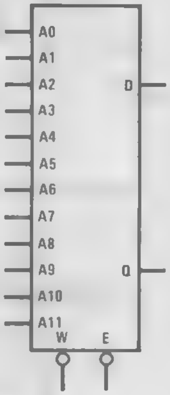


TOP VIEW

Order Number NMC6504J-2, NMC6504J-9 or NMC6504J-5
See NS Package J18A

Order Number NMC6504N-5
See NS Package N18A

Logic Symbol



Pin Names

A0–A11	Address Inputs
Ē	Chip Enable
W̄	Write Enable
D	Data Input
Q	Data Output

Functional Description

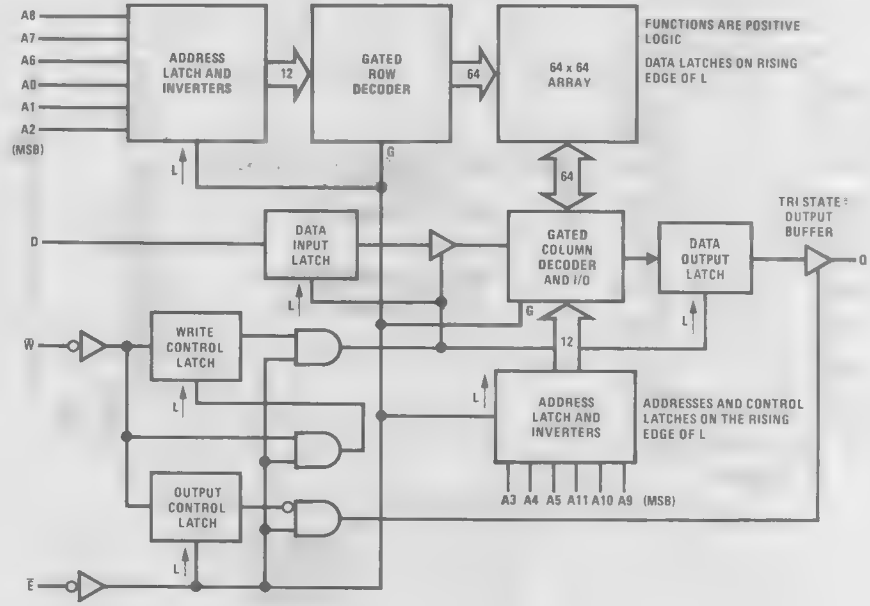
An NMC6504 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input which latches the address information into the on-chip registers. On-chip latches allow selection of a read, early write, or read-modify-write cycle as a function of the ENABLE and WRITE ($\overline{W}$) input levels and timing. Data output is enabled by the falling edge of the ENABLE input and disabled by the rising edge except when performing an early write cycle. The input and output data latches are transparent except during the write pulse (not the WRITE input).

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

An early write cycle is performed by preceding the ENABLE with the HIGH to LOW transition of the WRITE input. The WRITE input level is latched, and set-up and hold times must be met. The data output is not enabled during an early write cycle. The input data set-up and hold times are referenced to the leading edge of the write pulse, which is initiated by the falling edge of the ENABLE input and terminated by the rising edge of the ENABLE.

A read-modify-write cycle is performed as a read cycle, for the enable access time, followed by the write pulse which is initiated by the falling edge of the WRITE input and terminated by the rising edge of either the ENABLE or WRITE input, whichever occurs first. The input data set-up and hold times are referenced to the falling edge of the WRITE input. Data is latched when the WRITE input goes LOW, allowing the modified data to be written into the memory while continuing to read the original data.

Block Diagram


A8
A7
A6
A0
A1
A2
(MSB)
ADDRESS LATCH AND INVERTERS
12
GATED ROW DECODER
64
64 x 64 ARRAY
FUNCTIONS ARE POSITIVE LOGIC
DATA LATCHES ON RISING EDGE OF L
L
G
64
D
DATA INPUT LATCH
GATED COLUMN DECODER AND I/O
DATA OUTPUT LATCH
TRI STATE OUTPUT BUFFER
Q
L
G
L
W̄
WRITE CONTROL LATCH
12
L
L
ADDRESS LATCH AND INVERTERS
ADDRESSES AND CONTROL LATCHES ON THE RISING EDGE OF L
A3 A4 A5 A11 A10 A9 (MSB)
OUTPUT CONTROL LATCH
L
Ē

Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6504-9	4.5V	5.5V
NMC6504-2	4.5V	5.5V
NMC6504-5	4.75V	5.25V
Temperature		
NMC6504-9	−40°C	85°C
NMC6504-2	−55°C	125°C
NMC6504-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6504-9, NMC6504-2		NMC6504-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			50		500	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		10		10	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		25		500	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC −2.0	VCC +0.3	VCC −2	VCC +0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VOL	Output Low Voltage	IOL = 2.0 mA		0.4		0.45	V
VOH	Output High Voltage	IOH = −1.0 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		8		8	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

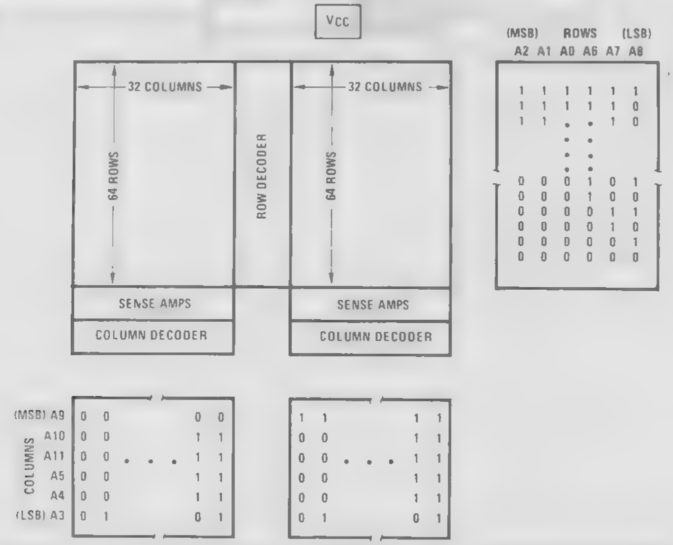
AC Test Conditions

Input Rise and Fall Times: ≤20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

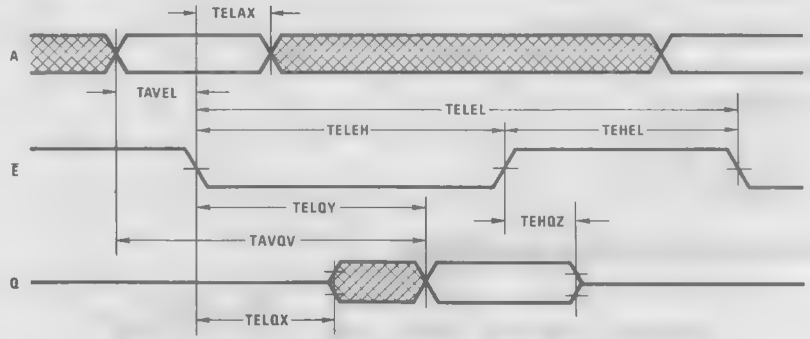
NMC6504 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TELEH	Enable (Ē) Minimum Low Time	300		350		ns
TELEL	Read or Write Cycle Time	420		500		ns
TEHEL	Enable (Ē) Minimum High Time	120		150		ns
TELQX	Output Enable from Enable (Ē)		100		100	ns
TEHQZ	Output Disable from Enable (Ē)		100		100	ns

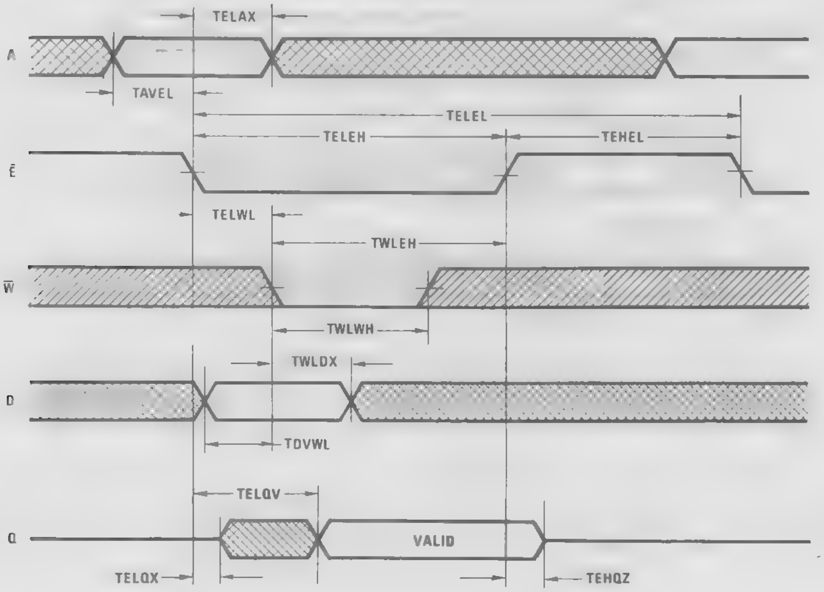
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	80		100		ns
TELEL	Read or Write Cycle Time	420		500		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	300		350		ns
TDVWL	Data Set-up Time	0		30		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	120		150		ns
TWLDX	Data Hold Time	80		100		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	80		100		ns
TELWL	Early Write Output Hi-Z Time	0		0		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	200		250		ns
TELQX	Output Enable from $\overline{E}$		100		100	ns
TELQV	Enable Access Time		300		350	ns
TEHQZ	Output Disable from $\overline{E}$		100		100	ns

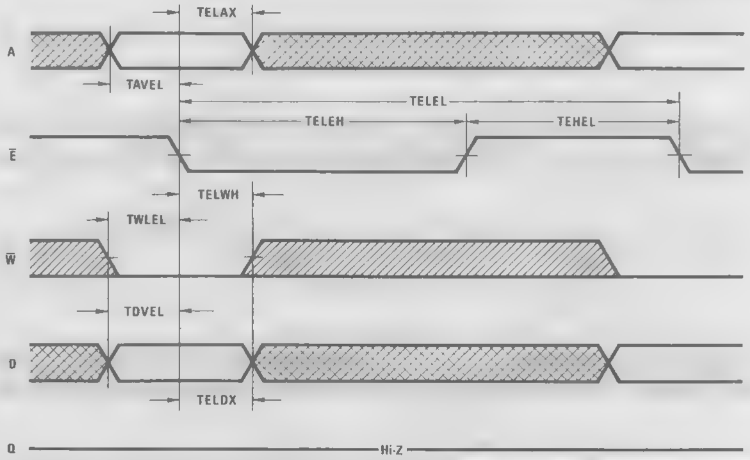
Write Cycle Waveforms



Early Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	80		100		ns
TDVEL	Early Write Data Set-up Time	0		30		ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	300		350		ns
TWLEL	Early Write Set-up Time	0		0		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TELDX	Early Write Data Hold Time	80		100		ns
TELEL	Read or Write Cycle Time	420		500		ns

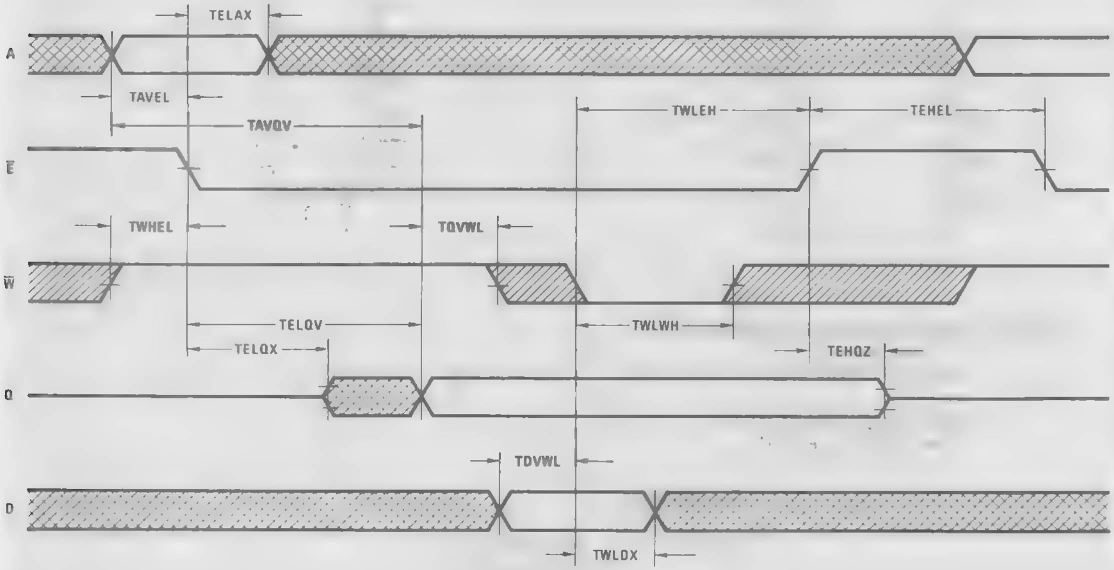
Early Write Cycle Waveforms



Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	120		150		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	200		250		ns
TQVWL	Data Valid to Write Time	0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	80		100		ns
TWLDX	Data Hold Time	80		100		ns
TELQX	Output Enable from Enable ($\overline{E}$)		100		100	ns
TEHQZ	Output Disable from Enable ($\overline{E}$)		100		100	ns
TDVWL	Data Set-up Time	0		30		ns

Read-Modify-Write Cycle Waveforms



National Semiconductor

NMC6508 1024-Bit (1024 × 1) Static RAM

General Description

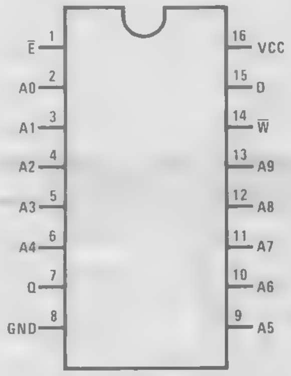
The NMC6508 is a static CMOS random access read/write memory organized as 1024 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible to the TTL environment. Synchronous operation is provided by the on-chip latches for the address inputs. The NMC6508 may be used in common I/O applications by externally connecting the data input and output terminals. The TRI-STATE® output, in conjunction with the ENABLE input, allows for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 16 pin — high density packaging
- Output data latches

Connection Diagram

Dual-In-Line Package

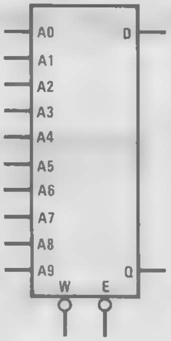


TOP VIEW

Order Number NMC6508J-2, NMC6508J-9 or NMC6508J-5
See NS Package J18A

Order Number NMC6508N-5
See NS Package N18A

Logic Symbol



Pin Names

A0–A9	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

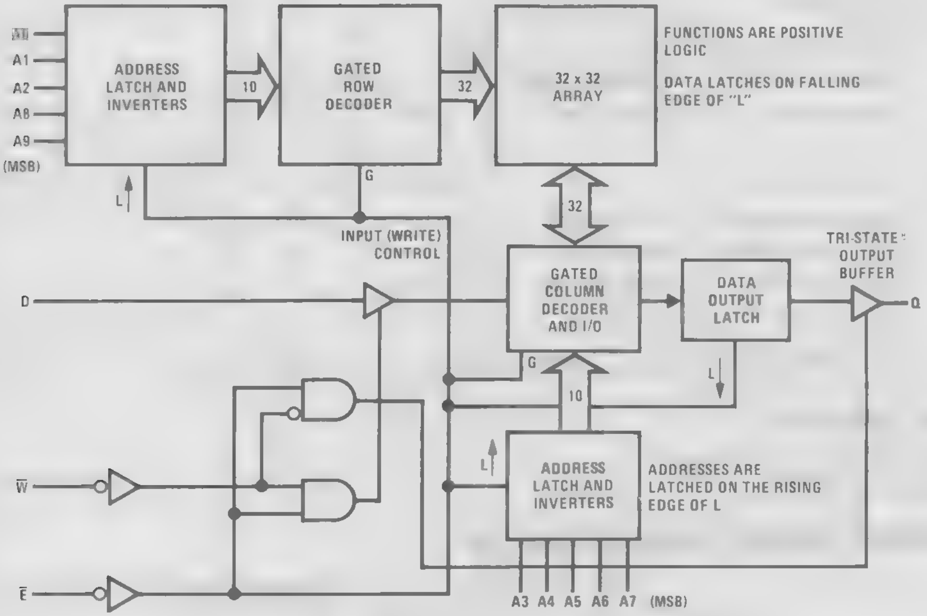
Functional Description

An NMC6508 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the address information into the on-chip registers. The output buffer is enabled when the WRITE ($\overline{W}$) input is HIGH and the ENABLE input is LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next memory cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse is created by the coincident LOW of the ENABLE and WRITE inputs. The data set-up and hold times are referenced to the rising edge of either the ENABLE or WRITE input, whichever occurs first.

Block Diagram



A0
A1
A2
A8
A9
(MSB)
ADDRESS LATCH AND INVERTERS
10
GATED ROW DECODER
32
32 x 32 ARRAY
FUNCTIONS ARE POSITIVE LOGIC
DATA LATCHES ON FALLING EDGE OF "L"
L
G
32
INPUT (WRITE) CONTROL
TRI-STATE® OUTPUT BUFFER
D
GATED COLUMN DECODER AND I/O
DATA OUTPUT LATCH
Q
G
10
L
L
ADDRESS LATCH AND INVERTERS
ADDRESSES ARE LATCHED ON THE RISING EDGE OF L
W̄
Ē
A3 A4 A5 A6 A7 (MSB)

Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6508B-9	4.5V	5.5V
NMC6508B-2	4.5V	5.5V
NMC6508-9	4.5V	5.5V
NMC6508-2	4.5V	5.5V
NMC6508-5	4.75V	5.25V
Temperature		
NMC6508B-9	−40°C	85°C
NMC6508B-2	−55°C	125°C
NMC6508-9	−40°C	85°C
NMC6508-2	−55°C	125°C
NMC6508-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6508B-9, NMC6508B-2 NMC6508-9, NMC6508-2		NMC6508-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

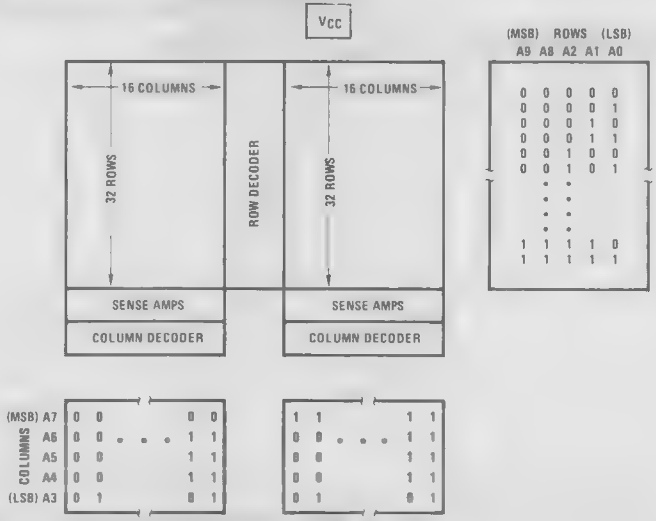
AC Test Conditions

Input Rise and Fall Times: ≤20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

NMC6508 Bit Map and Address Decoding



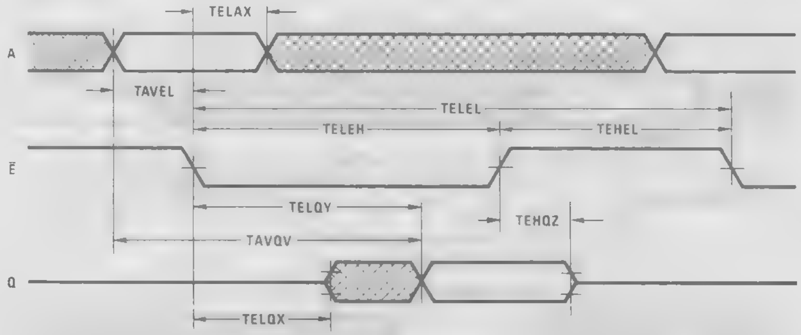
A9 A8 A2 A1 A0
0 0 0 0 0
0 0 0 0 1
0 0 0 1 0
0 0 0 1 1
0 0 1 0 0
0 0 1 0 1
• •
• •
• •
1 1 1 1 0
1 1 1 1 1

(MSB) A7: 0 0 … 0 0 | 1 1 … 1 1
A6: 0 0 … 1 1 | 0 0 … 1 1
A5: 0 0 … 1 1 | 0 0 … 1 1
A4: 0 0 … 1 1 | 0 0 … 1 1
(LSB) A3: 0 1 … 0 1 | 0 1 … 0 1

Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TELEH	Enable (Ē) Minimum Low Time	180		250		300		ns
TELQX	Output Enable from Enable (Ē)		120		160		200	ns
TEHQZ	Output Disable from Enable (Ē)		120		160		200	ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	280		350		450		ns

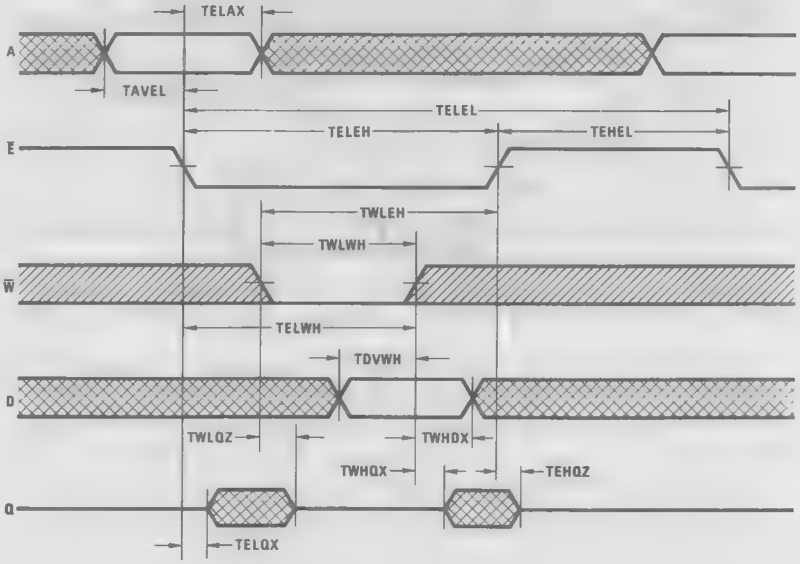
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TDVWH	Data Set-up Time	80		110		130		ns
TELWH	Write Pulse Width (Ē and W̄ Low)	100		130		160		ns
TWLWH	Write Pulse Width (W̄ Low)	100		130		160		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TWHDM	Data Hold Time	0		0		0		ns
TWLEH	Write Pulse Width (Ē and W̄ Low)	100		130		160		ns
TELEH	Enable (Ē) Minimum Low Time	180		250		300		ns
TELQX	Output Enable from Ē		120		160		200	ns
TWLQZ	Output Disable from W̄		120		160		200	ns
TWHQX	Output Enable from W̄		120		160		200	ns
TEHQZ	Output Disable from Ē		120		160		200	ns

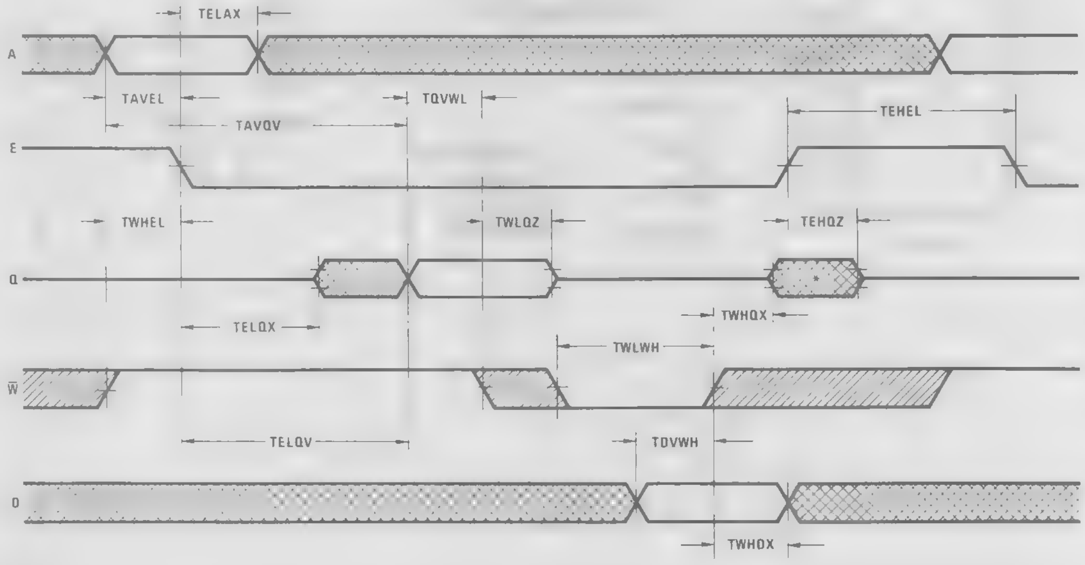
Write Cycle Waveforms



Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWHDM	Data Hold Time	0		0		0		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELQX	Output Enable from Enable ($\overline{E}$)		120		160		200	ns
TEHQZ	Output Disable from Enable ($\overline{E}$)		120		160		200	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		120		160		200	ns
TDVWH	Data Set-up Time	80		110		130		ns
TWHQX	Output Enable from Write ($\overline{W}$)		120		160		200	ns

Read-Modify-Write Cycle Waveforms



* Output enable can be avoided by preceding the rising edge of $\overline{W}$ with the rising edge of $\overline{E}$ by time: TEHQZ

National Semiconductor

PRELIMINARY

NMC6514 4096-Bit (1024 × 4) Static RAM

General Description

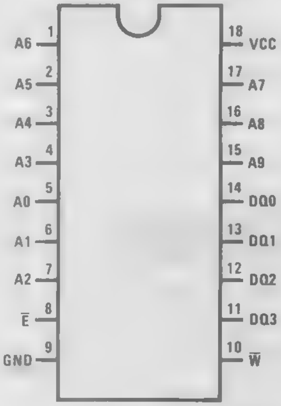
The NMC6514 is a static CMOS random access read/write memory organized as 1024 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by on-chip address latches. The ENABLE input serves as the device strobe controlling the address latching function. The data I/O terminals, when not output data enabled, represent a high impedance for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging

Connection Diagram

Dual-In-Line Package



TOP VIEW

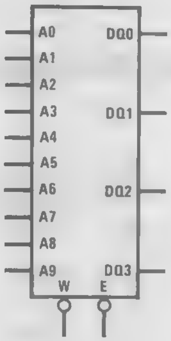
Order Number NMC6514J-2, NMC6514J-9
or NMC6514J-5
See NS Package J18A

Order Number NMC6514N-5
See NS Package N18A

Pin Names

A0–A9	Address Inputs
Ē	Chip Enable
W̄	Write Enable
DQ0–DQ3	Data In/Out

Logic Symbol



Functional Description

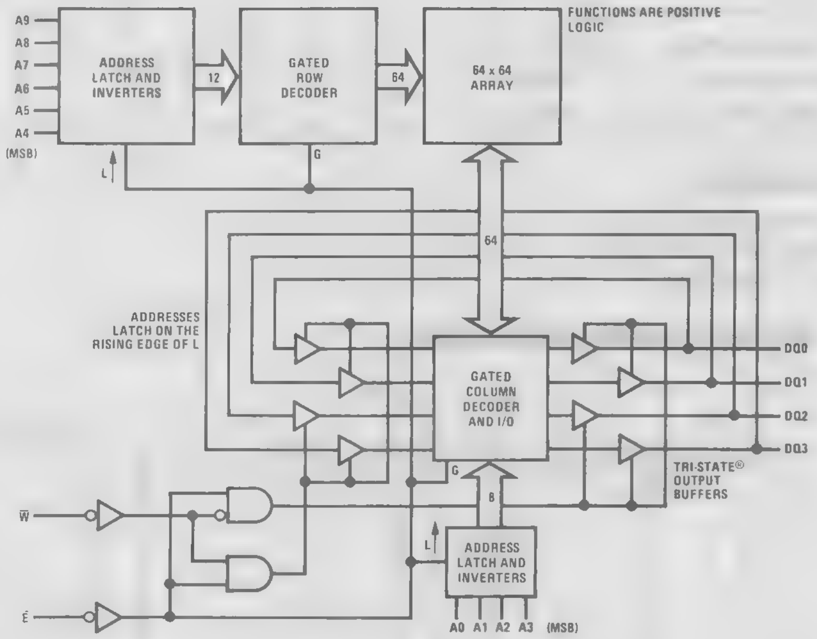
An NMC6514 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the address information into the on-chip registers. Read, write, the read-modify-write cycles are selected as a function of the ENABLE and WRITE ($\overline{W}$) input levels and timing. Data output is enabled by the falling edge of the ENABLE input and disabled by the rising edge when the WRITE input is HIGH. The output is disabled when writing.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

When performing a write cycle a minimum ENABLE LOW time is required to enter the new data. The write pulse is created by the coincident LOW of the ENABLE and WRITE inputs. The data set-up and hold time are referenced to the rising edge of either the ENABLE or WRITE inputs whichever occurs first.

A read-modify-write cycle is performed as a read cycle, for the enable access time, followed by the write pulse caused by the LOW time of the WRITE input. The output data is disabled by the falling edge of the WRITE input, and input data, meeting the set-up and hold requirements must be provided.

Block Diagram


A9
A8
A7
A6
A5
A4
(MSB)
ADDRESS LATCH AND INVERTERS
12
GATED ROW DECODER
64
64 x 64 ARRAY
FUNCTIONS ARE POSITIVE LOGIC
L
G
64
ADDRESSES LATCH ON THE RISING EDGE OF L
GATED COLUMN DECODER AND I/O
DQ0
DQ1
DQ2
DQ3
TRI-STATE® OUTPUT BUFFERS
G
8
W̄
L
ADDRESS LATCH AND INVERTERS
Ē
A0 A1 A2 A3 (MSB)

Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6514-9	4.5V	5.5V
NMC6514-2	4.5V	5.5V
NMC6514-5	4.75V	5.25V
Temperature		
NMC6514-9	−40°C	85°C
NMC6514-2	−55°C	125°C
NMC6514-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6514-9, NMC6514-2		NMC6514-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			50		500	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		10		10	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		25		500	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VOL	Output Low Voltage	IOL = 2.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −1.0 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		8		8	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

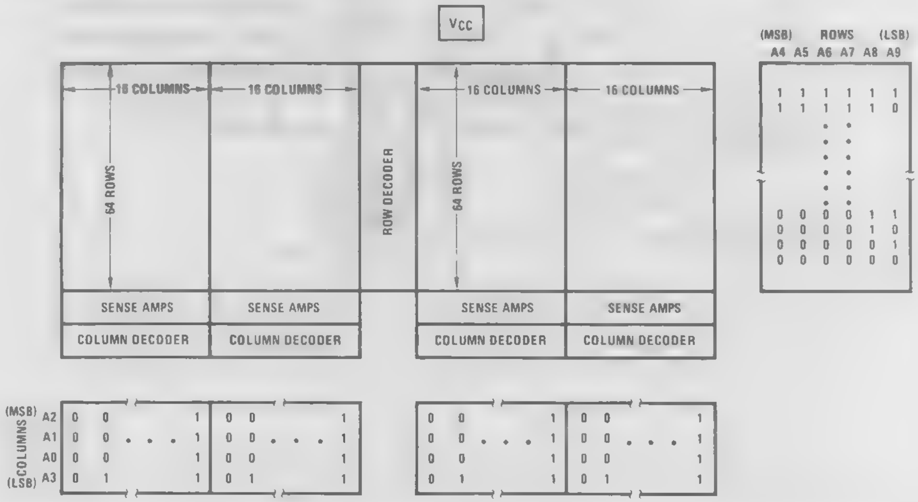
AC Test Conditions

Input Rise and Fall Times: ≤20 ns

All Timing Reference Levels: 1/2 VCC

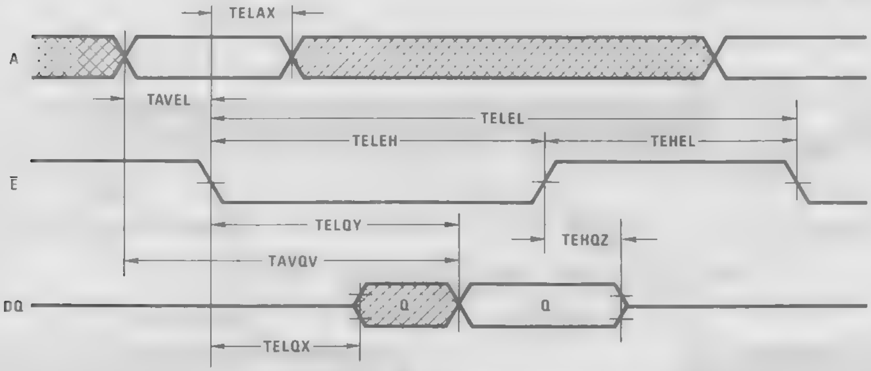
Output Load: 1 TTL Load, 50 pF

NMC6514 Bit Map and Address Decoding



		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TELEH	Enable (Ē) Minimum Low Time	300		350		ns
TEHEL	Enable (Ē) Minimum High Time	120		150		ns
TELQX	Output Enable from Enable (Ē)		100		100	ns
TEHQZ	Output Disable from (Ē)		100		100	ns
TELEL	Read or Write Cycle Time	420		500		ns

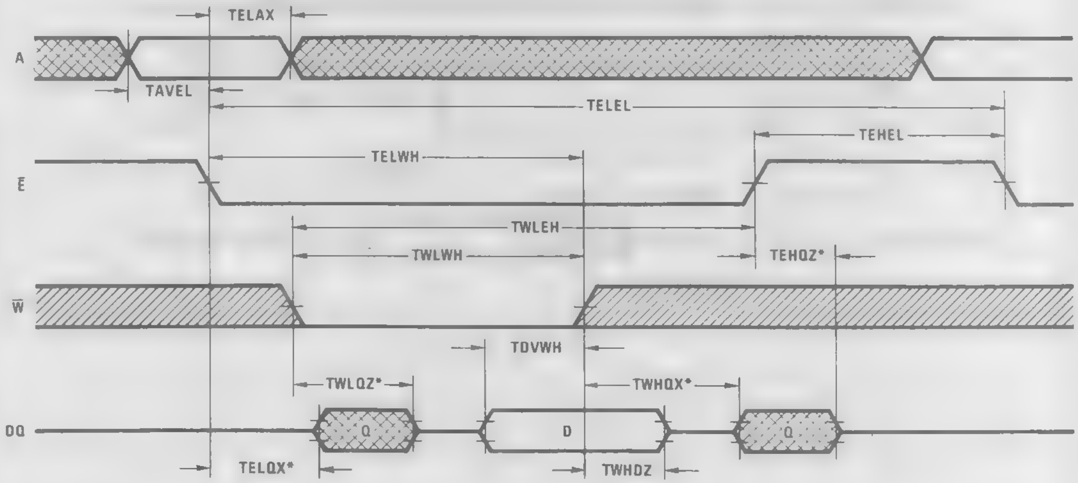
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TWLEH	Write Pulse Width (Ē and W̅ Low)	300		350		ns
TEHEL	Enable (Ē) Minimum High Time	120		150		ns
TWLWH	Write Pulse Width (W̅ Low)	300		350		ns
TELEL	Read or Write Cycle Time	420		500		ns
TWHQX	Output Enable from Write (W̅)		100		100	ns
TELQX	Output Enable from Enable (Ē)		100		100	ns
TEHQZ	Output Disable from Enable (Ē)		100		100	ns
TWLQZ	Output Disable from Write (W̅)		100		100	ns
TDVWH	Data Set-up Time	200		250		ns
TWHDZ	Data Hold Time	0		0		ns
TELWH	Write Pulse Width (Ē and W̅ Low)	300		350		ns

Write Cycle Waveforms

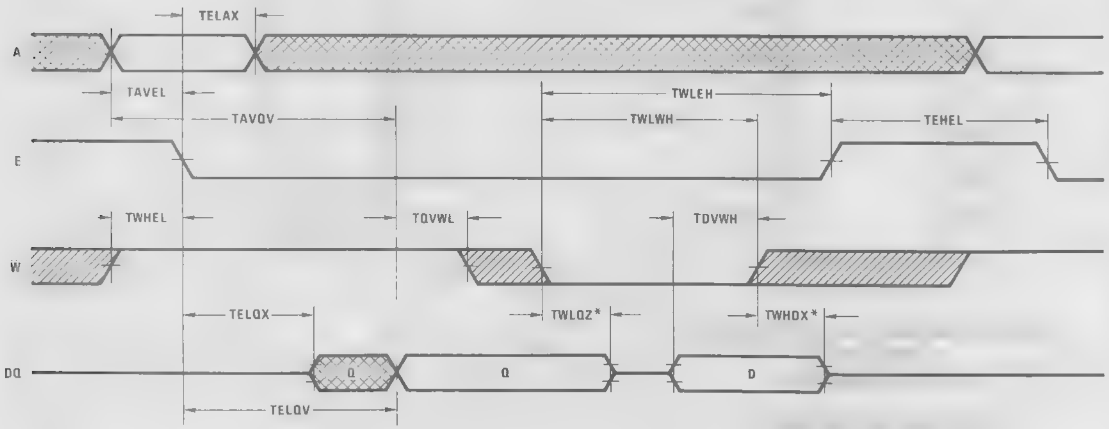


* Avoid bus contention

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TWLQZ	Output Disable from Write (W̄)		100		100	ns
TDVWH	Data Set-up Time	200		250		ns
TWHDX	Data Hold Time	0		0		ns
TWLEH	Write Pulse Width (W̄ and Ē Low)	300		350		ns
TQVWL	Data Valid to Write Time	0		0		ns
TWLWH	Write Pulse Width (W̄ Low)	300		350		ns
TELQX	Output Enable from Enable (Ē)		100		100	ns
TEHEL	Enable (Ē) Minimum High Time	120		150		ns
TWHEL	W̄ Read Mode Set-up Time	0		0		ns

Read-Modify-Write Cycle Waveforms



* Avoid bus contention

National Semiconductor

NMC6518 1024-Bit (1024 × 1) Static RAM

General Description

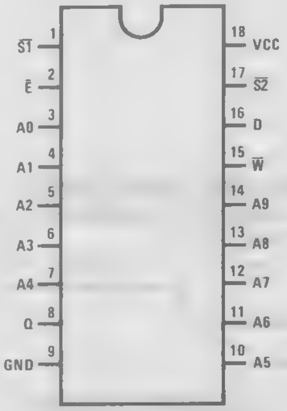
The NMC6518 is a static CMOS random access read/write memory organized as 1024 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by the on-chip latches for the address inputs and data output. The ENABLE input serves as the device strobe controlling the latching functions. The TRI-STATE® output, in conjunction with the ENABLE input, allow easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 18 pin — high density packaging
- Output data latches

Connection Diagram

Dual-In-Line Package

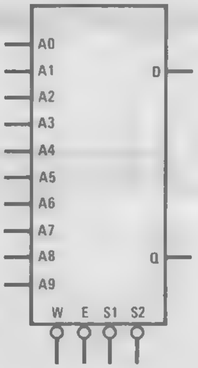


TOP VIEW

Order Number NMC6518J-2, NMC6518J-9
or NMC6518J-5
See NS Package J16A

Order Number NMC6518N-5
See NS Package N16A

Logic Symbol



Pin Names

A0–A9	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
$\overline{S1}$, $\overline{S2}$	Chip Selects

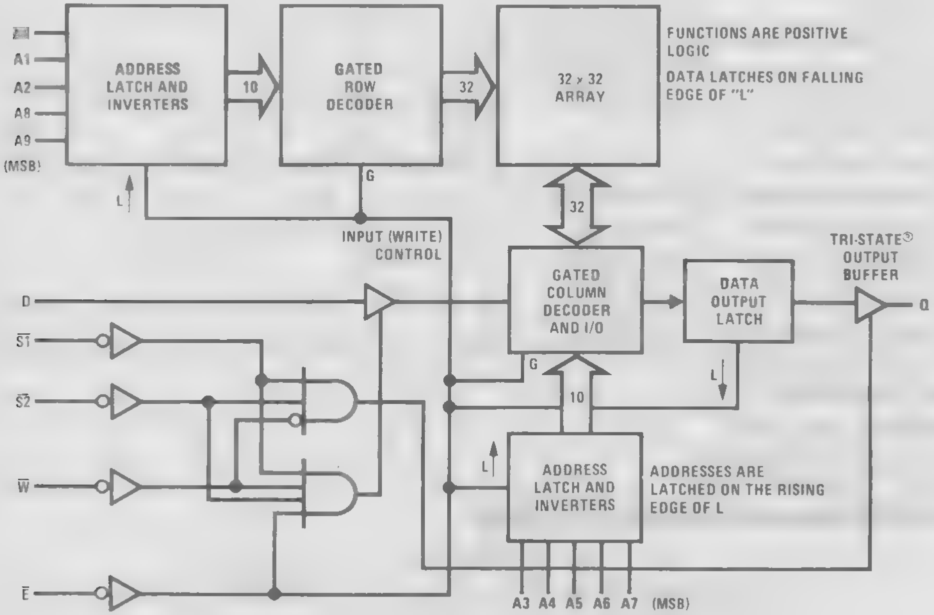
Functional Description

An NMC6518 memory cycle is initiated by the falling edge of the ENABLE input, which latches the address information into the on-chip registers. Data output is enabled when the WRITE ($\overline{W}$) input is high and the ENABLE, SELECT 1 ($\overline{S1}$) and SELECT 2 ($\overline{S2}$) inputs are LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum ENABLE LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse is created by the coincident LOW of the WRITE, ENABLE and both SELECT inputs. The input data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, SELECT 1 or SELECT 2 inputs, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6518B-9	4.5V	5.5V
NMC6518B-2	4.5V	5.5V
NMC6518-9	4.5V	5.5V
NMC6518-2	4.5V	5.5V
NMC6518-5	4.75V	5.25V
Temperature		
NMC6518B-9	−40°C	85°C
NMC6518B-2	−55°C	125°C
NMC6518-9	−40°C	85°C
NMC6518-2	−55°C	125°C
NMC6518-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6518B-9, NMC6518B-2 NMC6518-9, NMC6518-2		NMC6518-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

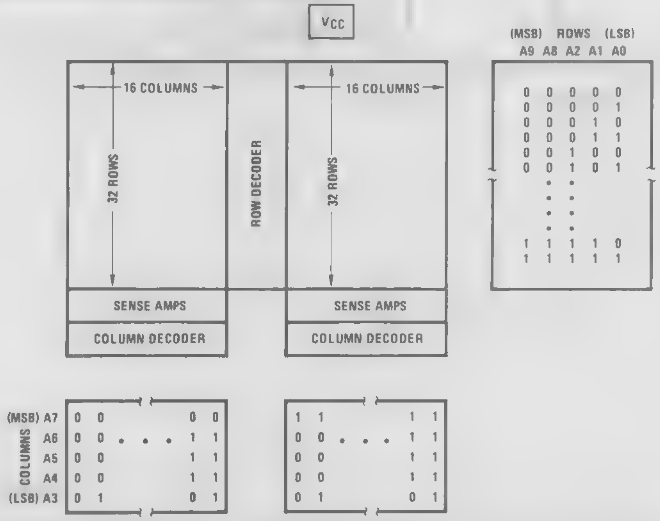
AC Test Conditions

Input Rise and Fall Times: ≤20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

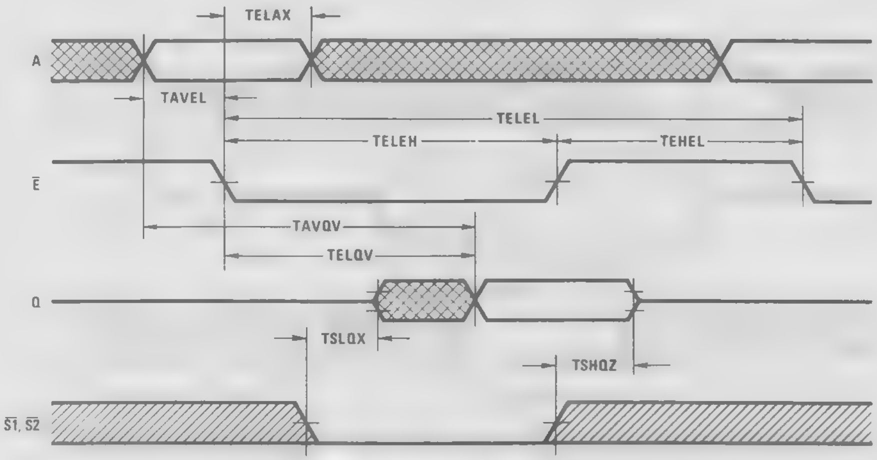
NMC6518 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TELEH	Enable (Ē) Minimum Low Time	180		250		300		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TSHQX	Chip Select Output Disable Time		120		160		200	ns
TSLQX	Chip Select Output Enable Time		120		160		200	ns

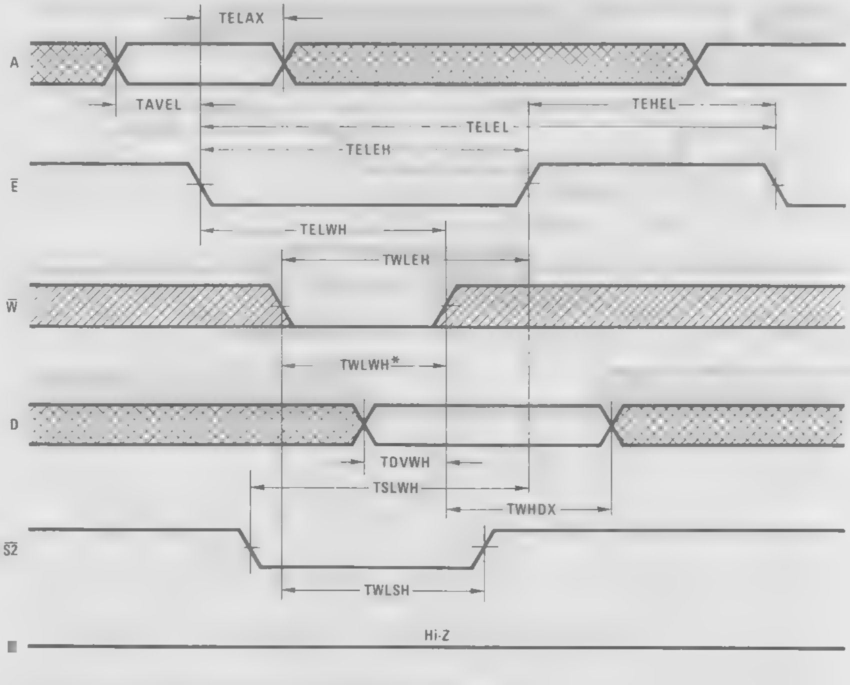
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TWLSH	Chip Select Write Pulse Set-up Time	100		130		160		ns
TWLEH	Chip Enable Write Pulse Set-up Time	100		130		160		ns
TSLWH	Chip Select Write Pulse Hold Time	100		130		160		ns
TWHDX	Data Hold Time	0		0		0		ns
TDVWH	Data Set-up Time	80		110		130		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	180		250		300		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns

Write Cycle Waveforms

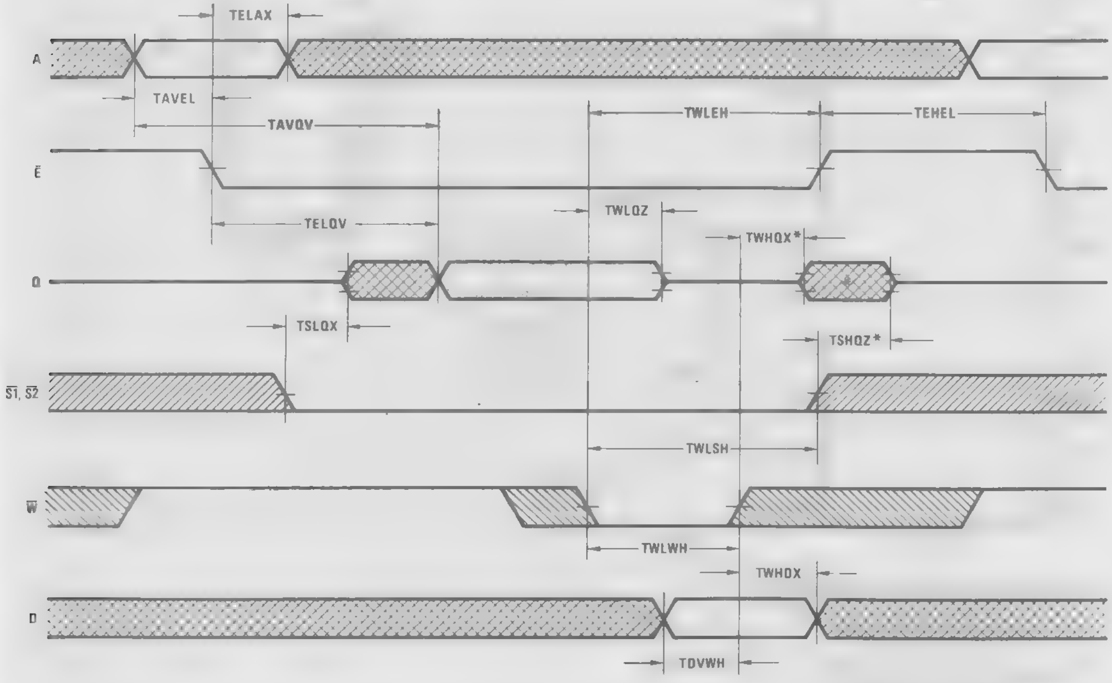


* TWLWH, the write pulse, is coincidence low of $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TSHQX	Chip Select Output Disable Time		120		160		200	ns
TWLWH	Write Pulse Width (W̄ Low)	100		130		160		ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TWLSH	Chip Select Write Pulse Set-up Time	100		130		160		ns
TWLEH	Chip Enable Write Pulse Set-up Time	100		130		160		ns
TSLQX	Chip Select Output Enable Time		120		160		200	ns
TWHDX	Data Hold Time	0		0		0		ns
TDVWH	Data Set-up Time	80		110		130		ns
TWHQX	Output Enable from Write (W̄)		120		160		200	ns
TWLQZ	Output Disable from Write (W̄)		120		160		200	ns

Read-Modify-Write Cycle Waveforms



* Precede W̄ rising edge with Ē rising edge to avoid unwanted output enabling

National Semiconductor

NMC6551 1024-Bit (256 × 4) Static RAM

General Description

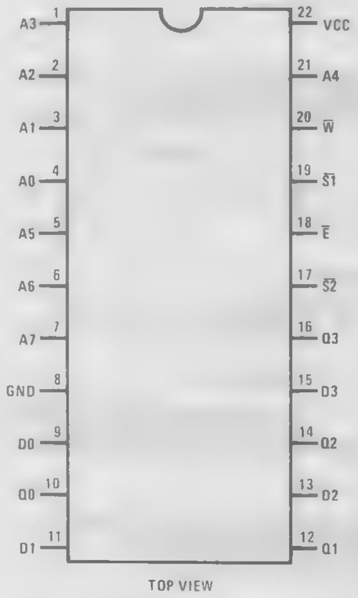
The NMC6551 is a static CMOS random access read/write memory organized as 256 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by on-chip address input and data output latches. The ENABLE input serves as the device strobe controlling the latching functions. The I/O terminals when not data output enabled, represent high impedance ports for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 22 pin — high density packaging
- Output data latches
- Select latch for microprocessor interface

Connection Diagram

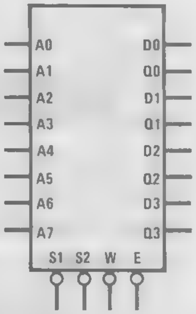
Dual-In-Line Package



Order Number NMC6551J-2, NMC6551J-9 or NMC6551J-5
See NS Package J22A

Order Number NMC6551N-5
See NS Package N22A

Logic Symbol



Pin Names

A0–A7	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
$\overline{S1}$, $\overline{S2}$	Chip Selects

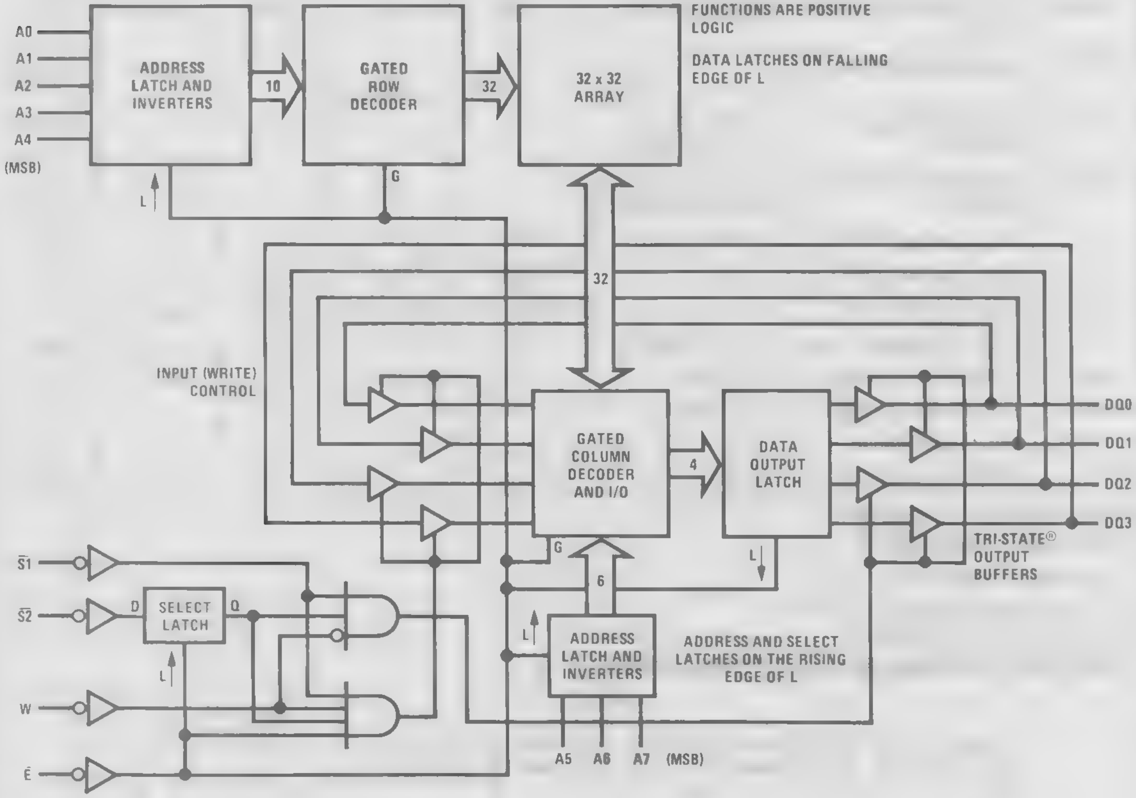
Functional Description

An NMC6551 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the ADDRESS and SELECT 2 ($\overline{S2}$) information into the on-chip registers. Set-up and hold times must be met. Data output is enabled when the WRITE ($\overline{W}$) input is HIGH and the ENABLE and SELECT 1 inputs are LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the outputs. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next memory cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse timing is created by the coincident LOW of the WRITE, ENABLE and SELECT 1 inputs. The data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, or SELECT 1 input, whichever occurs first.

Block Diagram


A0
A1
A2
A3
A4
(MSB)
ADDRESS LATCH AND INVERTERS
10
GATED ROW DECODER
32
32 x 32 ARRAY
FUNCTIONS ARE POSITIVE LOGIC
DATA LATCHES ON FALLING EDGE OF L
L
G
32
INPUT (WRITE) CONTROL
GATED COLUMN DECODER AND I/O
4
DATA OUTPUT LATCH
DQ0
DQ1
DQ2
DQ3
TRI-STATE® OUTPUT BUFFERS
S̄1
S̄2
D
SELECT LATCH
Q
L
W
Ē
G
6
L
L
ADDRESS LATCH AND INVERTERS
ADDRESS AND SELECT LATCHES ON THE RISING EDGE OF L
A5
A6
A7
(MSB)

Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6551B-9	4.5V	5.5V
NMC6551B-2	4.5V	5.5V
NMC6551-9	4.5V	5.5V
NMC6551-2	4.5V	5.5V
NMC6551-5	4.75V	5.25V
Temperature		
NMC6551B-9	−40°C	85°C
NMC6551B-2	−55°C	125°C
NMC6551-9	−40°C	85°C
NMC6551-2	−55°C	125°C
NMC6551-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6551B-9, NMC6551B-2 NMC6551-9, NMC6551-2		NMC6551-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10 1(+25°C)		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

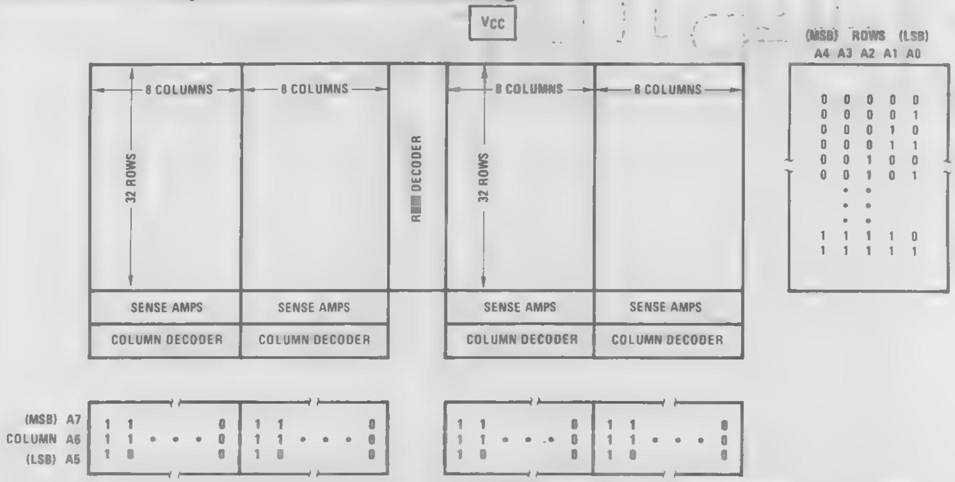
AC Test Conditions

Input Rise and Fall Times: ≤20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

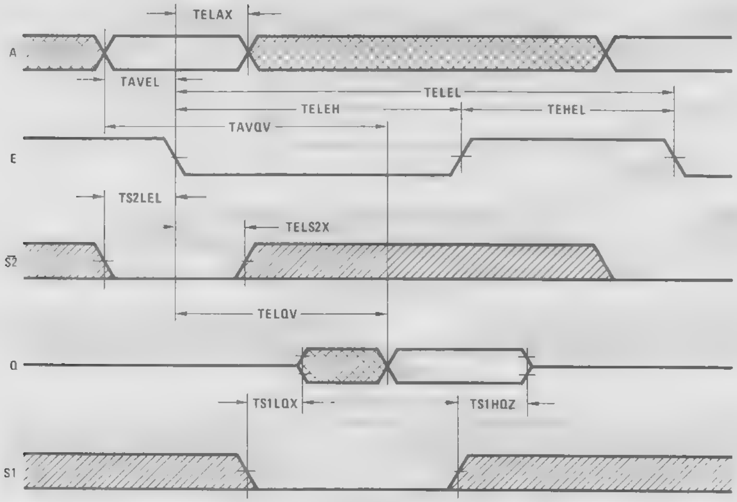
NMC6551 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6551B-9 NMC6551B-2		NMC6551-9 NMC6551-2		NMC6551-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TELEH	Enable (Ē) Minimum Low Time	220		300		350		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns

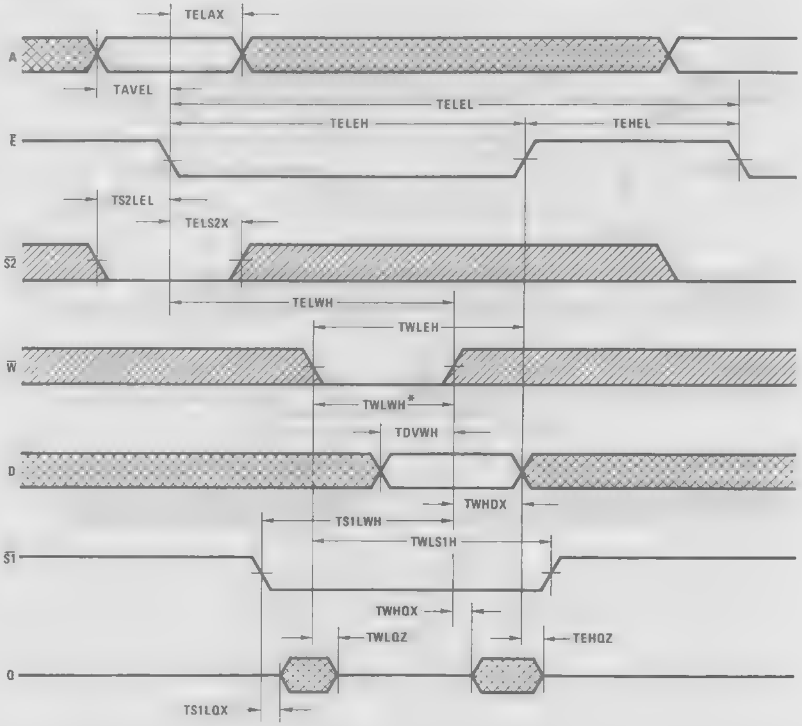
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6551B-9 NMC6551B-2		NMC6551-9 NMC6551-2		NMC6551-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	220		300		350		ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TDVWH	Data Set-up Time	100		150		170		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	120		180		210		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWLEH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	120		180		210		ns
TS1LWH	Chip Select 1 Write Pulse Hold Time	120		180		210		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LQX	Output Enable from $\overline{S1}$		130		150		180	ns
TWLQZ	Output Disable from $\overline{W}$		130		150		180	ns
TWHQX	Output Enable from $\overline{W}$		130		150		180	ns
TEHQZ	Output Disable from $\overline{E}$		130		150		180	ns

Write Cycle Waveforms

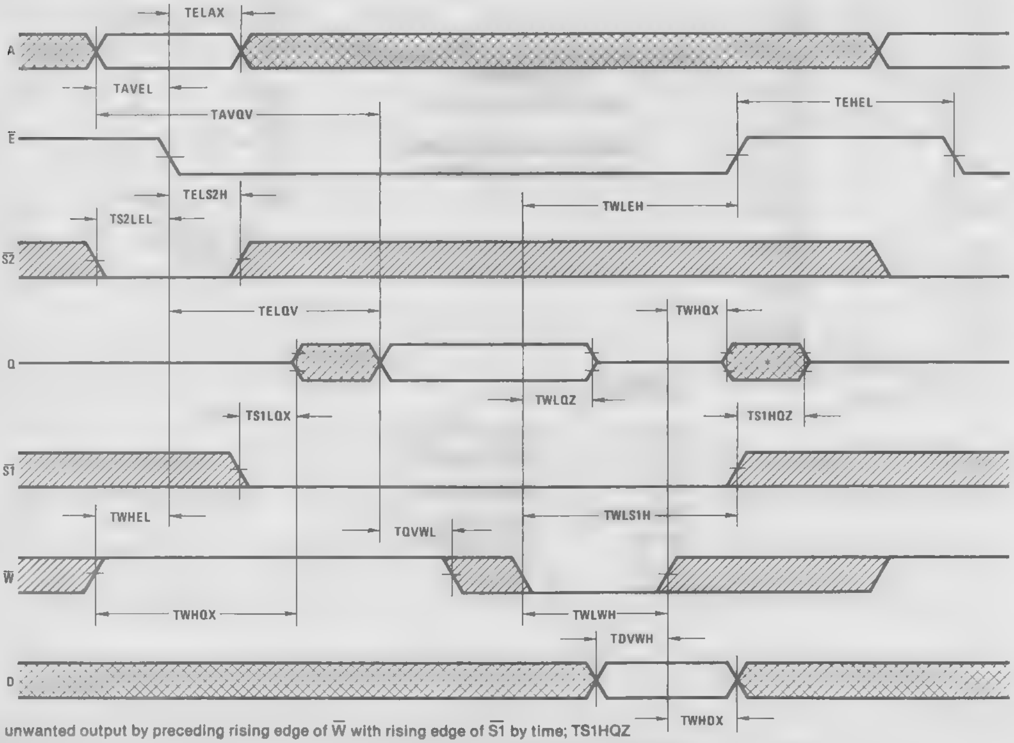


* TWLWH, the write pulse, is the coincidence low of $\overline{E}$, $\overline{W}$, and $\overline{S1}$ inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6551B-9 NMC6551B-2		NMC6551-9 NMC6551-2		NMC6551-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	120		180		210		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2H	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TWLQZ	Output Disable from Write ($\overline{W}$)		130		150		180	ns
TDVWH	Data Set-up Time	100		150		170		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		0		ns
TWHQX	Output Enable from Write ($\overline{W}$)		130		150		180	ns

Read-Modify-Write Cycle Waveforms



* Avoid unwanted output by preceding rising edge of $\overline{W}$ with rising edge of $\overline{S1}$ by time; TS1HQZ

National Semiconductor

NMC6552 1024-Bit (256 × 4) Static RAM

General Description

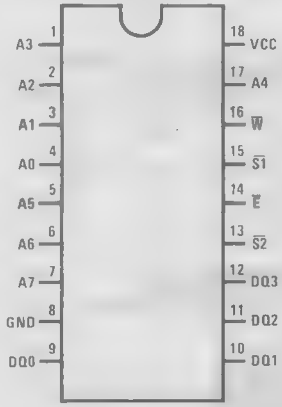
The NMC6552 is a static CMOS random access read/write memory organized as 256 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by the on-chip address input and data output registers. The ENABLE input serves as the device strobe controlling the latching functions. The data I/O terminals, when not output data enabled, represent a high impedance for easy memory expansion.

Features

- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging
- Output data latches
- Select latch for microprocessor interface

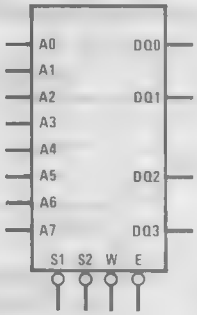
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Order Number NMC6552J-2, NMC6552J-9 or NMC6552J-5
See NS Package J18A

Order Number NMC6552N-5
See NS Package N18A

Pin Names

A0–A7	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ0–DQ3	Data In/Out
$\overline{S1}$, $\overline{S2}$	Chip Selects

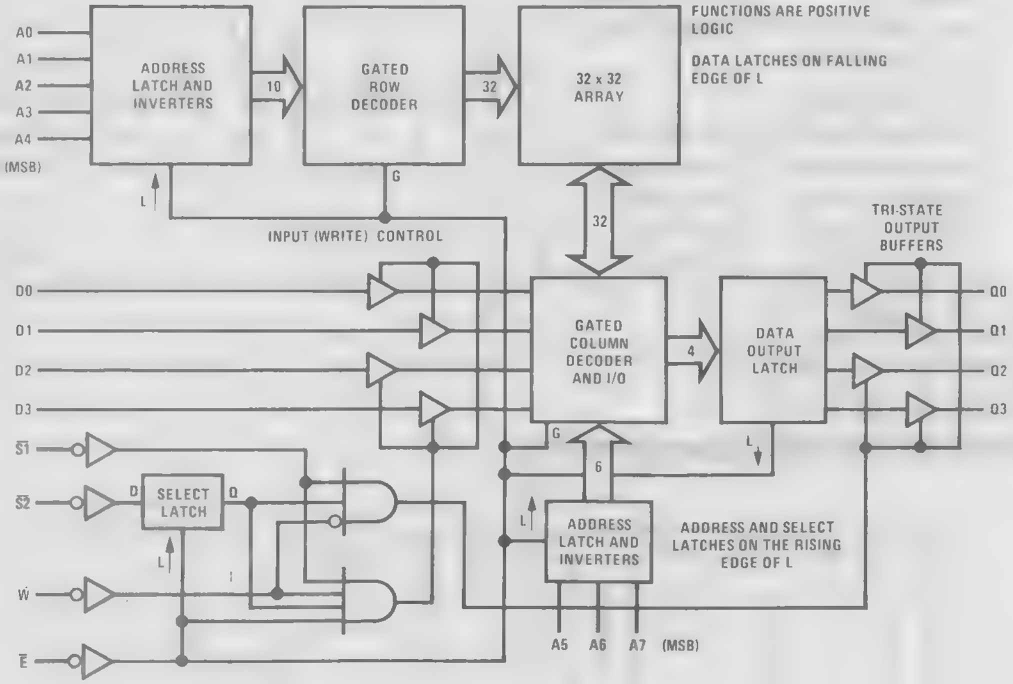
Functional Description

An NMC6552 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the ADDRESS and SELECT 2 ($\overline{S2}$) information into the on-chip registers. The output data latches are transparent when the ENABLE input is LOW, allowing the state of the memory to be presented to the output buffers. The output buffers are enabled when the WRITE ($\overline{W}$) input is HIGH, and the SELECT 1 ($\overline{S1}$) input is LOW.

When performing a read cycle, a minimum ENABLE LOW time is required to assure valid data at the device outputs. This minimum LOW time is defined as the enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle. The data is latched with the rising edge of the ENABLE input, allowing maintenance of output data until the SELECT 1 input goes HIGH.

When performing a write cycle, a minimum ENABLE LOW time is required for new data entry. The write pulse timing is defined by the coincident LOW of the WRITE, ENABLE and SELECT 1 inputs. The input data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, or SELECT 1 inputs, whichever occurs first.

Block Diagram



FUNCTIONS ARE POSITIVE LOGIC

DATA LATCHES ON FALLING EDGE OF L

ADDRESS AND SELECT LATCHES ON THE RISING EDGE OF L

Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	[illegible]	Max
Supply Voltage		
NMC6552B-9	4.5V	5.5V
NMC6552B-2	4.5V	5.5V
NMC6552-9	4.5V	5.5V
NMC6552-2	4.5V	5.5V
NMC6552-5	4.75V	5.25V
Temperature		
NMC6552B-9	−40°C	85°C
NMC6552B-2	−55°C	125°C
NMC6552-9	−40°C	85°C
NMC6552-2	−55°C	125°C
NMC6552-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6552B-9, NMC6552B-2 NMC6552-9, NMC6552-2		NMC6552-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10 1(+25°C)		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC−2.0	VCC+0.3	VCC−2	VCC+0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

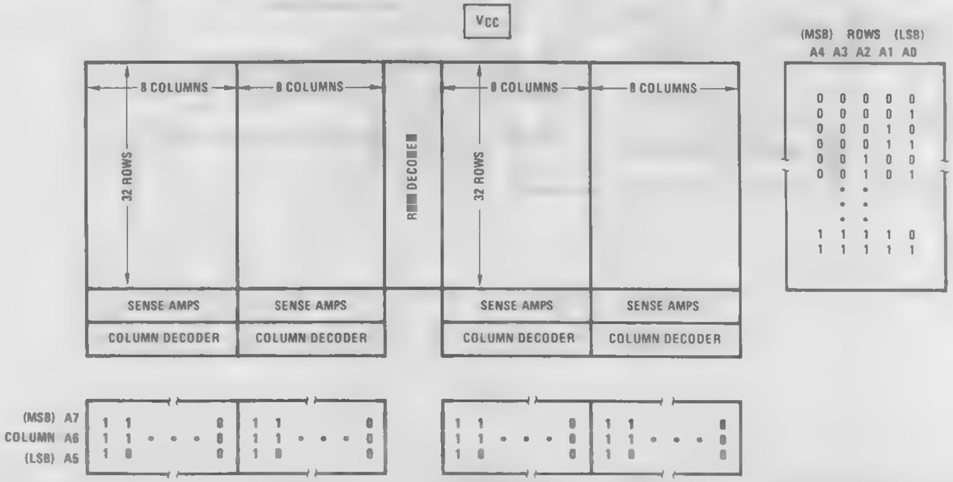
AC Test Conditions

Input Rise and Fall Times: ≤20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

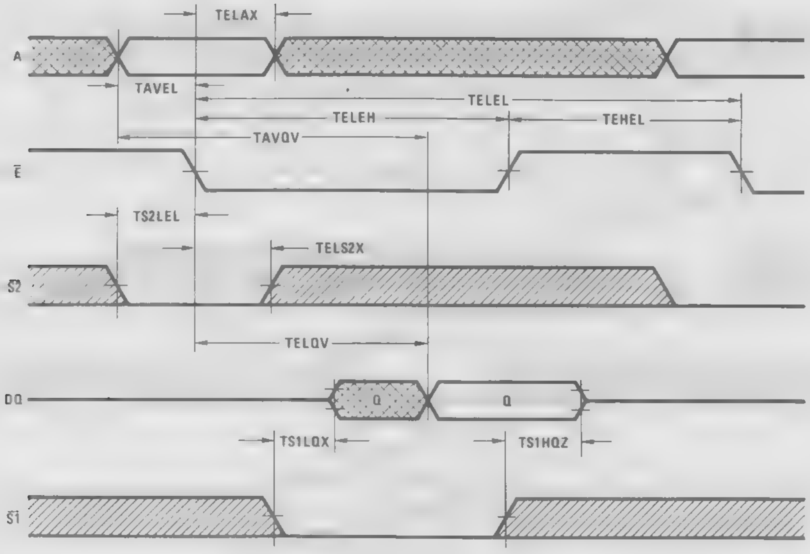
NMC6552 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TELEH	Enable (Ē) Minimum Low Time	220		300		350		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns

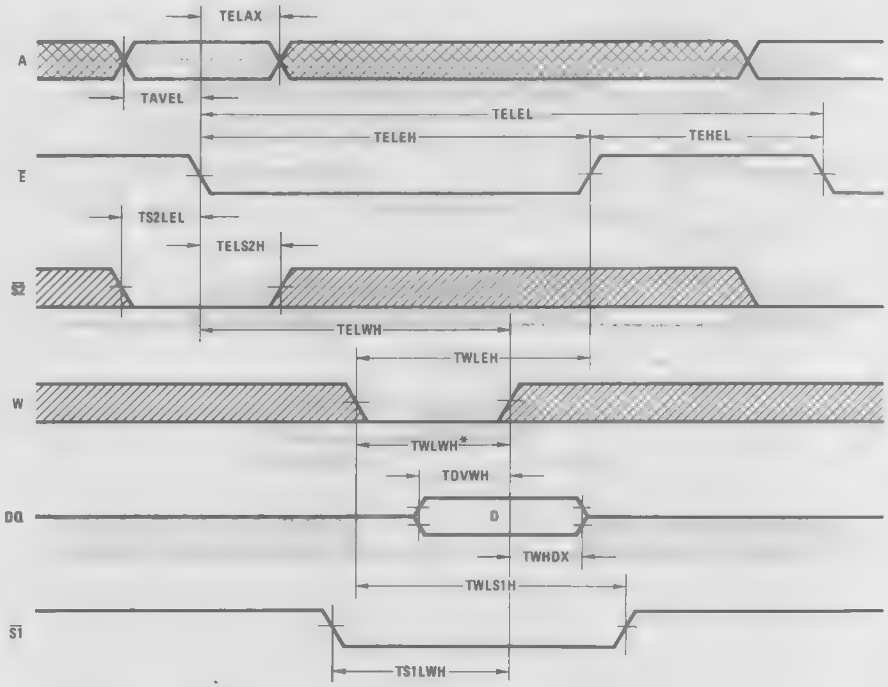
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELEH	Enable (Ē) Minimum Low Time	220		300		350		ns
TWLWH	Write Pulse Width (W̄ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TEHEL	Enable (Ē) Minimum High Time	100		100		150		ns
TDVWH	Data Set-up Time	100		150		170		ns
TELWH	Write Pulse Width (Ē and W̄ Low)	120		180		210		ns
TWLEH	Write Pulse Width (W̄ and Ē Low)	120		180		210		ns
TELS2H	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LWL	Chip Select 1 Write Pulse Hold Time	120		180		210		ns

Write Cycle Waveforms

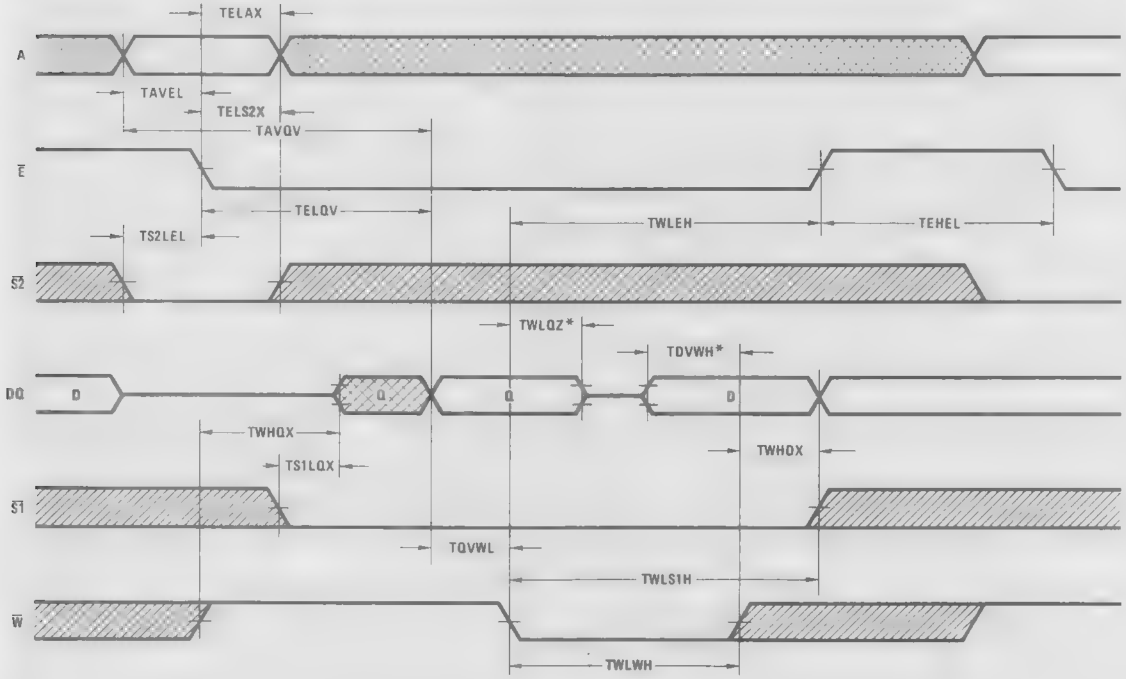


* TWLWH, the write pulse, is the coincidence low of Ē, W̄, and S̄1 inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TDVWH	Data Set-up Time	100		150		170		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	120		180		210		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHQX	Output Enable from Write ($\overline{W}$)		130		150		180	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		130		150		180	ns

Read-Modify-Write Cycle Waveforms



* Avoid bus contention

Section 5

CD4XXX Series Logic

National Semiconductor

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter

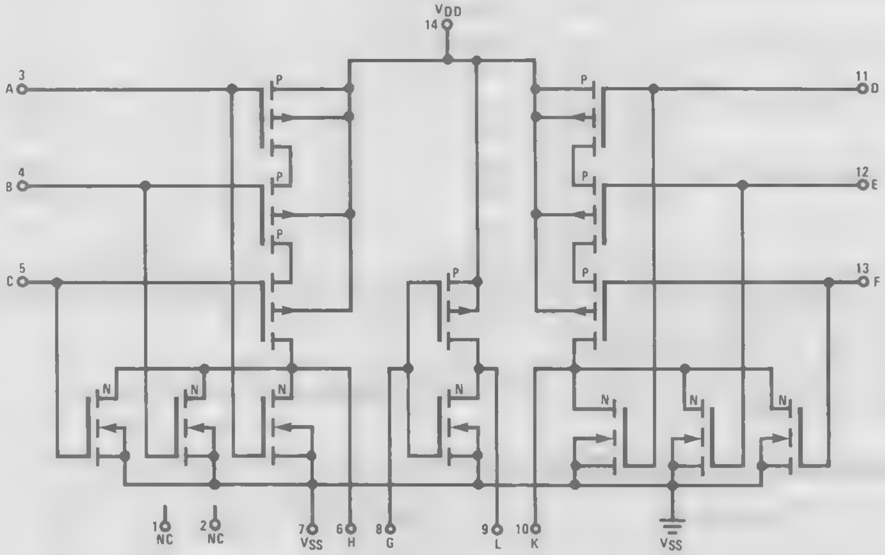
General Description

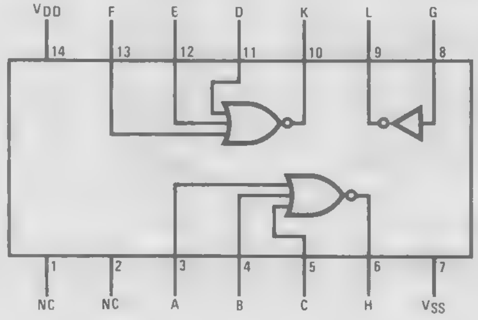
The CD4000M/CD4000C is a monolithic complementary MOS (CMOS) dual 2-input NOR gate plus an inverter. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Schematic and Connection Diagram





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	V_{SS} –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
CD4000M	–55°C to +125°C
CD4000C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3 V to V_{SS} + 15 V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics CD4000M (Note 2)

PARAMETER		CONDITIONS	–55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		0.05			0.05		3	µA
		V_{DD} = 10 V		0.1			0.1		6	µA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.5		1.5			1.4		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.4		1.5			1.5		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.5		0.4			0.28		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.1		0.9			0.65		mA
I_{DP}	High Level Output Current	V_{DD} = 5 V, V_O = 2.5 V	–0.62		–0.5			–0.35		mA
		V_{DD} = 10 V, V_O = 9.5 V	–0.62		–0.5			–0.35		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	–1.0		–0.1	-10^{-5}		–1.0		µA
		V_{DD} = 15 V, V_{IN} = 15 V		1.0		10^{-5}	0.1		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: For the NOR gates V_{NH} and V_{NL} are tested at each input while all other inputs are at V_{SS}.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics CD4000M $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level	V_{DD} = 5 V		40	50	ns
		V_{DD} = 10 V		20	40	ns
t_{PLH}	Propagation Delay Time, Low to High Level	V_{DD} = 5 V		50	95	ns
		V_{DD} = 10 V		25	45	ns
t_{THL}	Transition Time, High to Low Level	V_{DD} = 5 V		50	125	ns
		V_{DD} = 10 V		20	70	ns
t_{TLH}	Transition Time, Low to High Level	V_{DD} = 5 V		70	175	ns
		V_{DD} = 10 V		35	75	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		35		pF

DC Electrical Characteristics C4000C (Note 2)

PARAMETER		CONDITIONS	-40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5\,V$		0.5			0.5		15	µA
		$V_{DD} = 10\,V$		5			5		30	µA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\,V$		0.05			0.05		0.05	V
		$V_{DD} = 10\,V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\,V$	4.95		4.95			4.95		V
		$V_{DD} = 10\,V$	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	$V_{DD} = 5\,V$, $V_O = 1.4\,V$ or $3.6\,V$	1.5		1.5			1.4		V
		$V_{DD} = 10\,V$, $V_O = 2.8\,V$ or $7.2\,V$	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	$V_{DD} = 5\,V$, $V_O = 1.4\,V$ or $3.6\,V$	1.4		1.5			1.5		V
		$V_{DD} = 10\,V$, $V_O = 2.8\,V$ or $7.2\,V$	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current	$V_{DD} = 5\,V$, $V_O = 0.4\,V$	0.35		0.3			0.24		mA
		$V_{DD} = 10\,V$, $V_O = 0.5\,V$	0.72		0.6			0.48		mA
I_{DP}	High Level Output Current	$V_{DD} = 5\,V$, $V_O = 2.5\,V$	-0.35		-0.3			0.24		mA
		$V_{DD} = 10\,V$, $V_O = 9.5\,V$	-0.3		-0.25			-0.2		mA
I_{IN}	Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$	-0.3		-0.3	-10^{5}		1.0		µA
		$V_{DD} = 15\,V$, $V_{IN} = 15\,V$		0.3		10^{5}	0.1		1.0	µA

AC Electrical Characteristics CD4000C $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level	$V_{DD} = 5\,V$		40	80	ns
		$V_{DD} = 10\,V$		20	55	ns
t_{PLH}	Propagation Delay Time, Low to High Level	$V_{DD} = 5\,V$		50	120	ns
		$V_{DD} = 10\,V$		25	65	ns
t_{THL}	Transition Time, High to Low Level	$V_{DD} = 5\,V$		50	200	ns
		$V_{DD} = 10\,V$		20	115	ns
t_{TLH}	Transition Time, Low to High Level	$V_{DD} = 5\,V$		70	300	ns
		$V_{DD} = 10\,V$		35	125	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		35		pF

National Semiconductor

CD4001M/CD4001C Quadruple 2-Input NOR Gate
CD4011M/CD4011C Quadruple 2-Input NAND Gate

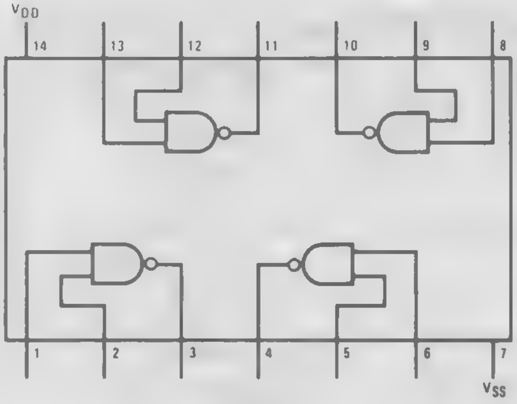
General Description

The CD4001M/CD4001C, CD4011M/CD4011C are monolithic complementary MOS (CMOS) quadruple two-input NOR and NAND gate integrated circuits. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

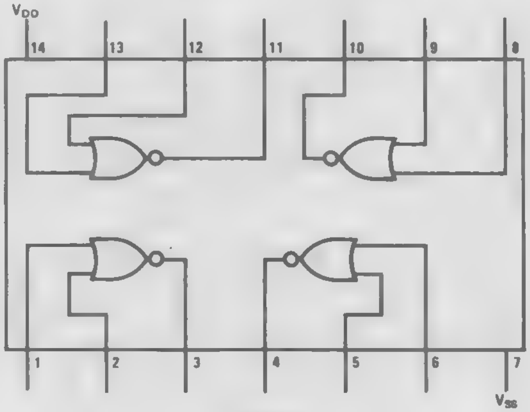
Features

- Wide supply voltage range 3.0 V to 15 V
- Low power 10 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)

Connection Diagrams



TOP VIEW



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage an Any Pin	$V_{SS} - 0.3\,V$ to $V_{DD} + 0.3\,V$	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
CD4001M, CD4011M	−55°C to +125°C	Operating V_{DD} Range	$V_{SS} + 3.0\,V$ to $V_{SS} + 15\,V$
CD4001C, CD4011C	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics — CD4001M, CD4011M

Parameter	Conditions	Limits							Units
		−55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent Device Current	$V_{DD} = 5.0V$		0.05		0.001	0.05		3.0	μA
	$V_{DD} = 10V$		0.1		0.001	0.1		6.0	μA
P_D Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$		0.25		0.005	0.25		15	μW
	$V_{DD} = 10V$		1.0		0.01	1.0		60	μW
V_{OL} Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
V_{OH} Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.95		9.95	10		9.95		V
V_{NL} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
	$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
	$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN Output Drive Current N-Channel (4001)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.5		0.40	1.0		0.28		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP Output Drive Current P-Channel (4001)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	-0.62		-0.5	−2.0		−0.35		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN Output Drive Current N-Channel (4011)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.31		0.25	0.5		0.175		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP Output Drive Current P-Channel (4011)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	0.75		0.6	−1.2		−0.4		mA
I_I Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics — CD4001C, CD4011C

Parameter	Conditions	Limits							Units
		−40°C		25°C			80°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent Device Current	$V_{DD} = 5.0V$		0.5		0.005	0.5		15	μA
	$V_{DD} = 10V$		5.0		0.005	5.0		30	μA
P_D Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$		2.5		0.025	2.5		75	μW
	$V_{DD} = 10V$		50		0.05	50		300	μW
V_{OL} Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
V_{OH} Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.95		9.95	10		9.95		V
V_{NL} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
	$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
	$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN Output Drive Current N-Channel (4001)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.35		0.3	1.0		0.24		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.72		0.6	2.5		0.48		mA
I_DP Output Drive Current P-Channel (4001)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.35		−0.3	−2.0		−0.24		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.3		−0.25	−1.0		−0.2		mA
I_DN Output Drive Current N-Channel (4011)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.145		0.12	0.5		0.095		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.3		0.25	0.6		0.2		mA
I_DP Output Drive Current P-Channel (4011)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.145		−0.12	−0.5		−0.095		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35		−0.3	−1.2		−0.24		mA
I_I Input Current					10				pA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter	Conditions	Min.	Typ.	Max.	Units
CD4001M					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	50	ns
	$V_{DD} = 10V$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	65	ns
	$V_{DD} = 10V$		25	40	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
C_{IN} Input Capacitance	Any Input		5.0		pF
CD4001C					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
C_{IN} Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter	Conditions	Min.	Typ.	Max.	Units
CD4011M					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		50	75	ns
	$V_{DD} = 10V$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		50	75	ns
	$V_{DD} = 10V$		25	40	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		75	125	ns
	$V_{DD} = 10V$		50	75	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		75	100	ns
	$V_{DD} = 10V$		40	60	ns
C_{IN} Input Capacitance	Any Input		5.0		pF
CD4011C					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		50	100	ns
	$V_{DD} = 10V$		25	50	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		50	100	ns
	$V_{DD} = 10V$		25	50	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		75	150	ns
	$V_{DD} = 10V$		50	100	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		75	125	ns
	$V_{DD} = 10V$		40	75	ns
C_{IN} Input Capacitance	Any Input		5.0		pF

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

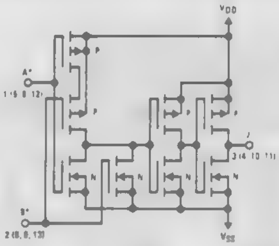
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

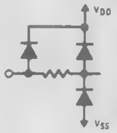
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5 V—10 V—15 V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15 V over full temperature range

Schematic and Connection Diagrams



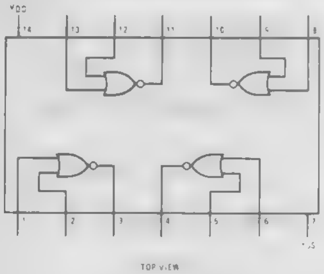


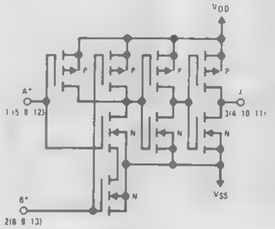
1/4 of device shown

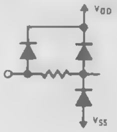
J = $\overline{A + B}$
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4001BC/CD4001BM
Dual-In-Line and Flat Package





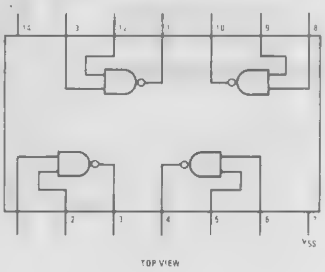


1/4 of device shown

J = $\overline{A \cdot B}$
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4011BC/CD4011BM
Dual-In-Line and Flat Package



Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Package Dissipation	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BM, CD4011BM	−55°C to +125°C
CD4001BC, CD4011BC	−40°C to +85°C

DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

PARAMETER		CONDITIONS	55 C		+25 C			+125 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	µA
		V_{DD} = 10V		0.50		0.005	0.50		15	µA
		V_{DD} = 15V		1.0		0.006	1.0		30	µA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $|I_O| < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $|I_O| < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5	μA
		V_{DD} = 10V		2		0.005	2		15	μA
		V_{DD} = 15V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\|I_O\| < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

AC Electrical Characteristics CD4011BC, CD4011BM

$T_A = 25°C$, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical Temperature Coefficient is 0.3%/°C.

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	V_{DD} = 5V	85	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Typical Performance Characteristics

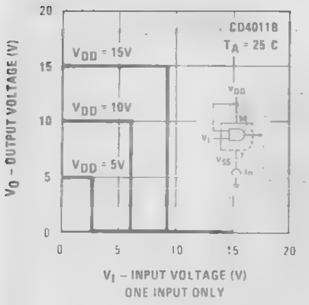


FIGURE 1. Typical Transfer Characteristics

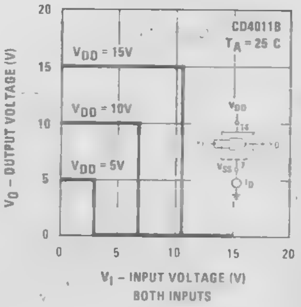


FIGURE 2. Typical Transfer Characteristics

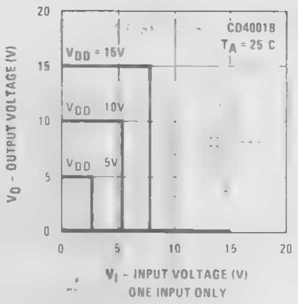


FIGURE 3. Typical Transfer Characteristics

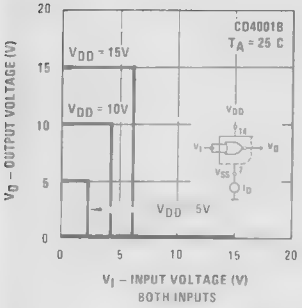


FIGURE 4. Typical Transfer Characteristics

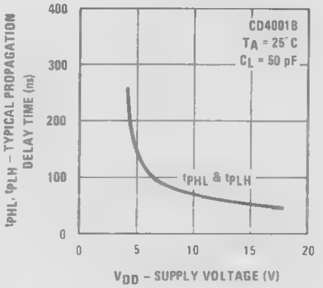


FIGURE 5

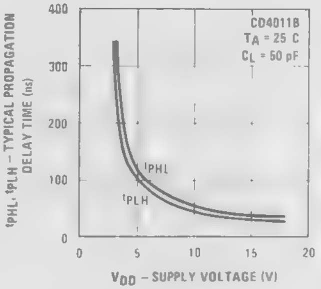


FIGURE 6

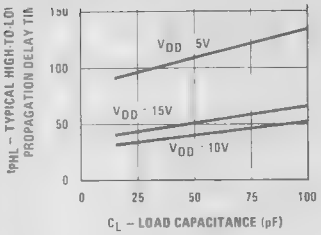


FIGURE 7

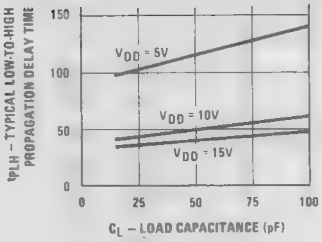


FIGURE 8

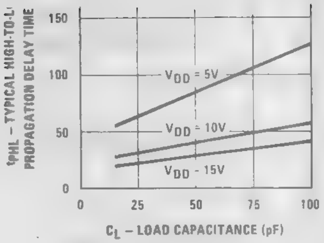


FIGURE 9

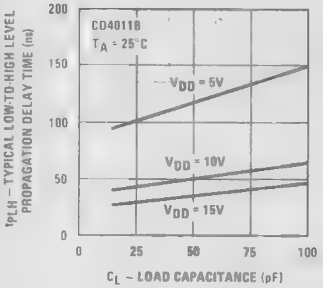


FIGURE 10

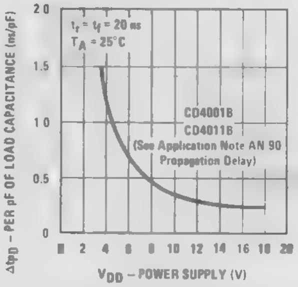


FIGURE 11

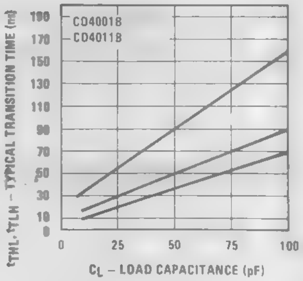


FIGURE 12

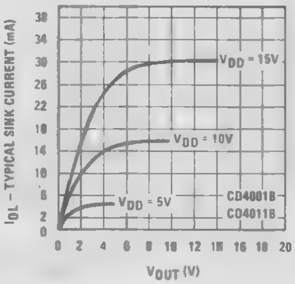


FIGURE 13

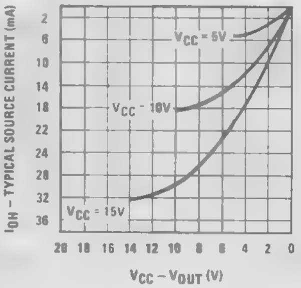


FIGURE 14

National Semiconductor

CD4002M/CD4002C Dual 4-Input NOR Gate CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

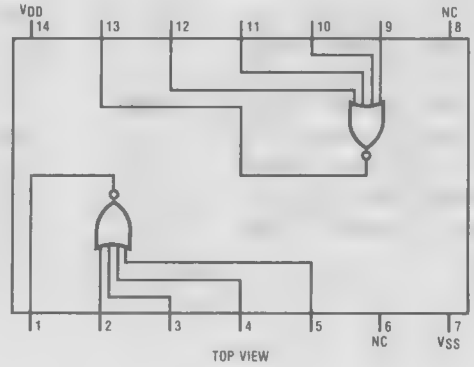
■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Applications

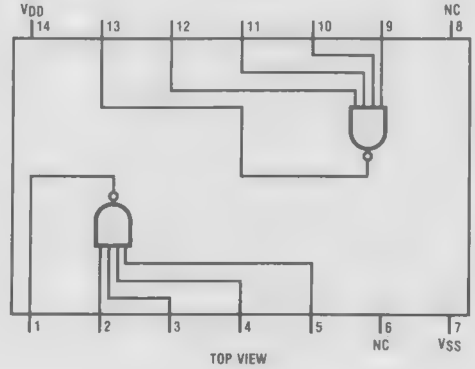
- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams

CD4002



CD4012



Absolute Maximum Ratings (Note 1)

Voltage an Any Pin	$V_{SS} - 0.3\,V$ to $V_{DD} + 0.3\,V$
Operating Temperature Range	
CD4002M, CD4012M	−55°C to +125°C
CD4002C, CD4012C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0\,V$ to $V_{SS} + 15\,V$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics — CD4002M, CD4012M

Parameter		Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD} = 10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD} = 10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
		$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
		$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4002)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4002)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.62		−0.5	−2.0		−0.35		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN	Output Drive Current N-Channel (4012)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4012)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.75		−0.6	−1.2		−0.4		mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4002C, CD4012C

Parameter	Conditions	Limits							Units
		−40°C		25°C			85°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent Device Current	$V_{DD} = 5.0V$		0.5		0.005	0.5		15	μA
	$V_{DD} = 10V$		5.0		0.005	5.0		30	μA
P_D Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$		2.5		0.025	2.5		75	μW
	$V_{DD} = 10V$		50		0.05	50		300	μW
V_{OL} Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
V_{OH} Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.95		9.95	10		9.95		V
V_{NL} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \geqslant 3.5V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
	$V_{DD} = 10V$, $V_O \geqslant 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \leqslant 1.5V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
	$V_{DD} = 10V$, $V_O \leqslant 3.5V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN Output Drive Current N-Channel (4002)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.35		0.3	1.0		0.24		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.72		0.6	2.5		0.48		mA
I_DP Output Drive Current P-Channel (4002)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.35		−0.3	−2.0		−0.24		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.3		−0.25	−1.0		−0.2		mA
I_DN Output Drive Current N-Channel (4012)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.145		0.12	0.5		0.095		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.3		0.25	0.6		0.2		mA
I_DP Output Drive Current P-Channel (4012)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.145		−0.12	−0.5		−0.095		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35		−0.3	−1.2		−0.24		mA
I_I Input Current					10				pA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter	Conditions	Min.	Typ.	Max.	Units
CD4002M					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	50	ns
	$V_{DD} = 10V$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	50	ns
	$V_{DD} = 10V$		25	40	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
C_{IN} Input Capacitance	Any Input		5.0		pF
CD4002C					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
C_{IN} Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter	Conditions	Min.	Typ.	Max.	Units
CD4012M					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		50	75	ns
	$V_{DD} = 10V$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		50	75	ns
	$V_{DD} = 10V$		25	40	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		75	125	ns
	$V_{DD} = 10V$		50	75	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		75	100	ns
	$V_{DD} = 10V$		40	60	ns
C_{IN} Input Capacitance	Any Input		5.0		pF
CD4012C					
t_{PHL} Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		50	100	ns
	$V_{DD} = 10V$		25	50	ns
t_{PLH} Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		50	100	ns
	$V_{DD} = 10V$		25	50	ns
t_{THL} Transition Time High to Low Level	$V_{DD} = 5.0V$		75	150	ns
	$V_{DD} = 10V$		50	100	ns
t_{TLH} Transition Time Low to High Level	$V_{DD} = 5.0V$		75	125	ns
	$V_{DD} = 10V$		40	75	ns
C_{IN} Input Capacitance	Any Input		5.0		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

National Semiconductor

CD4002BM/CD4002BC Dual 4-Input NOR Gate
CD4012BM/CD4012BC Dual 4-Input NAND Gate

General Description

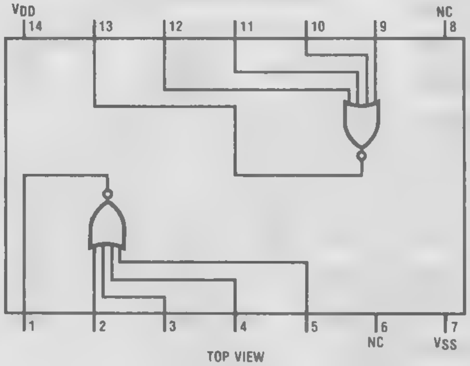
These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fanout of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

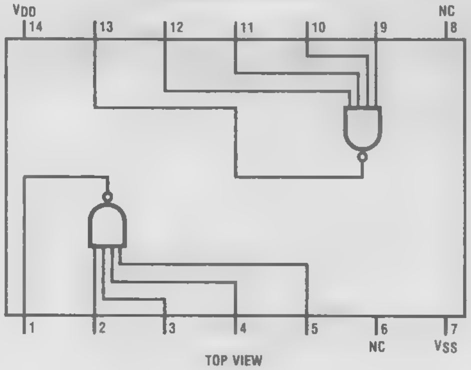
Connection Diagram

CD4002BM/CD4002BC



TOP VIEW

CD4012BM/CD4012BC



TOP VIEW

CD4002BM/CD4002BC, CD4012BM/CD4012BC

5

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 to V_{DD}0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD}	Supply Voltage	3.0 to 15 V
V_{IN}	Input Voltage	0 V to V_{DD} V
T_A	Operating Temperature Range	
	CD4002BM, CD4012BM	−55°C to +125°C
	CD4002BC, CD4012BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4002BM, CD4012BM

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		0.25		0.004	0.25		7.5	μA
	V_{DD} = 10 V		0.5		0.005	0.5		15	μA
	V_{DD} = 15 V		1.0		0.006	1.0		30	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10		9.95		V
	V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.2		0.90		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.0		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.2		−0.90		mA
	V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.0		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.10		-10^{-5}	−0.10		−1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.10		10^5	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

DC Electrical Characteristics (Note 2) — CD4002BC, CD4012BC

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD}=5.0\,V$		1.0		0.004	1.0		7.5	μA
	$V_{DD}=10\,V$		2.0		0.005	2.0		15	μA
	$V_{DD}=15\,V$		4.0		0.006	4.0		30	μA
V_{OL} Low Level Output Voltage	$V_{DD}=5.0\,V$		0.05		0	0.05		0.05	V
	$V_{DD}=10\,V$		0.05		0	0.05		0.05	V
	$V_{DD}=15\,V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD}=5.0\,V$	4.95		4.95	5.0		4.95		V
	$V_{DD}=10\,V$	9.95		9.95	10		9.95		V
	$V_{DD}=15\,V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD}=5\,V$, $V_O=0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
	$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$		3.0		4.50	3.0		3.0	V
	$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD}=5.0\,V$, $V_O=0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
	$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$	7.0		7.0	5.50		7.0		V
	$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$	11		11	8.25		11		V
I_{OL} Low Level Output Current	$V_{DD}=5.0\,V$, $V_O=0.4\,V$	0.52		0.44	0.88		0.36		mA
	$V_{DD}=10\,V$, $V_O=0.5\,V$	1.3		1.1	2.2		0.90		mA
	$V_{DD}=15\,V$, $V_O=1.5\,V$	3.6		3.0	8.0		2.4		mA
I_{OH} High Level Output Current	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	−0.88		−0.36		mA
	$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	−2.2		−0.90		mA
	$V_{DD}=15\,V$, $V_O=13.5\,V$	−3.6		−3.0	−8.0		−2.4		mA
I_{IN} Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.3		-10^{-5}	−0.3		−1.0	μA
	$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHL} Propagation Delay, High to Low Level	$V_{DD}=5.0\,V$		125	250	ns
	$V_{DD}=10\,V$		60	100	ns
	$V_{DD}=15\,V$		45	70	ns
t_{PLH} Propagation Delay, Low to High Level	$V_{DD}=5.0\,V$		125	250	ns
	$V_{DD}=10\,V$		60	100	ns
	$V_{DD}=15\,V$		45	70	ns
t_{THL}, t_{TLH} Transition Time	$V_{DD}=5.0\,V$		100	200	ns
	$V_{DD}=10\,V$		50	100	ns
	$V_{DD}=15\,V$		40	80	ns
C_{IN} Average Input Capacitance (Note 3)	Any Input		5.0	7.5	pF
C_{PD} Power Dissipation Capacity (Note 4)	Any Gate		20		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.

National Semiconductor

CD4006BM/CD4006BC 18-Stage Static Shift Register

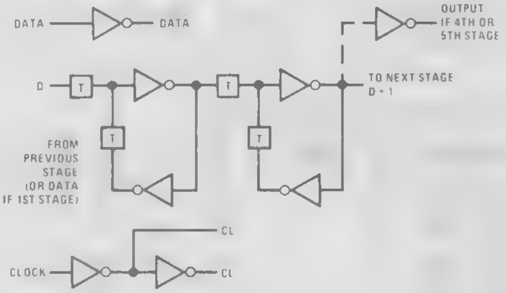
General Description

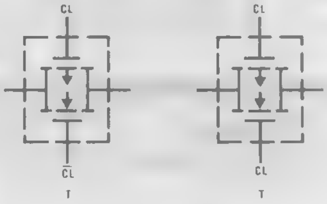
The CD4006BM/CD4006BC 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages, or single register sections of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one package.

Features

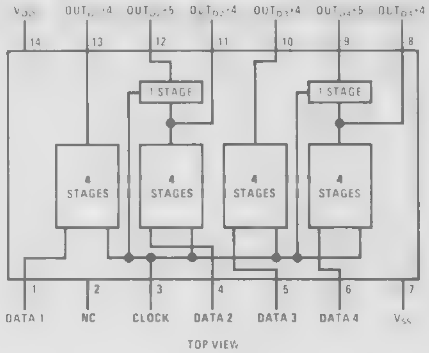
■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 drving 74L or 1 driving 74LS
■ Low clock input capacitance	6 pF (typ.)
■ Medium speed	10 MHz (typ.) (with $V_{DD} = 10V$)
■ Low power	
■ Fully static operation	

Logic Diagrams


DATA
DATA
OUTPUT IF 4TH OR 5TH STAGE
D
T
T
T
T
TO NEXT STAGE D + 1
FROM PREVIOUS STAGE (OR DATA IF 1ST STAGE)
CLOCK
CL
CL



Connection Diagram



Truth Table

D	CL$^{\Delta}$	D+1
0	‾_	0
1	‾_	1
X	_‾	NC

X = Don't care
Δ = Level change
NC = No change

P_D Package Dissipation 500 mW — CD4006BM −55°C to +125°C
T_L Lead Temperature (Soldering, 10 seconds) 300°C — CD4006BC −40°C to +85°C

DC Electrical Characteristics CD4006BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0		0.005	5.0		150	μA
	V_{DD} = 10 V		10		0.010	10		300	μA
	V_{DD} = 15 V		20		0.015	20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10		9.95		V
	V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 5.0 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.1		−0.1	-10^{-5}		−1.0		μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{5}	0.1		1.0	μA

DC Electrical Characteristics CD4006BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20		0.005	20		150	μA
	V_{DD} = 10 V		40		0.010	40		300	μA
	V_{DD} = 15 V		80		0.015	80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10		9.95		V
	V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 5.0 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11		11	8.25		11		V

DC Electrical Characteristics (cont'd) CD4006BC (Note 2)

Parameter		Conditions	−55°C		25°C			85°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OL}	Low Level Output Current	$V_{DD}=5.0\,V$, $V_O=0.4\,V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10\,V$, $V_O=0.5\,V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15\,V$, $V_O=1.5\,V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IL}=0\,V$, $V_{IH}=V_{DD}$								
		$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15\,V$, $V_O=13.5\,V$	−3.6		−0.3	−8.8	−8.8	−2.4		mA
I_{IN}	Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$	−0.3		−0.3	-10^{-5}		−1.0		μA
		$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.3		10^{-5}	0.3		1.0	μA

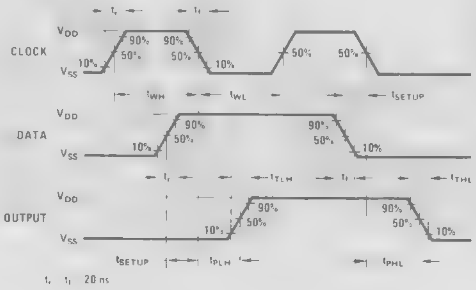
AC Electrical Characteristics CD4006BM/CD4006BC $T_A=25°C$, $C_L=50\,pF$, unless otherwise noted

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PLH}, t_{PHL}	Propagation Delay Time ($t_{PLH}=t_{PHL}$)	$V_{DD}=5.0\,V$		200	400	ns
		$V_{DD}=10\,V$		100	200	ns
		$V_{DD}=15\,V$		80	150	ns
t_{TLH}, t_{THL}	Transition Time ($t_{TLH}=t_{THL}$)	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		50	100	ns
		$V_{DD}=15\,V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width ($t_{WL}=t_{WH}$)	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		45	100	ns
		$V_{DD}=15\,V$		35	70	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time ($t_{RCL}=t_{FCL}$)	$V_{DD}=5.0\,V$			15	μs
		$V_{DD}=10\,V$			15	μs
		$V_{DD}=15\,V$			15	μs
t_{SU}	Minimum Set-up Time	$V_{DD}=5.0\,V$		50	100	ns
		$V_{DD}=10\,V$		25	50	ns
		$V_{DD}=15\,V$		20	40	ns
t_H	Minimum Hold Time	$V_{DD}=5.0\,V$		55	110	ns
		$V_{DD}=10\,V$		35	70	ns
		$V_{DD}=15\,V$		30	60	ns
f_{CL}	Maximum Clock Frequency	$V_{DD}=5.0\,V$	2.5	5.0		MHz
		$V_{DD}=10\,V$	5.0	12		MHz
		$V_{DD}=15\,V$	7.0	16		MHz
C_L	Input Capacitance	Data Input		5.0		pF
		CLK Input		7.5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0\,V$ unless otherwise specified.

Switching Time Waveforms



National Semiconductor

CD4007M/CD4007C Dual Complementary Pair Plus Inverter

General Description

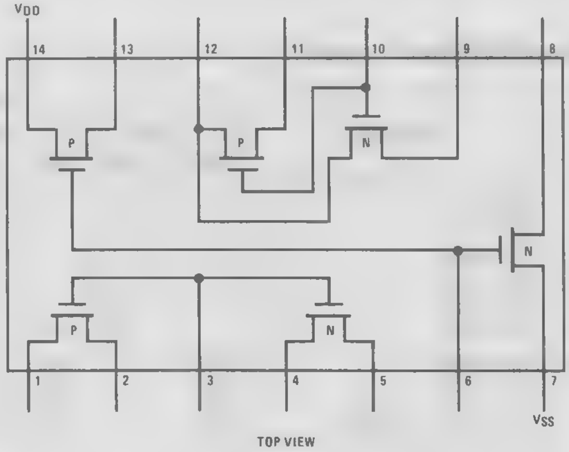
The CD4007M/CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

For proper operation the voltages at all pins must be constrained to be between $V_{SS} - 0.3\,V$ and $V_{DD} + 0.3\,V$ at all times.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{CC} (typ.)

Connection Diagram



Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS}.

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Operating Temperature Range	
CD4007M	−55°C to +125°C
CD4007C	−40°C to +85°C
Storage Tempeature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS}+3.0V$ to $V_{SS}+15V$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics — CD4007M

Parameter		Conditions	Limits									Units
			−55°C			25°C			125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent Device Current	$V_{DD}=5.0V$			0.05		0.001	0.05			3.0	μA
		$V_{DD}=10V$			0.1		0.001	0.1			6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$			0.25		0.005	0.25			15	μW
		$V_{DD}=10V$			1.0		0.001	1.0			60	μW
V_{OL}	Output Voltage Low Level	$V_{DD}=5.0V$			0.05		0	0.05			0.05	V
		$V_{DD}=10V$			0.05		0	0.05			0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V$	4.95			4.95	5.0		4.95			V
		$V_{DD}=10V$	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All inputs)	$V_{DD}=5.0V$, $V_O=3.6V$	1.5			1.5	2.25		1.4			V
		$V_{DD}=10V$, $V_O=7.2V$	3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity (All inputs)	$V_{DD}=5.0V$, $V_O=0.95V$	1.4			1.5	2.25		1.5			V
		$V_{DD}=10V$, $V_O=2.9V$	2.9			3.0	4.5		3.0			V
I_DN	Output Drive Current N-Channel	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.75			0.6	1.0		0.4			mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	1.6			1.3	2.5		0.95			mA
I_DP	Output Drive Current P-Channel	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	−1.75			−1.4	−4.0		−1.0			mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	−1.35			−1.1	−2.5		−0.75			mA
I_I	Input Current						10					pA

DC Electrical Characteristics — CD4007C

Parameter		Conditions	Limits									Units
			−40°C			25°C			85°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent Device Current	$V_{DD}=5.0V$			0.5		0.005	0.5			15	μA
		$V_{DD}=10V$			1.0		0.005	1.0			30	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$			2.5		0.025	2.5			75	μW
		$V_{DD}=10V$			10		0.05	10			300	μW
V_{OL}	Output Voltage Low Level	$V_{DD}=5.0V$			0.05		0	0.01			0.05	V
		$V_{DD}=10V$			0.05		0	0.01			0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V$	4.95			4.95	5.0		4.95			V
		$V_{DD}=10V$	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All inputs)	$V_{DD}=5.0V$, $V_O=3.6V$	1.5			1.5	2.25		1.4			V
		$V_{DD}=10V$, $V_O=7.2V$	3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity (All inputs)	$V_{DD}=5.0V$, $V_O=0.95V$	1.4			1.5	2.25		1.5			V
		$V_{DD}=10V$, $V_O=2.9V$	2.9			3.0	4.5		3.0			V
I_DN	Output Drive Current N-Channel	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.35			0.3	1.0		0.24			mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	1.2			1.0	2.5		0.8			mA
I_DP	Output Drive Current P-Channel	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	−1.3			−1.1	−4.0		−0.9			mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	−0.65			−0.55	−2.5		−0.45			mA
I_I	Input Current						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics

— CD4007M $T_A = 25°C$ and $C_L = 15\,pF$ and rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

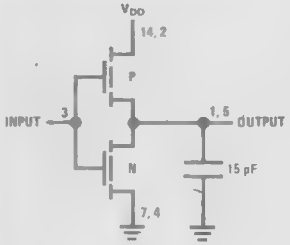
Parameter		Conditions	Min.	Typ.	Max.	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 20	60 40	ns ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 30	75 40	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

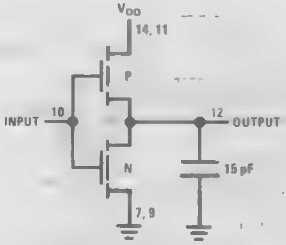
AC Electrical Characteristics

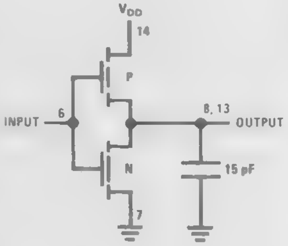
CD4007C $T_A = 25°C$ and $C_L = 15\,pF$ and rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter		Conditions	Min.	Typ.	Max.	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 20	75 50	ns ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 30	100 50	ns ns
C_I	Input Capacitance	Any Input		5		pF

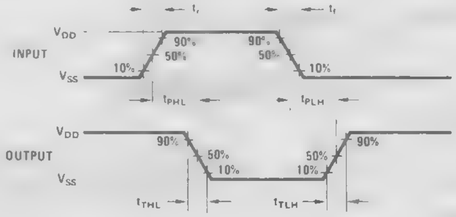
AC Test Circuits







Switching Time Waveforms



$t_r = t_f = 20\,ns$

National Semiconductor

CD4008BM/CD4008BC 4-Bit Full Adder

General Description

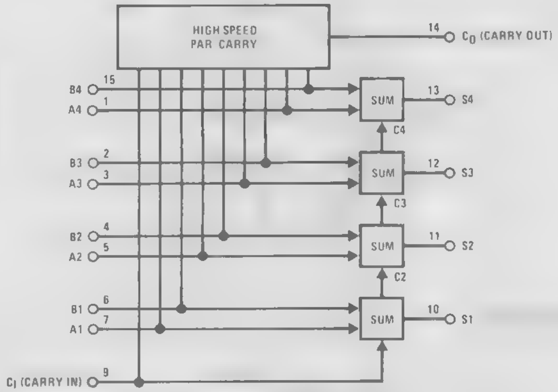
The CD4008B types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008B's. CD4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry in" bit from a previous section. CD4008B outputs include the four sum bits, S1 and S4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and GND.

Features

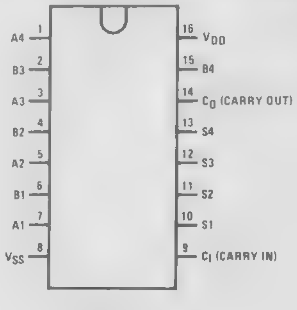
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 4 sum outputs plus parallel look-ahead carry-output
- Quiescent current specified to 15V
- Maximum input leakage of 1 μA at 15V (full package temperature range)

Block Diagram



Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Truth Table

A_i	B_i	C_i	C0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4008BM	−55°C to +125°C
CD4008BC	−40°C to +85°C

DC Electrical Characteristics 4008BM (Note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		5		0.3	5		150	μA
	$V_{DD} = 10V$		10		0.5	10		300	μA
	$V_{DD} = 15V$		20		1.0	20		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0			3.0		3.0	V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0			7.0		V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
	$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	0.25		−0.2	0.35		0.14		mA
	$V_{DD} = 10V$, $V_O = 9.5V$	0.62		0.5	0.8		0.35		mA
	$V_{DD} = 15V$, $V_O = 13.5V$	1.8		1.5	3.5		1.1		mA
I_{IN} Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		0.1		10^{-5}	0.1		1.0	μA
	$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics 4008BC (Note 2)

PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		20		0.5	20		150	μA
	$V_{DD} = 10V$		40		1	40		300	μA
	$V_{DD} = 15V$		80		5	80		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0			3.0		3.0	V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0			7.0		V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V

DC Electrical Characteristics (Cont'd) CD4008BC (Note 2)

PARAMETER		CONDITIONS	-40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.35		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.8		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3			−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3			0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 2000\,k$, input t_r, $t_f = 20\,ns$, unless otherwise specified.

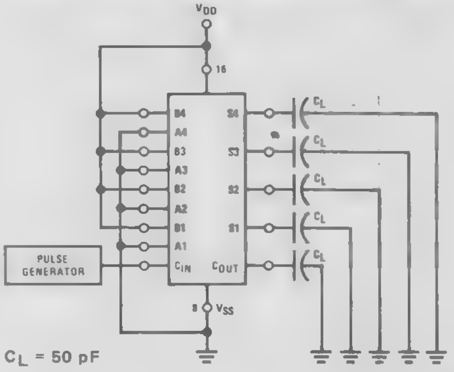
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time					
	Sum In to Sum Out	V_{DD} = 5V		425	750	ns
		V_{DD} = 10V		170	250	ns
		V_{DD} = 15V		125	190	ns
	Carry In to Sum Out	V_{DD} = 5V		320	650	ns
		V_{DD} = 10V		125	225	ns
		V_{DD} = 15V		95	175	ns
	Sum In to Carry Out	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	200	ns
		V_{DD} = 15V		90	160	ns
	Carry In to Carry Out	V_{DD} = 5V		130	245	ns
		V_{DD} = 10V		60	105	ns
		V_{DD} = 15V		45	80	ns
	Carry In to Carry Out	C_L = 15 pF				
		V_{DD} = 5V		100	175	ns
		V_{DD} = 10V		45	75	ns
		V_{DD} = 15V		35	60	ns
t_{THL}	High-to-Low Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Transition Time	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
C_{IN}	Average Input Capacitance			5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Note 3		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

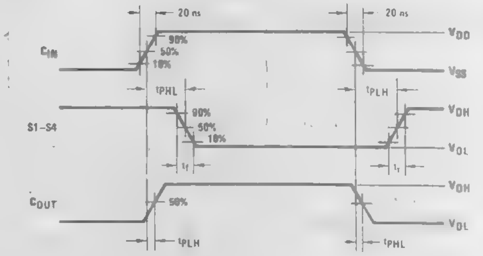
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

AC Test Circuit and Switching Time Waveforms



C_L = 50 pF



National Semiconductor

CD4009M/CD4009C Hex Buffers (Inverting) CD4010M/CD4010C Hex Buffers (Non-Inverting)

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

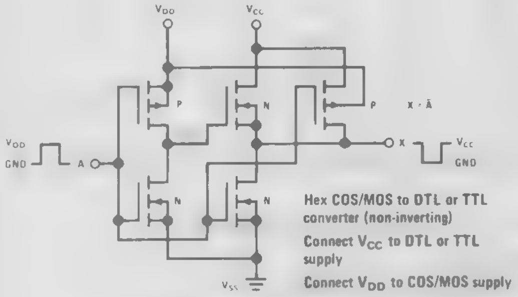
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Low power	100 nW (typ.)
■ High noise immunity	$0.45 V_{DD}$ (typ.)
■ High current sinking capability	8 mA (min.) at $V_O = 0.5 V$ and $V_{DD} = 10 V$

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Schematic Diagrams

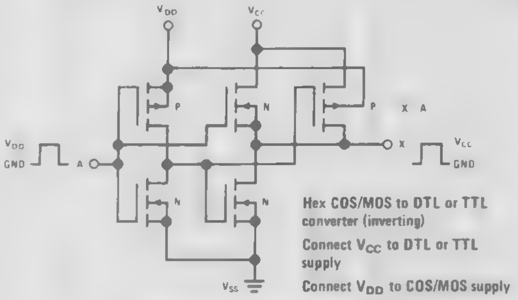


Hex COS/MOS to DTL or TTL converter (non-inverting)

Connect V_{CC} to DTL or TTL supply

Connect V_{DD} to COS/MOS supply

CD4009M/CD4009C



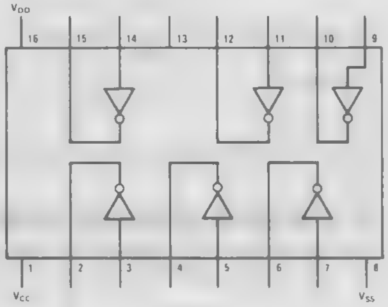
Hex COS/MOS to DTL or TTL converter (inverting)

Connect V_{CC} to DTL or TTL supply

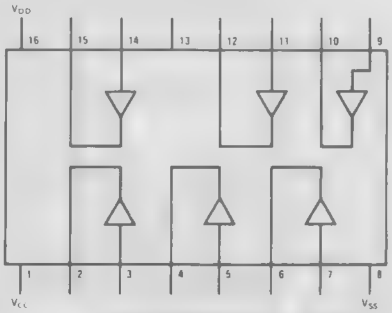
Connect V_{DD} to COS/MOS supply

CD4010M/CD4010C

Connection Diagrams



TOP VIEW



TOP VIEW

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)		V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	CD40XXM	–55°C to +125°C
	CD40XXC	–40°C to +85°C
Storage Temperature Range		–65°C to +150°C
Package Dissipation		500mW
Lead Temperature (Soldering, 10 seconds)		300°C
Operating V_{DD} Range		V_{SS} + 3V to V_{SS} + 15V

DC Electrical Characteristics

CHARACTERISTICS	TEST CONDITIONS VOLTS		LIMITS															UNITS
			CD40XXM							CD40XXC								
			–55°C		+25°C			+125°C		–40°C		+25°C			+125°C			
	V_O	V_{DD}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current (I_L)		5		0.3		0.01	0.3		20		3		0.03	3		42	µA
		10		0.5		0.01	0.5		30		5		0.05	5		70	µA
Quiescent Device Dissipation/Package (P_D)		5		1.5		0.05	1.5		100		15		0.15	15		210	µW
		10		5		0.1	5		300		50		0.5	50		700	µW
Output Voltage Low Level (V_{OL})		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
		10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
High Level (V_{OH})		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
		10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
Noise Immunity (All Inputs)																	
(V_{NL}) CD4009M	V_O>4.0	5	1		1	2.25		0.9		1		1	2.25		0.9		V
	V_O>8.0	10	2		2	4.5		1.9		2		2	4.5		1.9		V
(V_{NL}) CD4010M	V_O>1.5	5	1.6		1.5	2.25		1.4		1.6		1.5	2.25		1.4		V
	V_O>3.0	10	3.2		3	4.5		2.9		3.2		3	4.5		2.9		V
(V_{NH})	V_O>3.5	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
	V_O≥7.0	10	2.9		3	4.5		3		2.9		3	4.5		3		V
Output Drive Current N-Channel (I_DN)	0.4	5	3.75		3	4		2.1		3.6		3			2.4		mA
	0.5	10	10		8	10		5.6		9.6		8			6.4		mA
P-Channel (I_DP)	2.5	5	–1.85		–1.25	–1.75		–0.9		–1.5		–1.25			–1		mA
	9.5	10	–0.9		–0.6	–0.8		–0.4		–0.72		–0.6			–0.48		mA
Input Current (I_I)						10							10				pA

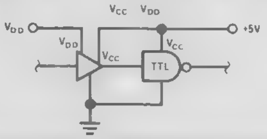
Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15\,pF$, unless otherwise noted

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			CD40XXM			CD40XXC			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	V_{CC} V_{DD}	5	—	15	55	—	15	70	ns
		10	—	10	30	—	10	40	
	V_{DD} 10V V_{CC} 5V		—	10	25	—	10	35	
Low-to High Level (t_{PLH})	V_{CC} V_{DD}	5	—	50	80	—	50	100	ns
		10	—	25	55	—	25	70	
	V_{DD} 10V V_{CC} 5V		—	15	30	—	15	40	
Transition Time High-to-Low Level (t_{THL})	V_{CC} V_{DD}	5	—	20	45	—	20	60	ns
		10	—	16	40	—	16	50	
Low-to High Level (t_{TLH})	V_{CC} V_{DD}	5	—	80	125	—	80	160	ns
		10	—	50	100	—	50	120	
Input Capacitance (C_I)	Any Input		—	5	—	—	5	—	pF

Typical Applications



National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

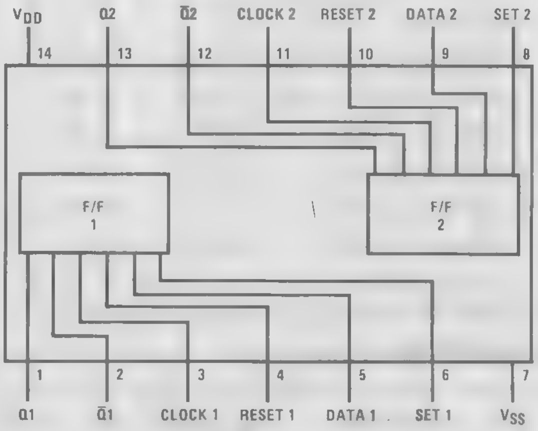
Wide supply voltage range	3.0 V to 15 V
High noise immunity	0.45 V_{DD} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Truth Table

CL†	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
† = Level change
x = Don't care case

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4013BM	−55°C to +125°C
CD4013BC	−40°C to +85°C

DC Electrical Characteristics 4013BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	0.64		−0.51	−0.88		0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 13.5V	4.2		−3.4	8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics 4013BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4.0			4.0		30	μA
		V_{DD} = 10V		8.0			8.0		60	μA
		V_{DD} = 15V		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4013BC (Note 2)

PARAMETER		CONDITIONS	-40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$I_O < 1.0\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	-0.52		0.44	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.3		-1.1	2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	3.6		-3.0	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		0.3		10^{-5}	0.3		1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	µA

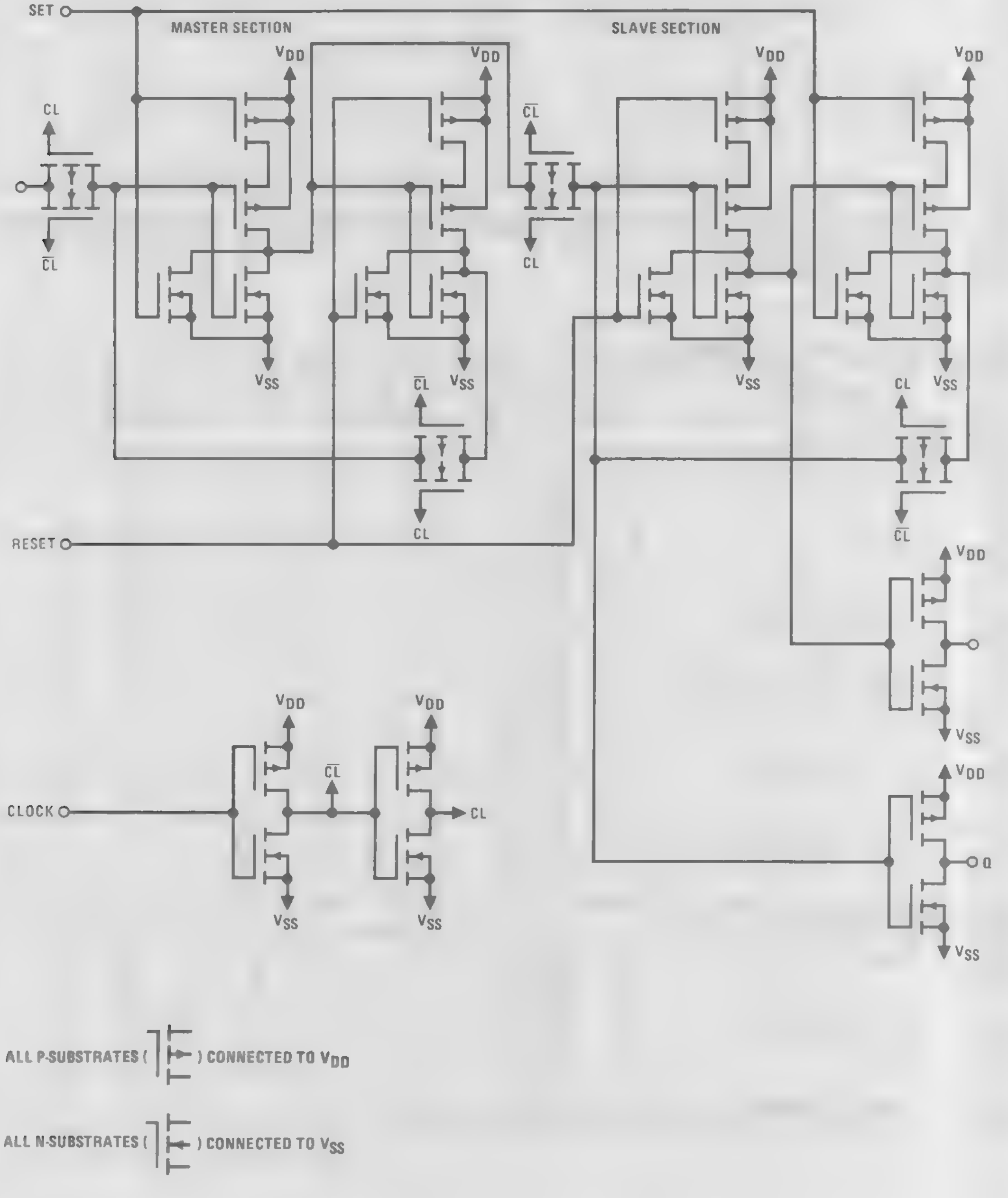
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

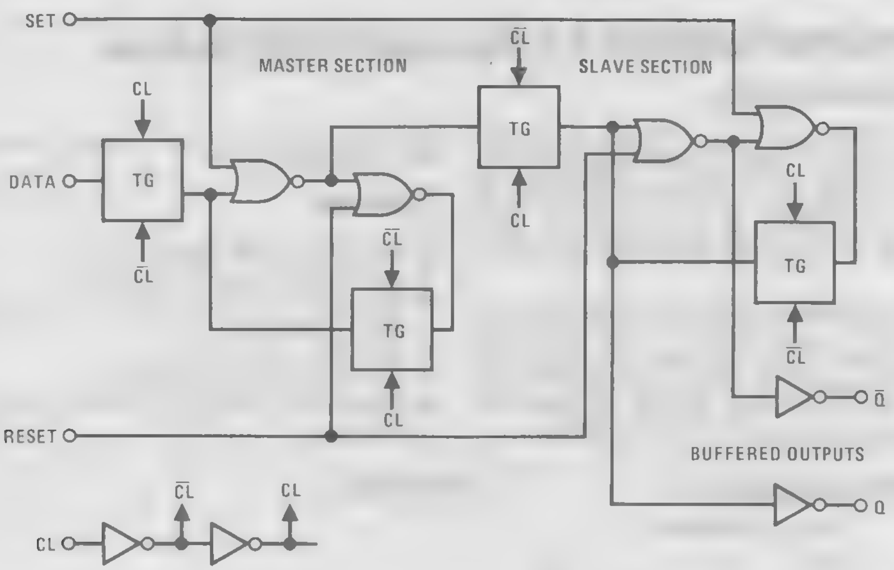
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	120	ns
t_{THL}, or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, or t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			15	µs
		$V_{DD} = 10V$			10	µs
		$V_{DD} = 15V$			5	µs
t_{SU}	Minimum Set-Up Time	$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		15	30	ns
		$V_{DD} = 15V$		12	25	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.5	5		MHz
		$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

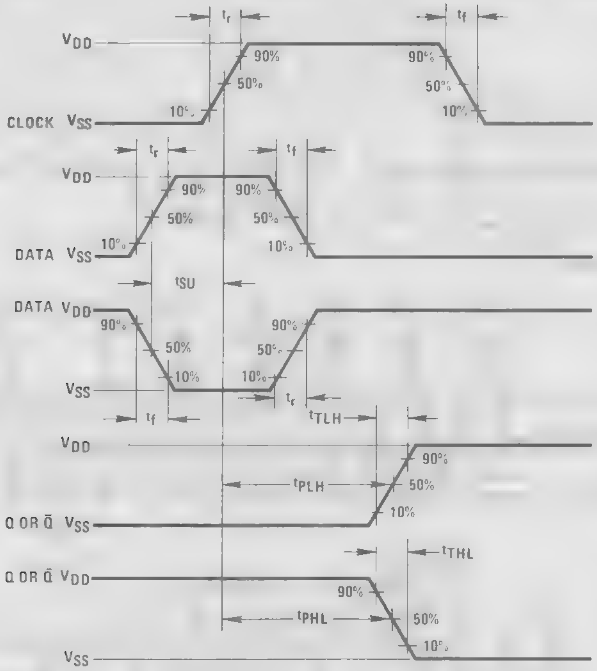
Schematic Diagram



Logic Diagram



Switching Time Waveforms



National Semiconductor

February 1980

CD4014BM/CD4014BC 8-Stage Static Shift Register

General Description

The CD4014BM/CD4014BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

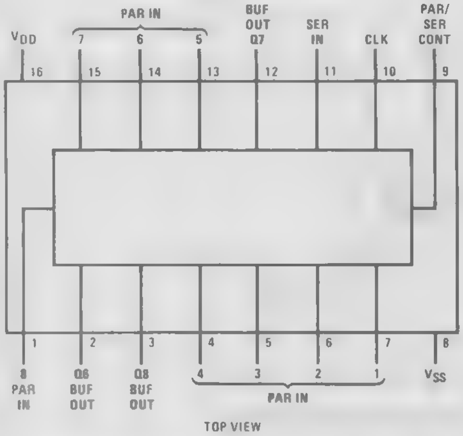
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range—3.0V to 15V
- High noise immunity—0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package

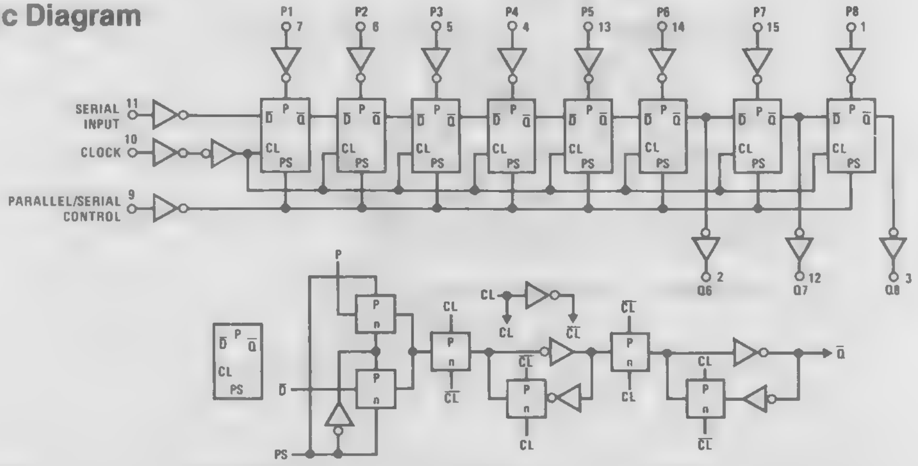


Truth Table

CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n	
⟋	X	1	0	0	0	0	
⟋	X	1	1	0	1	0	
⟋	X	1	0	1	0	1	
⟋	X	1	1	1	1	1	
⟋	0	0	X	X	0	Q_{n-1}	
⟋	1	0	X	X	1	Q_{n-1}	
⟍	X	X	X	X	Q1	Q_n	No Change

*Level change
X = Don't care case

Logic Diagram



Absolute Maximum Ratings

(Notes 1 & 2)

V_{DD}	Supply Voltage	−0.5 to +18 V
V_{IN}	Input Voltage	−0.5 to V_{DD} + 0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD}	Supply Voltage	3.0 to 15 V
V_{IN}	Input Voltage	0 to V_{DD}
T_A	Operating Temperature Range	
	CD4014BM	−55°C to +125°C
	CD4014BC	40°C to 85°C

DC Electrical Characteristics (Note 2) — CD4014BM

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		5		0.1	5		150	μA
		$V_{DD}=10V$		10		0.2	10		300	μA
		$V_{DD}=15V$		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$, $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$, $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$, $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$, $\|I_O\|<1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$, $\|I_O\|<1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4014BC

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		20		0.1	20		150	μA
		$V_{DD}=10V$		40		0.2	40		300	μA
		$V_{DD}=15V$		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$, $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$, $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$, $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$, $\|I_O\|<1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$, $\|I_O\|<1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

Parameter		Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		200	320	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	2.8	4		MHz
		$V_{DD} = 10V$	6	12		MHz
		$V_{DD} = 15V$	8	16		MHz
t_W	Minimum Clock Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
t_rCL, t_fCL	Clock Rise and Fall Time (Note 3)	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			15	μs
t_s	Minimum Set-up Time (Note 5)					
	Serial Input	$V_{DD} = 5V$		60	120	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns
	Parallel Inputs	$V_{DD} = 5V$		80	160	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns
	Parallel/Serial Control	$V_{DD} = 5V$		100	200	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_H	Minimum Hold Time	$V_{DD} = 5V$			0	ns
	Serial In, Parallel In, $t_s \geq 400$ ns	$V_{DD} = 10V$			10	ns
	Parallel/Serial Control	$V_{DD} = 15V$			15	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)			110		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

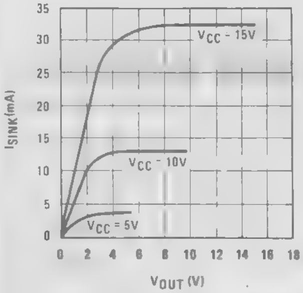
Note 2: $V_{SS} = 0V$ unless otherwise specified.

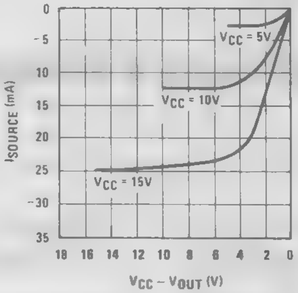
Note 3: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

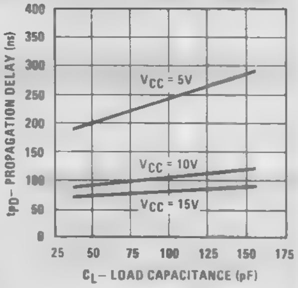
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Note 5: Set-up times are measured with reference to clock and a fixed hold time (t_H) as specified.

Typical Performance Characteristics







National Semiconductor

CD4015BM/CD4015BC DUAL 4-BIT Static Shift Register

General Description

The CD4015BM/CD4015BC contains two identical, 4-stage, serial-input/parallel-output registers with independent "Data," "Clock," and "Reset" inputs. The logic level present at the input of each stage is transferred to the output of that stage at each positive-going clock transition. A logic high on the "Reset" input resets all four stages covered by that input. All inputs are protected from static discharge by a series resistor and diode clamps to V_{DD} and V_{SS}.

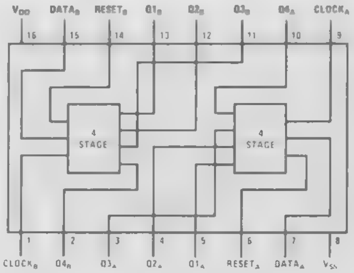
Features

Wide supply voltage range	3.0 V to 18 V
High noise immunity	0.45 V_{DD} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
Medium speed operation	8 MHz (typ) clock rate
Fully static design	@$V_{DD} - V_{SS} = 10$ Volts

Applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

Connection Diagram and Truth Table

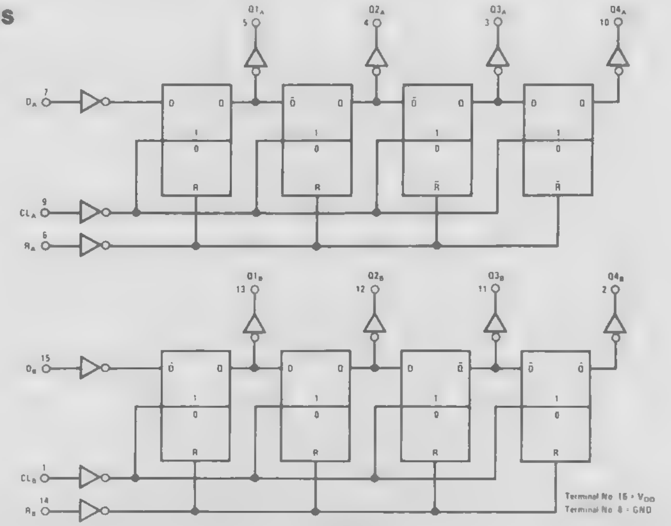


CL▲	D	R	Q_1	Q_n	
↗	0	0	0	Q_{n-1}	
↗	1	0	1	Q_{n-1}	
↘	X	0	Q_1	Q_n	(No change)
X	X	1	0	0	

▲ Level change

X Don't care case

Logic Diagrams



Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	-0.5 to $+18 V_{DC}$
V_{IN}	Input Voltage	-0.5 to $V_{DD} + 0.5 V_{DC}$
T_S	Storage Temperature Range	−65 to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD}	DC Supply Voltage	$+3$ to $+15 V_{DC}$
V_{IN}	Input Voltage	0 to $V_{DD} V_{DC}$
T_A	Operating Temperature Range	
	CD4015BM	−55°C to +125°C
	CD4015BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4015BM

	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	μA
		$V_{DD} = 10V$		10		0.010	10		300	μA
		$V_{DD} = 15V$		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$; or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics (Note 2) — CD4015BC

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.005	20		150	μA
		$V_{DD} = 10V$		40		0.010	40		300	μA
		$V_{DD} = 15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$; or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = OV$ unless otherwise specified.

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50 pF$, $R_L = 200 K$, $t_r = t_f = 20 ns$, unless otherwise specified.

Clocked Operation	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propogation Delay Time	$V_{DD} = 5V$		230	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	40	ns
t_{WL}, t_{WM}	Minimum Clock Pulse-Width	$V_{DD} = 5V$		160	250	ns
		$V_{DD} = 10V$		60	110	ns
		$V_{DD} = 15V$		50	100	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	$V_{DD} = 5V$			15	μS
		$V_{DD} = 10V$			15	μS
		$V_{DD} = 15V$			15	μS
t_{SU}	Minimum Data Set-Up Time	$V_{DD} = 5V$		50	100	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2	3.5		MHz
		$V_{DD} = 10V$	4.5	8		MHz
		$V_{DD} = 15V$	6	11		MHz
C_{IN}	Input Capacitance	Clock Input		7.5	10	pF
		Other Inputs		5	7.5	pF
Reset Operation						
$t_{PHL(R)}$	Propogation Delay Time	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		135	250	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns

CD4016BM/CD4016BC Quad Bilateral Switch

General Description

The CD4016BM/CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BM/CD4066BC.

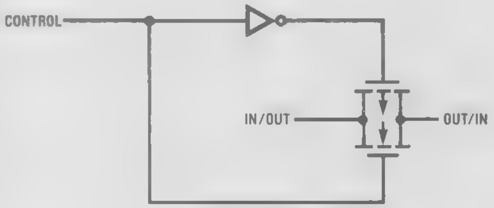
Features

- Wide supply voltage range 3V to 15V
- Wide range of digital and analog switching ±7.5 V_{PEAK}
- "ON" resistance for 15V operation 400Ω (typ.)
- Matched "ON" resistance over 15V signal input $\Delta R_{ON} = 10\Omega$ (typ.)
- High degree of linearity 0.4% distortion (typ.) @ $f_{IS} = 1\text{ kHz}$, $V_{IS} = 5\text{ Vp-p}$, $V_{DD} - V_{SS} = 10V$, $R_L = 10\text{ k}\Omega$
- Extremely low "OFF" switch leakage 0.1 nA (typ.) @ $V_{DD} - V_{SS} = 10V$ $T_A = 25\,°C$
- Extremely high control input impedance $10^{12}\Omega$ (typ.)
- Low crosstalk between switches −50 dB (typ.) @ $f_{IS} = 0.9\text{ MHz}$, $R_L = 1\text{ k}\Omega$
- Frequency response, switch "ON" 40 MHz (typ.)

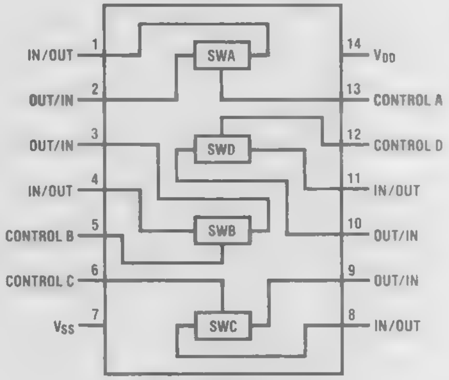
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} Supply Voltage	$-0.5V$ to $+18V$
V_{IN} Input Voltage	$-0.5V$ to $V_{DD}+0.5V$
T_S Storage Temperature Range	$-65°C$ to $+150°C$
P_D Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions
(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4016BM	$-55°C$ to $+125°C$
CD4016BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4016BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD}=5V$		0.25		0.01	0.25		7.5	μA
	$V_{DD}=10V$		0.5		0.01	0.5		15	μA
	$V_{DD}=15V$		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs									
R_{ON} "ON" Resistance	$R_L=10k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$, $V_{IS}=V_{SS}$ or V_{DD}								
	$V_{DD}=10V$		600		250	660		960	Ω
	$V_{DD}=15V$		360		200	400		600	Ω
	$R_L=10k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$								
	$V_{DD}=10V$, $V_{IS}=4.75$ to $5.25V$		1870		850	2000		2600	Ω
	$V_{DD}=15V$, $V_{IS}=7.25$ to $7.75V$		775		400	850		1230	Ω
ΔR_{ON} Δ "ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L=10k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
	$V_{DD}=10V$				15				Ω
	$V_{DD}=15V$				10				Ω
I_{IS} Input or Output Leakage Switch "OFF"	$V_C=0$, $V_{DD}=15V$ $V_{IS}=15V$ and 0V, $V_{OS}=0V$ and 15V		±50		±0.1	±50		±500	nA
Control Inputs									
V_{ILC} Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD} $V_{OS}=V_{DD}$ and V_{SS} $I_{IS}=\pm10\mu A$								
	$V_{DD}=5V$		0.9			0.7		0.5	V
	$V_{DD}=10V$		0.9			0.7		0.5	V
	$V_{DD}=15V$		0.9			0.7		0.5	V
V_{IHC} High Level Input Voltage	$V_{DD}=5V$	3.5		3.5			3.5		V
	$V_{DD}=10V$ (see Note 6 and	7.0		7.0			7.0		V
	$V_{DD}=15V$ Figure 8)	11.0		11.0			11.0		V
I_{IN} Input Current	$V_{DD}-V_{SS}=15V$ $V_{DD}\geqslant V_{IS}\geqslant V_{SS}$ $V_{DD}\geqslant V_C\geqslant V_{SS}$		±0.1		$\pm10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics CD4016BC (Note 2)

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1.0		0.01	1.0		7.5	μA
		$V_{DD} = 10V$		2.0		0.01	2.0		15	μA
		$V_{DD} = 15V$		4.0		0.01	4.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L = 10 k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_C = V_{DD}$, $V_{IS} = V_{SS}$ or V_{DD}								
		$V_{DD} = 10V$		610		275	660		840	Ω
		$V_{DD} = 15V$		370		200	400		520	Ω
		$R_L = 10 k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_C = V_{DD}$								
		$V_{DD} = 10V$, $V_{IS} = 4.75$ to $5.25V$		1900		850	2000		2380	Ω
		$V_{DD} = 15V$, $V_{IS} = 7.25$ to $7.75V$		790		400	850		1080	Ω
ΔR_{ON}	Δ "ON" Resistance (Between any 2 of 4 Switches) (In Same Package)	$R_L = 10 k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		$V_{DD} = 10V$				15				Ω
		$V_{DD} = 15V$				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C = 0$, $V_{DD} = 15V$ $V_{IS} = 0V$ or $15V$ $V_{OS} = 15V$ or $0V$		±50		±0.1	±50		±200	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10 \mu A$								
		$V_{DD} = 5V$		0.9			0.7		0.4	V
		$V_{DD} = 10V$		0.9			0.7		0.4	V
		$V_{DD} = 15V$		0.9			0.7		0.4	V
V_{IHC}	High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$ (see Note 6 and	7.0		7.0			7.0		V
		$V_{DD} = 15V$ *Figure 8)*	11.0		11.0			11.0		V
I_{IN}	Input Current	$V_{CC} - V_{SS} = 15V$ $V_{DD} \geqslant V_{IS} \geqslant V_{SS}$ $V_{DD} \geqslant V_C \geqslant V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $t_r = t_f = 20 ns$ and $V_{SS} = 0V$ unless otherwise specified

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50 pF$, *(Figure 1)* $R_L = 200k$				
		$V_{DD} = 5V$		58	100	ns
		$V_{DD} = 10V$		27	50	ns
		$V_{DD} = 15V$		20	40	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0 k\Omega$, $C_L = 50 pF$, *(Figures 2 and 3)*				
		$V_{DD} = 5V$		20	50	ns
		$V_{DD} = 10V$		18	40	ns
		$V_{DD} = 15V$		17	35	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time *Control Input to Signal* Output Logical Level to High Impedance	$R_L = 1.0 k\Omega$, $C_L = 50 pF$, *(Figures 2 and 3)*				
		$V_{DD} = 5V$		15	40	ns
		$V_{DD} = 10V$		11	25	ns
		$V_{DD} = 15V$		10	22	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$ $R_L = 10 k\Omega$, $V_{IS} = 5 V_{P-P}$, $f = 1 kHz$, *(Figure 4)*		0.4		%

AC Electrical Characteristics (Cont'd)

$T_A = 25°C$, $t_r = t_f = 20 ns$ and $V_{SS} = 0V$ unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
	Frequency Response — Switch "ON" (Frequency at −3dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1 kΩ$, $V_{IS} = 5 V_{P\text{-}P}$, $20 \text{ Log}_{10} V_{OS}/V_{OS}$ (1 kHz) − dB, *(Figure 4)*		40		MHz
	Feedthrough — Switch "OFF" (Frequency at −50dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1 kΩ$, $V_{IS} = 5 V_{P\text{-}P}$, $20 \text{ Log}_{10} (V_{OS}/V_{IS}) = -50 dB$, *(Figure 4)*		1.25		MHz
	Crosstalk Between Any Two Switches (Frequency at −50dB)	$V_{DD} = V_{C(A)} = 5V$; $V_{SS} = V_{C(B)} = -5V$, $R_L = 1 kΩ$, $V_{IS(A)} = 5 V_{P\text{-}P}$, $20 \text{ Log}_{10} (V_{OS(B)}/V_{OS(A)}) = -50 dB$, *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10 kΩ$ $R_{IN} = 1 kΩ$, $V_{CC} = 10V$ Square Wave, $C_L = 50 pF$ *(Figure 6)*		150		$mV_{P\text{-}P}$
	Maximum Control Input	$R_L = 1 kΩ$, $C_L = 50 pF$, *(Figure 7)* $V_{OS(f)} = ½ V_{OS}(1 kHz)$				
		$V_{DD} = 5V$		6.5		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		9.0		MHz
C_{IS}	Signal Input Capacitance			4		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		4		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.2		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: If the switch input is held at V_{DD}, V_{IHC} is the control input level that will cause the switch output to meet the standard "B" series V_{OH} and I_{OH} output levels. If the analog switch input is conected to V_{SS}, V_{IHC} is the control input level — which allows the switch to *sink* standard "B" series $|I_{OH}|$, high level current, and still maintain a $V_{OL} \leqslant$ standard "B" series. See *Figure 8*.

AC Test Circuits and Switching Time Waveforms

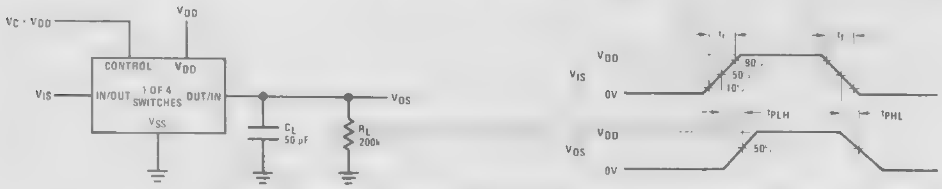


Figure 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

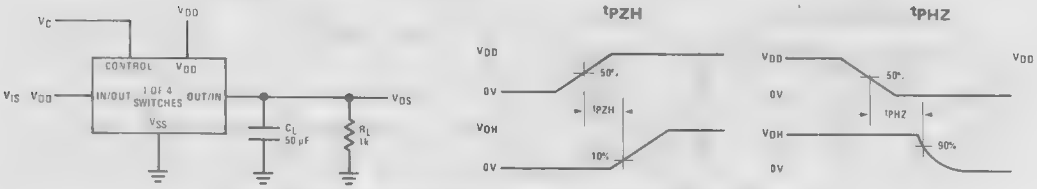


Figure 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

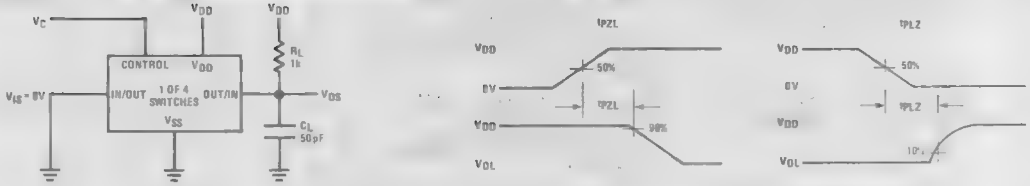
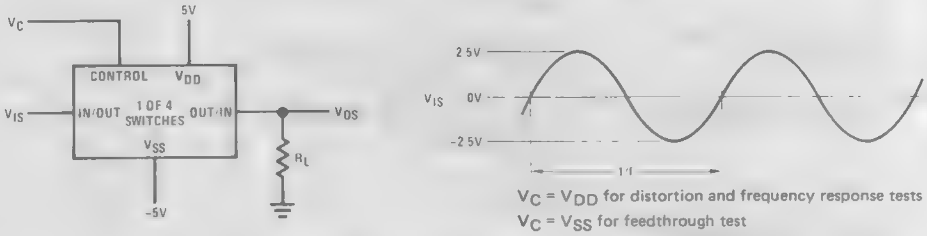


Figure 3. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$ for distortion and frequency response tests
$V_C = V_{SS}$ for feedthrough test

Figure 4. Sine Wave Distortion, Frequency Response and Feedthrough

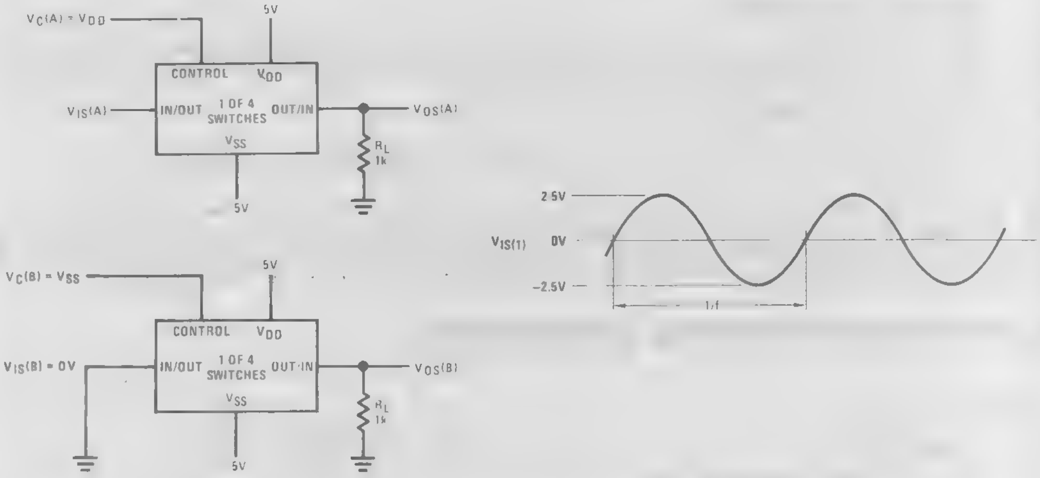


Figure 5. Crosstalk Between Any Two Switches

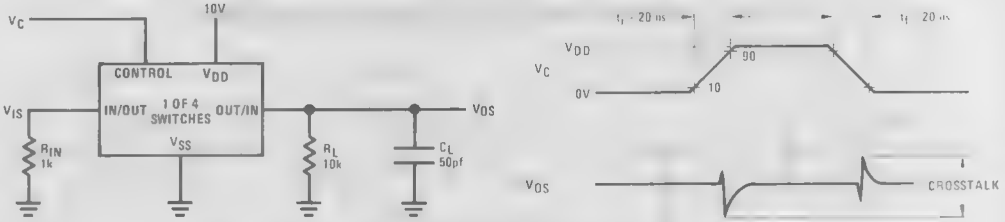


Figure 6. Crosstalk — Control to Input Signal Output

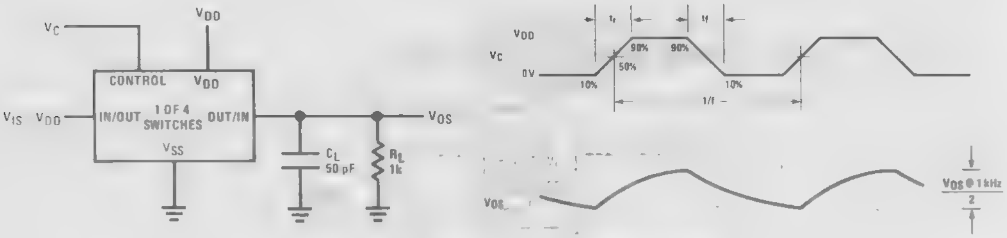


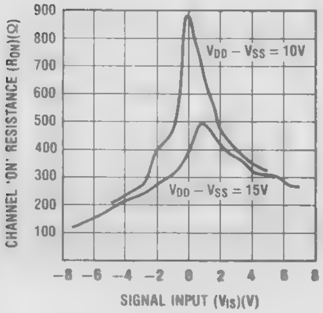
Figure 7. Maximum Control Input Frequency

Temperature Range	V_{DD}	V_{IS}	Switch Input I_{IS} (mA)			Switch Output $V_{OS(V)}$	
			T_{LOW}	25°C	T_{HIGH}	Min.	Max.
MILITARY	5	0	0.25	0.2	0.14		0.4
	5	5	−0.25	−0.2	−0.14	4.6	
	10	0	0.62	0.5	0.35		0.5
	10	10	−0.62	−0.5	−0.35	9.5	
	15	0	1.8	1.5	1.1		1.5
	15	15	−1.8	−1.5	−1.1	13.5	
COMMERCIAL	5	0	0.2	0.16	0.12		0.4
	5	5	−0.2	−0.16	−0.12	4.6	
	10	0	0.5	0.4	0.3		0.5
	10	10	−0.5	−0.4	−0.3	9.5	
	15	0	1.4	1.2	1.0		1.5
	15	15	−1.4	−1.2	−1.0	13.5	

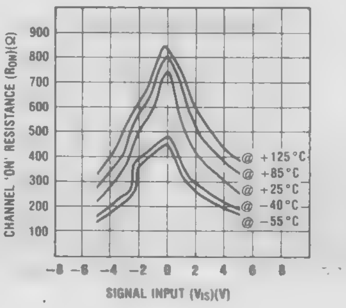
Figure 8. CD4016B Switch Test Conditions for V_{IHC}

Typical Performance Characteristics

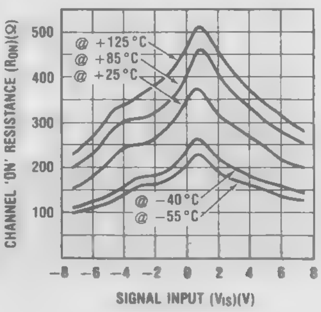
'ON' Resistance vs. Signal Voltage $T_A = 25°C$



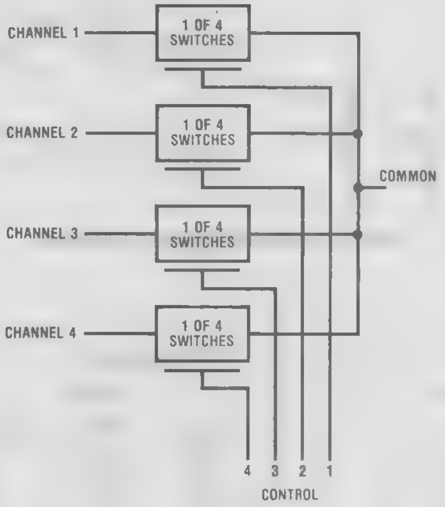
'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 10V$



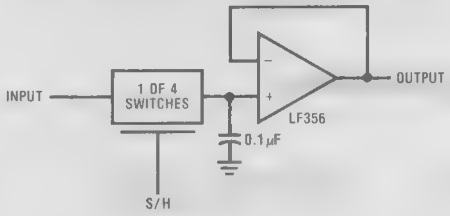
'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 15V$



Typical Applications



4 Input Multiplexer



Sample/Hold Amplifier

Special Considerations

The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R_{ON}" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages, ≤5V, the CD4016B's on resistance becomes non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either V_{DD} or V_{SS}; and that at 3V the voltages on the in/out pins should be at V_{DD} or V_{SS} for reliable operation.

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

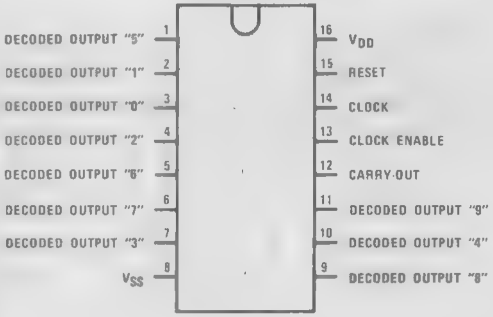
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz (typ.) with 10V V_{DD}
■ Low power	10μW (typ.)
■ Fully static operation	

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

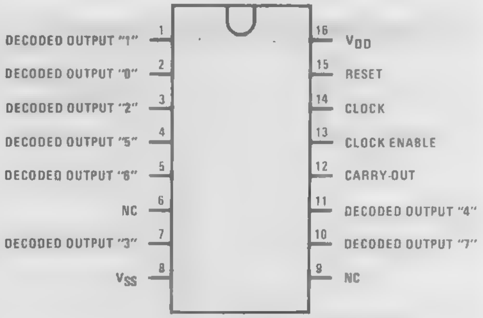
Connection Diagrams

CD4017B
Dual-In-Line and Flat Package



TOP VIEW

CD4022B
Dual-In-Line and Flat Package



TOP VIEW

V_{DD}	V_{DC}		to +15 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C	V_{IN} Input Voltage	0 to V_{DD} V_{DC}
P_D Package Dissipation	500 mW	T_A Operating Temperature Range	
T_L Lead Temperature (Soldering, 10 seconds)	300°C	CD4017BM, CD4022BM	−55°C to +125°C
		CD4017BC, CD4022BC	−40°C to +85°C

DC Electrical Characteristics CD4017BM, CD4022BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		1.5	−3.5		1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{5}	0.1		1.0	μA

DC Electrical Characteristics CD4017BC, CD4022BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) 4017BC, 4022BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1.0\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.2		−0.16	−0.36		−0.12		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.5		−0.4	−0.9		−0.3		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20\,ns$, unless otherwise specified

PARAMETER			CONDITIONS		MIN	TYP	MAX	UNITS
CLOCKED OPERATION								
t_{PHL}, t_{PLH}	Propagation Delay Time:							
		Carry Out Line	$V_{DD} = 5V$			415	800	ns
			$V_{DD} = 10V$			160	320	ns
			$V_{DD} = 15V$			130	250	ns
		Carry Out Line	$V_{DD} = 5V$	$C_L = 15\,pF$		240	480	ns
			$V_{DD} = 10V$			85	170	ns
			$V_{DD} = 15V$			70	140	ns
		Decode Out Lines	$V_{DD} = 5V$			500	1000	ns
			$V_{DD} = 10V$			200	400	ns
			$V_{DD} = 15V$			160	320	ns
t_{TLH}, t_{THL}	Transition Time Carry Out and Decode Out Lines							
		t_{TLH}	$V_{DD} = 5V$			200	360	ns
			$V_{DD} = 10V$			100	180	ns
			$V_{DD} = 15V$			80	130	ns
		t_{THL}	$V_{DD} = 5V$			100	200	ns
			$V_{DD} = 10V$			50	100	ns
			$V_{DD} = 15V$			40	80	ns
f_{CL}	Maximum Clock Frequency		$V_{DD} = 5V$	Measured with Respect to Carry Output Line	2.0	2		MHz
			$V_{DD} = 10V$		5.0	5		MHz
			$V_{DD} = 15V$		6.7	6		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width		$V_{DD} = 5V$			125	250	ns
			$V_{DD} = 10V$			45	90	ns
			$V_{DD} = 15V$			35	70	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time		$V_{DD} = 5V$				20	µs
			$V_{DD} = 10V$				15	µs
			$V_{DD} = 15V$				5	µs
t_{SU}	Minimum Clock Inhibit Data Set Up Time		$V_{DD} = 5V$			120	240	ns
			$V_{DD} = 10V$			40	80	ns
			$V_{DD} = 15V$			32	65	ns
C_{IN}	Average Input Capacitance					5	7.5	pF

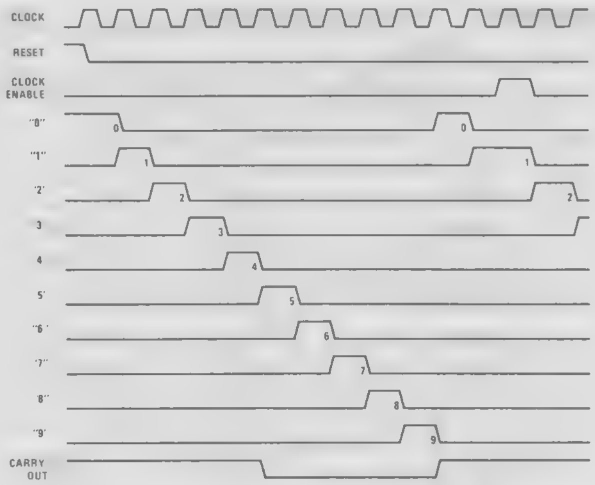
AC Electrical Characteristics (Cont'd.)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20$ ns, unless otherwise specified.

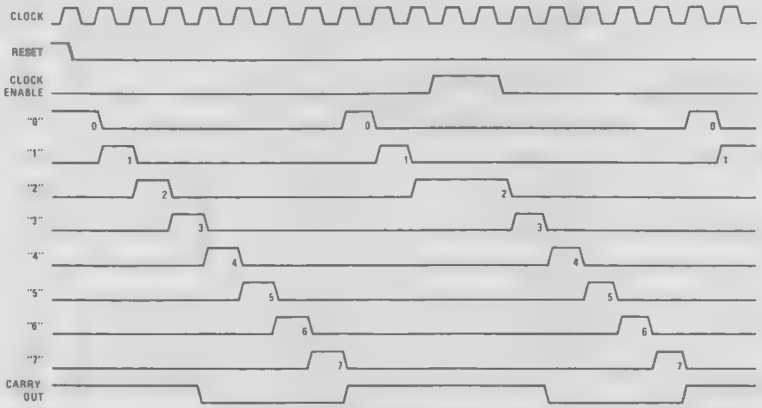
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET OPERATION						
t_{PHL}	Propagation Delay Time: Carry Out Line	$V_{DD} = 5V$		415	800	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	250	ns
	Carry Out Line	$V_{DD} = 5V$, C_L 15 pF		240	480	ns
		$V_{DD} = 10V$, C_L 15 pF		85	170	ns
		$V_{DD} = 15V$, C_L 15 pF		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{WH}	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
t_{REM}	Minimum Reset Removal Time	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns

Timing Diagrams

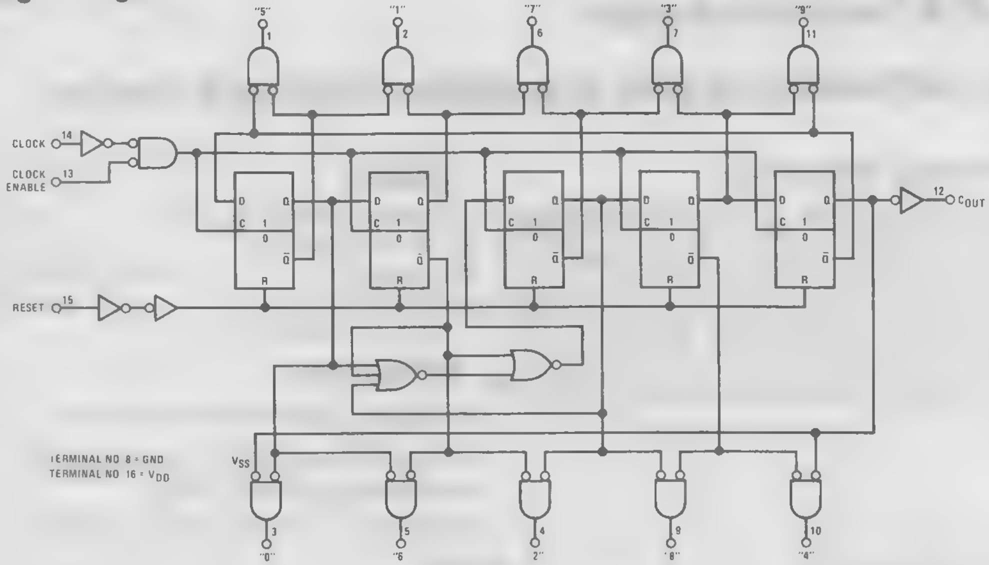
CD4017B



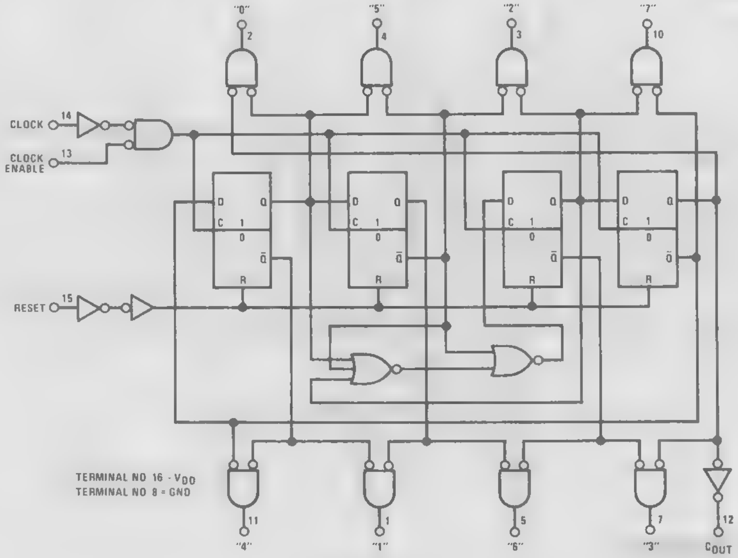
CD4022B



Logic Diagrams



CD4017B



CD4022B

General Description

The CD4018B consists of 5 Johnson counter stages. A buffered $\overline{Q}$ output from each stage, "CLOCK", "RESET", "DATA", "PRESET ENABLE", and 5 individual "JAM" inputs are provided. The counter is advanced one count at the positive clock signal transition. A high "RESET" signal clears the counters to an "ALL ZERO" condition. A high "PRESET ENABLE" signal allows information on the "JAM" inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

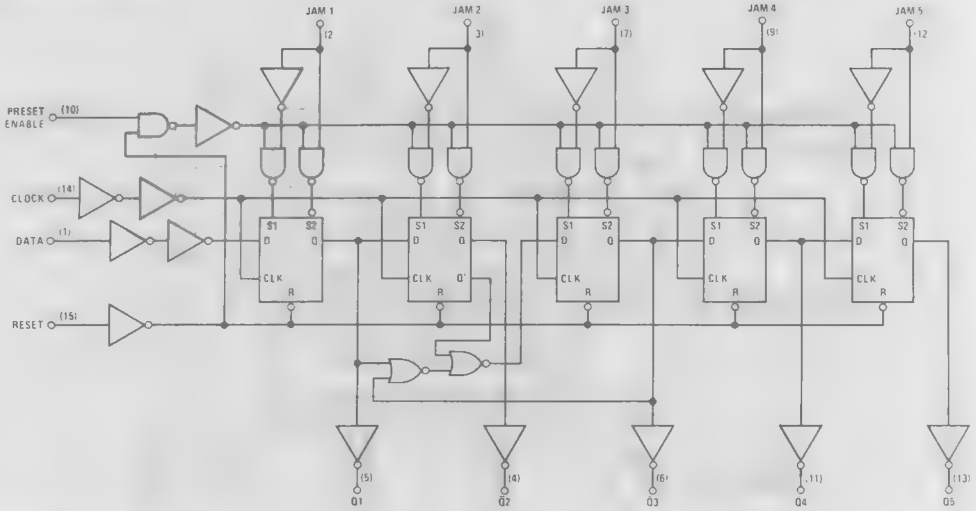
Features

Wide supply voltage range	3.0V to 15V
High noise immunity	0.45 V_{DD} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
Fully static operation	

Applications

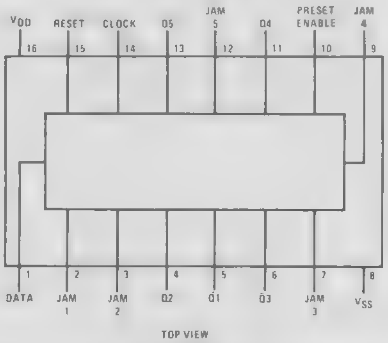
- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counter
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide by "N" counters/frequency synthesizers

Logic Diagram



Connection Diagram

Dual-In-Line and Flat Package



Absolute Maximum Ratings (Note 1)

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4018BM	−55°C to +125°C
CD4018BC	−40°C to +85°C

DC Electrical Characteristics CD4018BM (Note 2)

	PARAMETER	CONDITIONS	-55 C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4018BC (Note 2)

	PARAMETER	CONDITIONS	40 C		25°C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (Continued) CD4018BC

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics

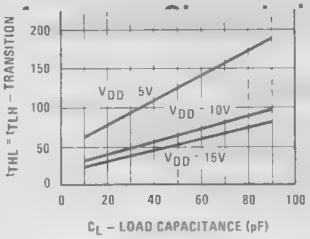
$T_A = 25^\circ C$, $C_L = 50$ pF, $R_L = 200k$, Input $t_r = t_f = 20$ ns, unless otherwise specified

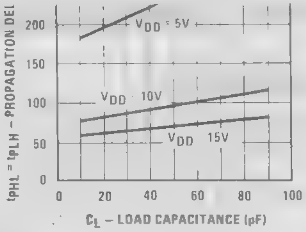
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	700	ns
		V_{DD} = 10V		95	250	ns
		V_{DD} = 15V		70	200	ns
t_{THL}, t_{TLH}	Transition Time $\overline{Q}$ Outputs	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		50	100	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	500	ns
		V_{DD} = 10V		50	200	ns
		V_{DD} = 15V		40	160	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_{SU}	Minimum Data Input Set-Up Time	V_{DD} = 5V		40	200	ns
		V_{DD} = 10V		20	100	ns
		V_{DD} = 15V		16	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	4		MHz
		V_{DD} = 10V	3	9		MHz
		V_{DD} = 15V	5	14		MHz
PRESET OR RESET OPERATION						
$t_{PLH(R)}$	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	750	ns
$t_{PHL(PR)}$		V_{DD} = 10V		95	250	ns
$t_{PLH(PR)}$		V_{DD} = 15V		70	200	ns
$t_{WH(R)}$ $t_{WH(PR)}$	Minimum Preset or Reset Pulse Width	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
t_{REM}	Minimum Preset or Reset Removal Time	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		63		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.



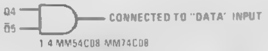


External Connections

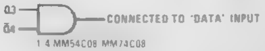
External Connections for Divide by
10, 9, 8, 7, 6, 5, 4, 3, 2, Operation

Divide By 10	$\overline{Q}5$	Connected Back To "DATA" Input
Divide By 8	$\overline{Q}4$	
Divide By 6	$\overline{Q}3$	
Divide By 4	$\overline{Q}2$	
Divide By 2	$\overline{Q}1$	

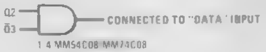
Divide By 9



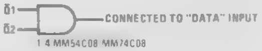
Divide By 7



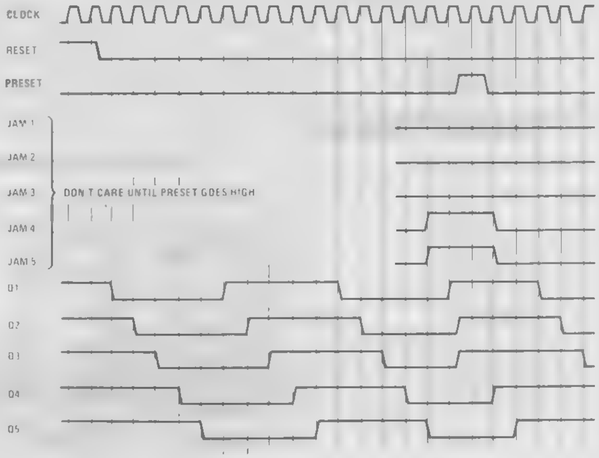
Divide By 5



Divide By 3



Timing Diagram



Note. "Data" input tied to $\overline{Q}5$ for decade counter configuration.

CD4019BM/CD4019BC Quad AND-OR Select Gate

General Description

The CD4019BM/CD4019BC is a complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N and P-channel enhancement mode transistors. These complementary MOS (CMOS) transistors provide the building blocks for the 4 "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

Features

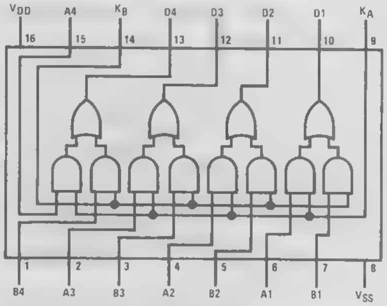
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/EXCLUSIVE-OR selection

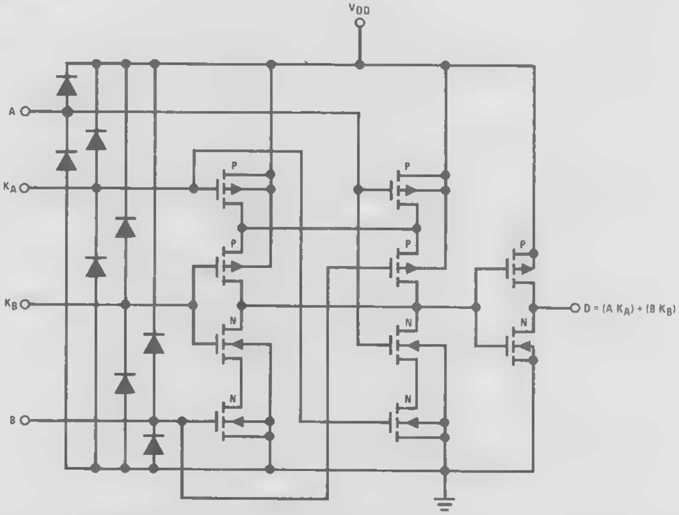
Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Schematic Diagram



Schematic diagram for 1 of 4 identical stages

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD} V
T_A Operating Temperature Range	
CD4019BM	−55°C to +125°C
CD4019BC	−40°C to +85°C

DC Electrical Characteristics CD4019BM (Note 2)

PARAMETER	CONDITIONS	-55 C		25 C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		0.25		0.03	0.25		7.5	μA
	V_{DD} = 10V		0.5		0.05	0.5		15	μA
	V_{DD} = 15V		1.0		0.07	1.0		30	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
	V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.5		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	10		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
	V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
	V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4019BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.03	1		7.5	µA
		V_{DD} = 10V		2		0.05	2		15	µA
		V_{DD} = 15V		4		0.07	4		30	µA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	1		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	10		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.4		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−1.0		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.0		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	µA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Input to Output	V_{DD} = 5V		100	300	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		45	100	ns
t_{THL}	High-to-Low Level Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Level Transition Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	All A and B Inputs		5	7.5	pF
		K_A and K_B Inputs, (Note 3)		10	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters
CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters
CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

General Description

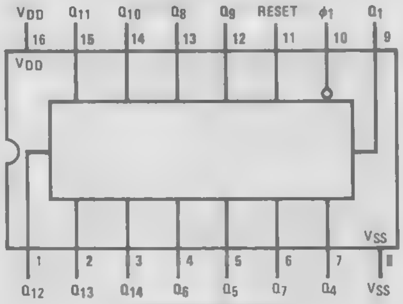
The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

Features

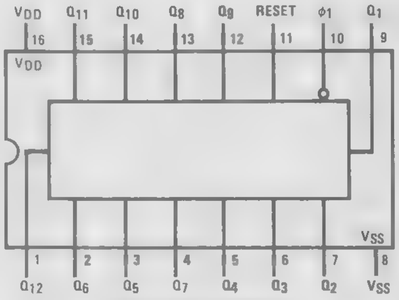
■ Wide supply voltage range	1.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz typ. at V_{DD} = 10 V
■ Schmitt trigger clock input	

Connection Diagrams

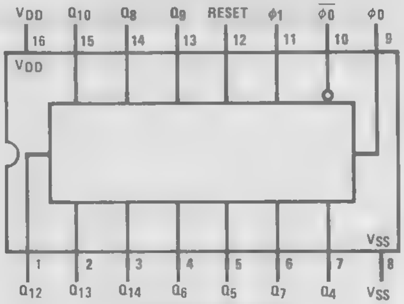
TOP VIEW



CD4020BM/CD4020BC



CD4040BM/CD4040BC



CD4060BM/CD4060BC

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5V to +18V
V_{IN}	Input Voltage	−0.5V to V_{DD} + 0.5V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD}	Supply Voltage	+3V to +15V
V_{IN}	Input Voltage	0V to V_{DD}
T_A	Operating Temperature Range	
	CD40XXBM	−55°C to +125°C
	CD40XXBC	−40°C to +85°C

DC Electrical Characteristics CD40XXBM (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BM/CD4060BC.

DC Electrical Characteristics 40XXBC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20			20		150	µA
		$V_{DD} = 10V$		40			40		300	µA
		$V_{DD} = 15V$		80			80		600	µA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.6	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		−1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	µA

AC Electrical Characteristics CD4020BM/CD4020BC, CD4040BM/CD4040BC

$T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, $t_r = t_f = 20ns$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	$V_{DD} = 5V$		250	550	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		125	335	ns
		$V_{DD} = 10V$		50	125	ns
		$V_{DD} = 15V$		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			no limit	ns
		$V_{DD} = 10V$			no limit	ns
		$V_{DD} = 15V$			no limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	4		MHz
		$V_{DD} = 10V$	4	10		MHz
		$V_{DD} = 15V$	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input (Note 1)		5	7.5	pF
C_{pd}	Power Dissipation Capacitance	(Note 2)		50		pF

Note 1: Capacitance guaranteed by periodic testing.

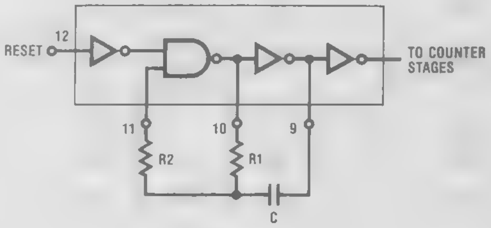
Note 2: Cpd determines the no-load etc.

t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			no limit	ns
		$V_{DD} = 10V$			no limit	ns
		$V_{DD} = 15V$			no limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input (Note 1)		5	7.5	pF
C_{pd}	Power Dissipation Capacitance	(Note 2)		50		pF

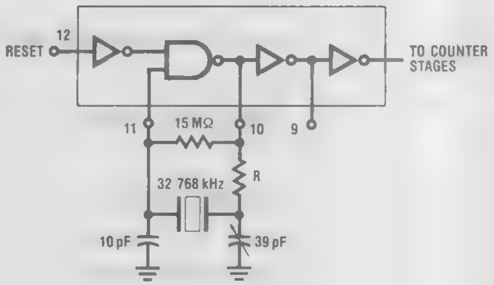
Note 1: Capacitance guaranteed by periodic testing.

Note 2: C_{pd} determines the no-load etc.

CD4060B Typical Oscillator Connections

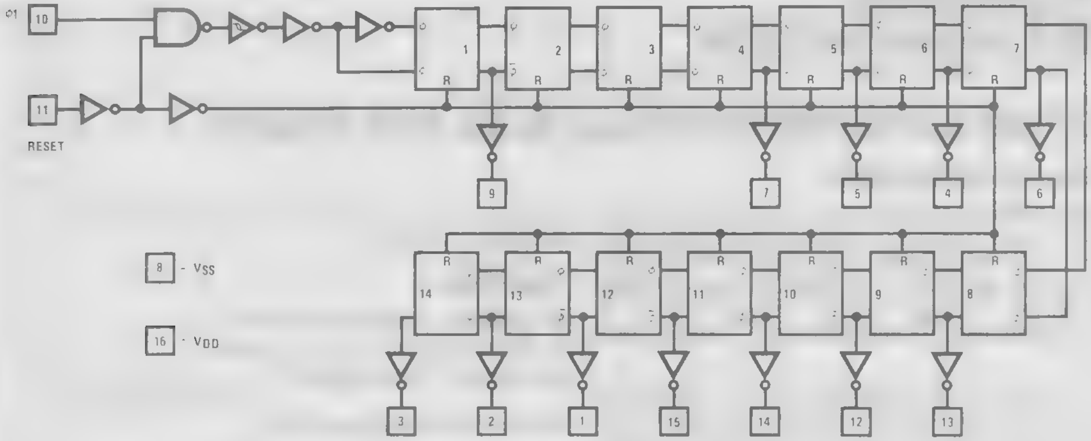


RC Oscillator

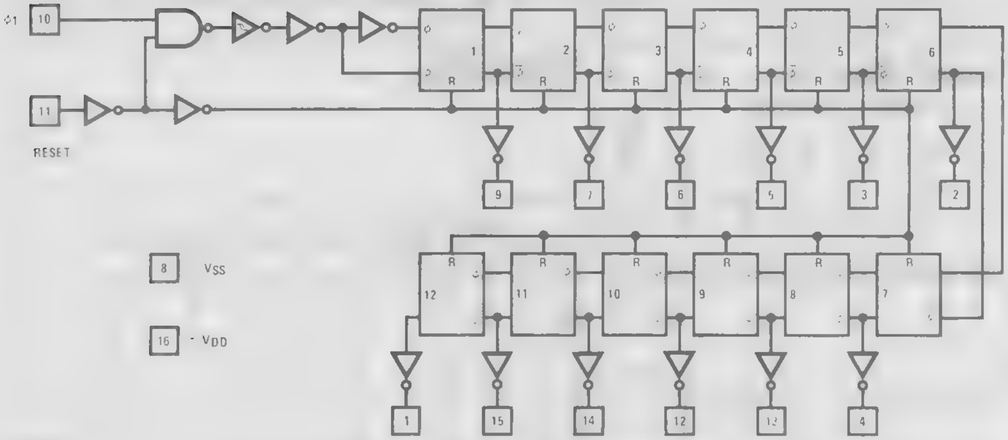


Crystal Oscillator

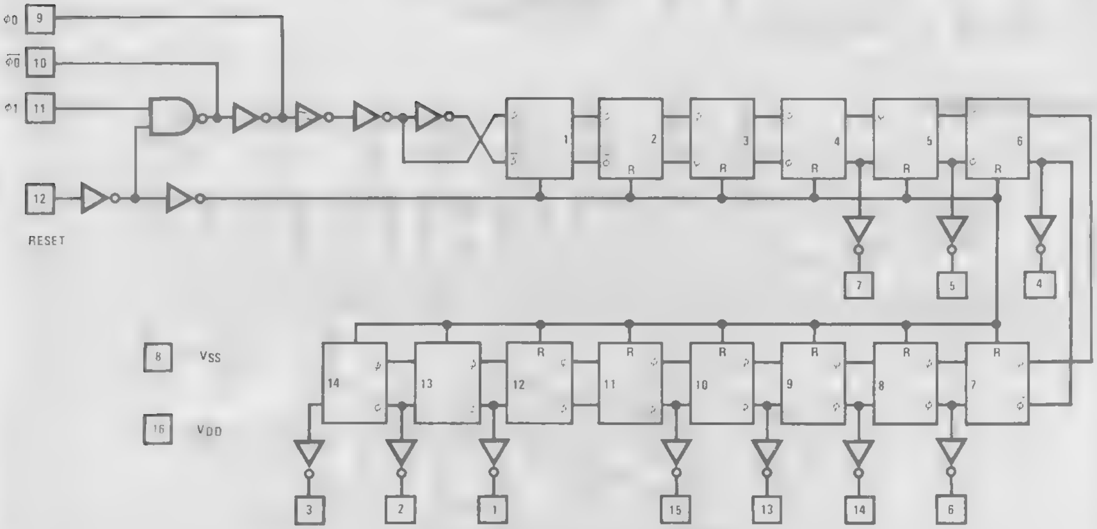
Schematic Diagrams



CD4020BM/CD4020BC Schematic Diagram



CD4040BM/CD4040BC Schematic Diagram



CD4060BM/CD4060BC Schematic Diagram

National Semiconductor

CD4021BM/CD4021BC 8-Stage Static Shift Register

General Description

The CD4021BM/CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q output are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

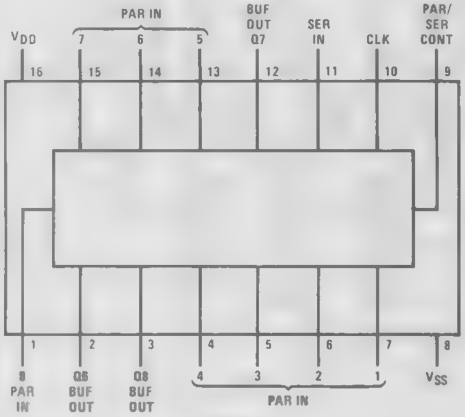
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package



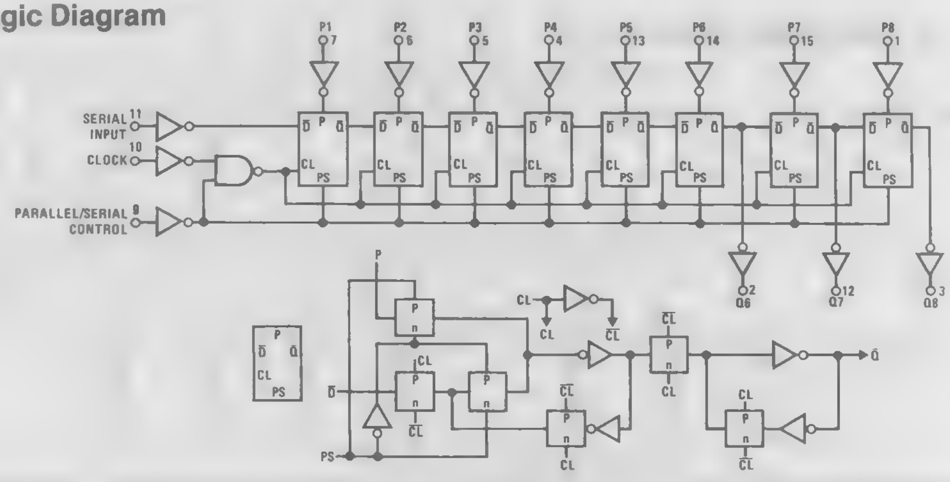
TOP VIEW

Truth Table

CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
↗	0	0	X	X	0	Q_{n-1}	
↗	1	0	X	X	1	Q_{n-1}	
↘	X	0	X	X	Q1	Q_n	No Change

*Level change
X = Don't care case

Logic Diagram



T_S Storage Temperature Range	−65°C to +150°C	
P_D Package Dissipation	500 mW	
T_L Lead Temperature (Soldering, 10 seconds)	300°C	

V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4021BM	−55°C to +125°C
CD4021BC	40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4021BM

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		5		0.1	5		150	μA
		$V_{DD}=10V$		10		0.2	10		300	μA
		$V_{DD}=15V$		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$, $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$, $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$, $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4021BC

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		20		0.1	20		150	μA
		$V_{DD}=10V$		40		0.2	40		300	μA
		$V_{DD}=15V$		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$, $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$, $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$, $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

t_{PLH}, t_{PHL}	Propagation Delay Time	$V_{DD}=5V$		240	330	ns
		$V_{DD}=10V$		100	175	ns
		$V_{DD}=15V$		70	140	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD}=5V$	2.5	3.5		MHz
		$V_{DD}=10V$	5	10		MHz
		$V_{DD}=15V$	8	16		MHz
t_W	Minimum Clock Pulse Width	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_rCL, t_fCL	Clock Rise and Fall Time (Note 3)	$V_{DD}=5V$			15	μs
		$V_{DD}=10V$			15	μs
		$V_{DD}=15V$			15	μs
t_s	Minimum Set-up Time					
	Serial Input	$V_{DD}=5V$		60	120	ns
	$t_H \geq 200$ ns	$V_{DD}=10V$		40	80	ns
	(Ref. to CL)	$V_{DD}=15V$		30	60	ns
	Parallel Inputs	$V_{DD}=5V$		25	50	ns
	$t_H \geq 200$ ns	$V_{DD}=10V$		15	30	ns
	(Ref. to P/S)	$V_{DD}=15V$		10	20	ns
t_H	Minimum Hold Time	$V_{DD}=5V$			0	ns
	Serial In, Parallel In, $t_s \geq 400$ ns	$V_{DD}=10V$			10	ns
	Parallel/Serial Control	$V_{DD}=15V$			15	ns
t_{WH}	Minimum P/S Pulse Width	$V_{DD}=5V$		150	250	ns
		$V_{DD}=10V$		75	125	ns
		$V_{DD}=15V$		50	100	ns
t_{REM}	Minimum P/S Removal Time (Ref. to CL)	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)			100		pF

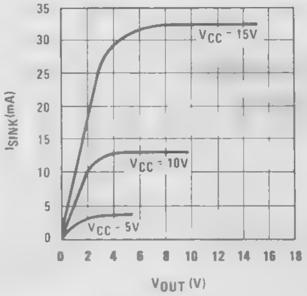
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

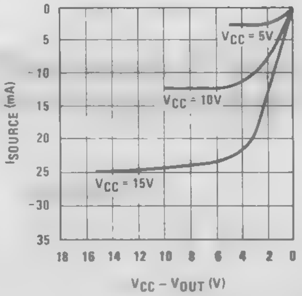
Note 2: $V_{SS}=0V$ unless otherwise specified.

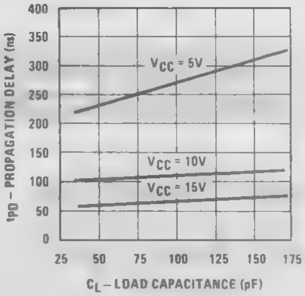
Note 3: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Typical Performance Characteristics







National Semiconductor

CD4023M/CD4023C Triple 3-Input NAND Gate
CD4025M/CD4025C Triple 3-Input NOR Gate

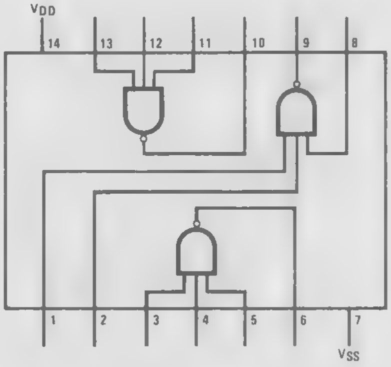
General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

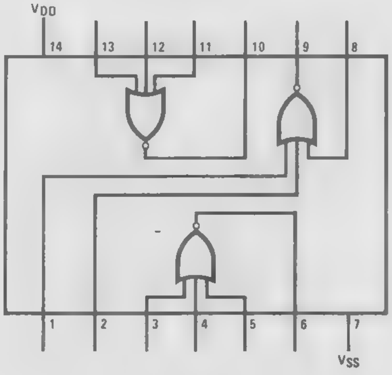
Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ 5-10 V parametric ratings	
■ Low Power	

Connection Diagrams



CD4023M/CD4023C
TOP VIEW



CD4025M/CD4025C
TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$V_{SS} -$ to $V_{DD} + 0.3\,V$
Operating Temperature Range	−55°C to +125°C
CD4023M, CD4025M	−55°C to +125°C
CD4023C, CD4025C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0\,V$ to $V_{SS} + 15\,V$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics — CD4023M, CD4025M

Parameter		Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Device Current	$V_{DD} = 5.0\,V$		0.05		0.001	0.05		3.0	μA
		$V_{DD} = 10\,V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0\,V$		0.25		0.005	0.25		15	μW
		$V_{DD} = 10\,V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0\,V$, $V_I = V_{DD}$, $I_O = 0\,A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\,V$, $V_I = V_{DD}$, $I_O = 0\,A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0\,V$, $V_I = V_{SS}$, $I_O = 0\,A$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10\,V$, $V_I = V_{SS}$, $I_O = 0\,A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0\,V$, $V_O = 3.6V$, $I_O = 0\,A$	1.5		1.5	2.25		1.4		V
		$V_{DD} = 10\,V$, $V_O = 7.2V$, $I_O = 0\,A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0\,V$, $V_O = 0.95\,V$, $I_O = 0\,A$	1.4		1.5	2.25		1.5		V
		$V_{DD} = 10\,V$, $V_O = 2.9\,V$, $I_O = 0\,A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4025)	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$, $V_I = V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD} = 10\,V$, $V_O = 0.5\,V$, $V_I = V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4025)	$V_{DD} = 5.0\,V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.62		−0.5	−2.0		−0.35		mA
		$V_{DD} = 10\,V$, $V_O = 9.5\,V$, $V_I = V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN	Output Drive Current N-Channel (4023)	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$, $V_I = V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD} = 10\,V$, $V_O = 0.5\,V$, $V_I = V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4023)	$V_{DD} = 5.0\,V$, $V_O = 2.5\,V$, $V_I = V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
		$V_{DD} = 10\,V$, $V_O = 9.5\,V$, $V_I = V_{SS}$	−0.75		−0.6	−1.2		−0.4		mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4023C, CD4025C

Parameter	Conditions	Limits							Units
		−40°C		25°C			85°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent Device Current	$V_{DD} = 5.0$ V		0.5		0.005	0.5		15	μA
	$V_{DD} = 10$ V		5.0		0.005	5.0		30	μA
P_D Quiescent Device Dissipation/Package	$V_{DD} = 5.0$ V		2.5		0.025	2.5		75	μW
	$V_{DD} = 10$ V		50		0.05	50		300	μW
V_{OL} Output Voltage Low Level	$V_{DD} = 5.0$ V, $V_I = V_{DD}$, $_O = 0$ A		0.01		0	0.01		0.05	V
	$V_{DD} = 10$ V, $V_I = V_{DD}$, $I_O = 0$ A		0.01		0	0.01		0.05	V
V_{OH} Output Voltage High Level	$V_{DD} = 5.0$ V, $V_I = V_{SS}$, $I_O = 0$ A	4.99		4.99	5.0		4.95		V
	$V_{DD} = 10$ V, $V_I = V_{SS}$, $I_O = 0$ A	9.99		9.99	10		9.95		V
I_I Input Current					10				pA
V_{NL} Noise Immunity (All Inputs)	$V_{DD} = 5.0$ V, $V_O = 3.6$ V, $I_O = 0$ A	1.5		1.5	2.25		1.4		V
	$V_{DD} = 10$ V, $V_O = 7.2$ V, $I_O = 0$ A	3.0		3.0	4.5		2.9		V
V_{NH} Noise Immunity (All Inputs)	$V_{DD} = 5.0$ V, $V_o = 0.95$ V, $I_O = 0$ A	1.4		1.5	2.25		1.5		V
	$V_{DD} = 10$ V, $V_O = 2.9$ V, $I_O = 0$ A	2.9		3.0	4.5		3.0		V
I_DN Output Drive Current N-Channel (4025)	$V_{DD} = 5.0$ V, $V_O = 0.4$ V, $V_I = V_{DD}$	0.35		0.3	1.0		0.24		mA
	$V_{DD} = 10$ V, $V_O = 0.5$ V, $V_I = V_{DD}$	0.72		0.6	2.5		0.48		mA
I_DP Output Drive Current P-Channel (4025)	$V_{DD} = 5.0$ V, $V_O = 2.5$ V, $V_I = V_{SS}$	−0.35		−0.3	−2.0		−0.24		mA
	$V_{DD} = 10$ V, $V_O = 9.5$ V, $V_I = V_{SS}$	−0.3		−0.25	−1.0		−0.2		mA
I_DN Output Drive Current N-Channel (4023)	$V_{DD} = 5.0$ V, $V_O = 0.4$ V, $V_I = V_{DD}$	0.145		0.12	0.5		0.095		mA
	$V_{DD} = 10$ V, $V_O = 0.5$ V, $V_I = V_{DD}$	0.3		0.25	0.6		0.2		mA
$I_D P$ Output Drive Current P-Channel (4023)	$V_{DD} = 5.0$ V, $V_O = 2.5$ V, $V_I = V_{SS}$	−0.145		−0.12	−0.5		−0.095		mA
	$V_{DD} = 10$ V, $V_O = 9.5$ V, $V_I = V_{SS}$	−0.35		−0.3	−1.2		−0.24		mA
I_I Input Current					10				pA

	CD4025M					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		35 25	40 70	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		65 35	125 70	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		65 35	175 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
	CD4025C					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		35 25	80 55	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		35 25	120 65	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		65 35	200 115	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		65 35	300 125	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics

$T_A=25°C$, $C_L=15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD}=0.3\%/°C$

Parameter		Conditions	Min.	Typ.	Max.	Units
	CD4023M					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		75 40	100 60	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
	CD4023C					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD}=5.0V$ $V_{DD}=10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD}=5.0V$ $V_{DD}=10V$		75 40	125 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

National
Semiconductor

CD4023BM/CD4023BC Buffered Triple 3-Input NAND Gate
CD4025BM/CD4025BC Buffered Triple 3-Input NOR Gate

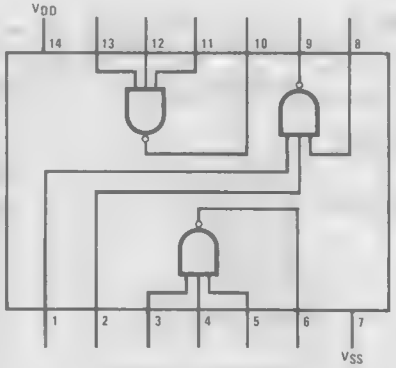
General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

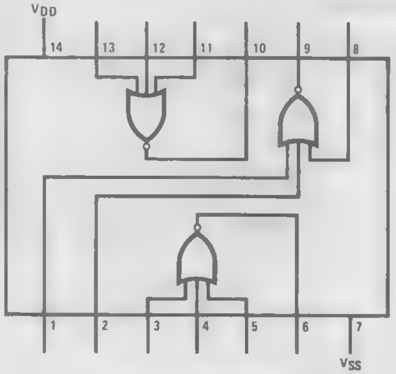
Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5 V–10 V–15 V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15 V over full temperature range

Connection Diagrams



CD4023BM/CD4023BM
TOP VIEW



CD4025BM/CD4025BC
TOP VIEW

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\,V_{DC}$ to $+18\,V_{DC}$
V_{IN}	Input Voltage	$-0.5\,V_{DC}$ to $V_{DD} + 0.5\,V_{DC}$
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

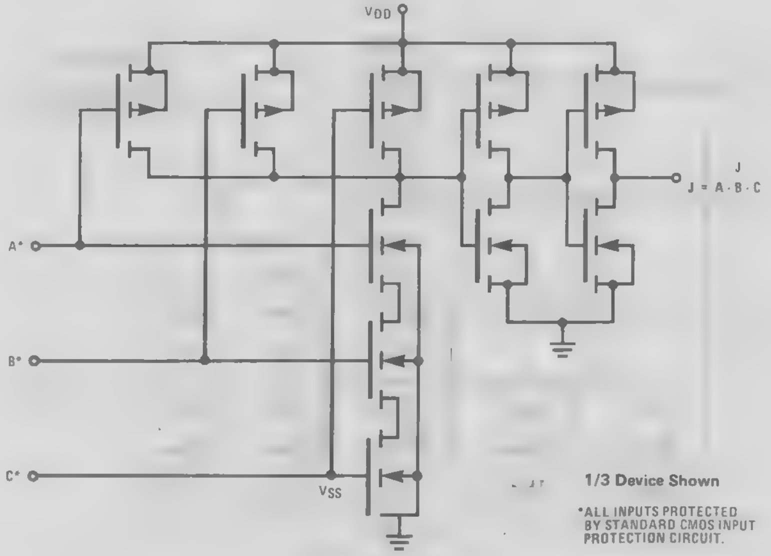
Recommended Operating Conditions

V_{DD}	DC Supply Voltage	$+5\,V_{DC}$ to $+15\,V_{DC}$
V_{IN}	Input Voltage	$0\,V_{DC}$ to $V_{DD}\,V_{DC}$
T_A	Operating Temperature Range	
	CD4023BM, CD4025BM	−55°C to +125°C
	CD4023BC, CD4025BC	−40°C to +85°C

DC Electrical Characteristics - CD4023BM, CD4025BM (Note 2)

	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5\,V$		0.25		0.004	0.25		7.5	µA
		$V_{DD} = 10\,V$		0.5		0.005	0.5		15	µA
		$V_{DD} = 15\,V$		1.0		0.006	1.0		30	µA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\,V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\,V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15\,V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\,V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10\,V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15\,V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\,V,\ V_O = 4.5\,V$ $\|I_O\| < 1\,\mu A$		1.5		2	1.5		1.5	V
		$V_{DD} = 10\,V,\ V_O = 9.0\,V$ $\|I_O\| < 1\,\mu A$		3.0		4	3.0		3.0	V
		$V_{DD} = 15\,V,\ V_O = 13.5\,V$ $\|I_O\| < 1\,\mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5\,V,\ V_O = 0.5\,V$ $\|I_O\| < 1\,\mu A$	3.5		3.5	3		3.5		V
		$V_{DD} = 10\,V,\ V_O = 1.0\,V$ $\|I_O\| < 1\,\mu A$	7.0		7.0	6		7.0		V
		$V_{DD} = 15\,V,\ V_O = 1.5\,V$ $\|I_O\| < 1\,\mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5\,V,\ V_O = 0.4\,V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\,V,\ V_O = 0.5\,V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15\,V,\ V_O = 1.5\,V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5\,V,\ V_O = 4.6\,V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10\,V,\ V_O = 9.5\,V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15\,V,\ V_O = 13.5\,V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\,V,\ V_{IN} = 0\,V$		−0.10		-10^{-5}	−0.10		−1.0	µA
		$V_{DD} = 15\,V,\ V_{IN} = 15\,V$		0.10		10^{-5}	0.10		1.0	µA

schematic diagram


VDD
A*
B*
C*
VSS
J
J = A · B · C
1/3 Device Shown
*ALL INPUTS PROTECTED BY STANDARD CMOS INPUT PROTECTION CIRCUIT.

CD4023BC/CD4023BM

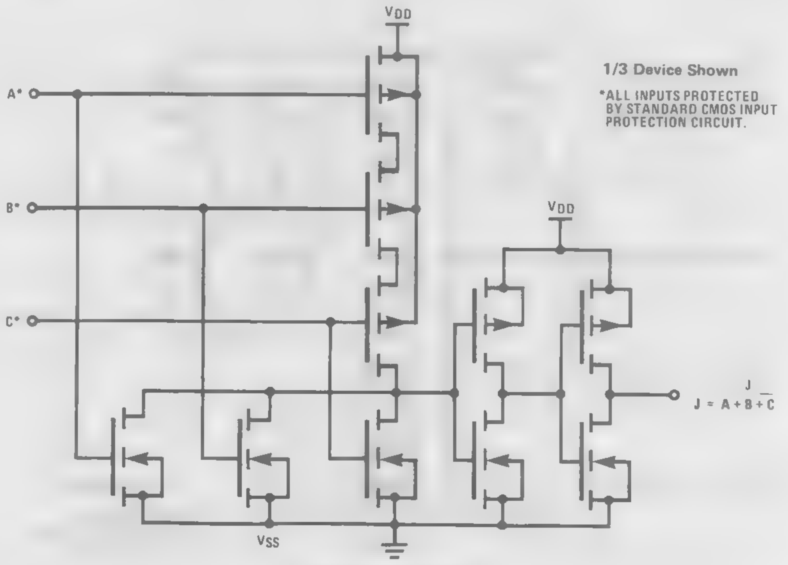
DC Electrical Characteristics CD4023BC, CD4025BC (Note 2)

	PARAMETER	CONDITIONS	−40° C		+25° C			+85° C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V				0.004			7.5	μA
		V_{DD} = 10 V				0.005			15	μA
		V_{DD} = 15 V				0.006			30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 4.5 V; $\lvert I_O \rvert < 1\,\mu A$		1.5		2	1.5		1.5	V
		V_{DD} = 10 V, V_O = 9.0 V		3.0		4	3.0		3.0	V
		V_{DD} = 15 V, V_O = 13.5 V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V; $\lvert I_O \rvert < 1\,\mu A$	3.5		3.5	3		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V	7.0		7.0	6		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

schematic diagram



1/3 Device Shown

*ALL INPUTS PROTECTED BY STANDARD CMOS INPUT PROTECTION CIRCUIT.

CD4025BM/CD4025BC

t_{PHL}	Propagation Delay, High to Low Level	V_{DD} = 5 V		130	250		130	250	ns
		V_{DD} = 10 V		60	100		60	100	ns
		V_{DD} = 15 V		40	70		40	70	ns
t_{PLH}	Propagation Delay, Low to High Level	V_{DD} = 5 V		110	250		120	250	ns
		V_{DD} = 10 V		50	100		60	100	ns
		V_{DD} = 15 V		35	70		40	70	ns
t_{THL} t_{TLH}	Transition Time	V_{DD} = 5 V		90	200		90	200	ns
		V_{DD} = 10 V		50	100		50	100	ns
		V_{DD} = 15 V		40	80		40	80	ns
C_{IN}	Average Input Capacitance (See Note 3)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (See Note 4)	Any Gate		17			17		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

National Semiconductor

CD4024BM/CD4024BC 7-Stage Ripple Carry Binary Counter

General Description

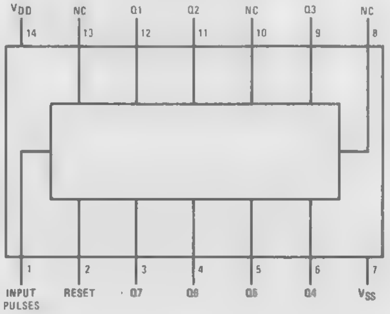
The CD4024BM/CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The couter is reset to its logical "0" stage by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ High speed	12 MHz (typ.) input pulse rate $V_{DD} - V_{SS} = 10$ V
■ Fully static operation	

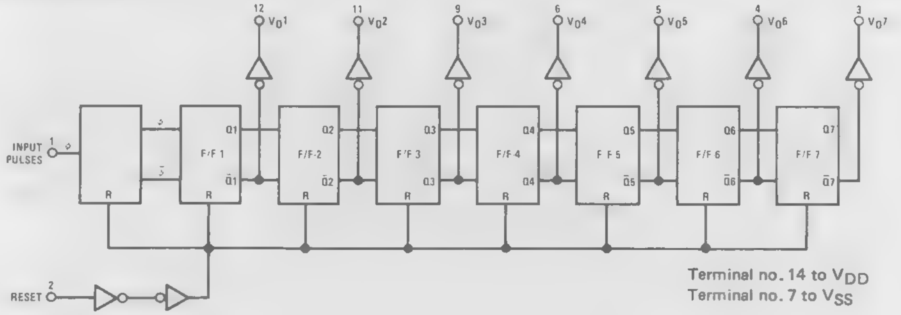
Connection Diagram

Dual-In-Line Package



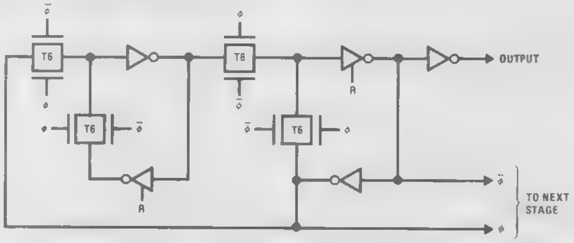
TOP VIEW

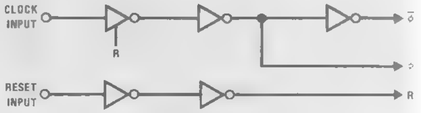
Logic Diagram



Terminal no. 14 to V_{DD}
Terminal no. 7 to V_{SS}

Schematic Diagram





Input Logic

Flip-flop logic (1 of 7 identical stages).

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4024BM	−55°C to +125°C
CD4024BC	−40°C to +85°C

DC Electrical Characteristics CD4024BM (Note 2)

PARAMETER		CONDITIONS	55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		0.7	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{5}	0.10		1.0	μA

DC Electrical Characteristics CD4024BC (Note 2)

PARAMETER		CONDITIONS	−40 C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.3	20		150	μA
		V_{DD} = 10V		40		0.5	40		300	μA
		V_{DD} = 15V		60		0.7	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4024BC (Note 2)

	PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	-0.52		-0.44	0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.3		1.1	2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	3.6		3.0	-8.8		2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		0.30		10^{-5}	-0.30		1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, t_r and $t_f = 20\,ns$ unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time (Note 3)	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width	$V_{DD} = 5V$		75	200	ns
		$V_{DD} = 10V$		40	110	ns
		$V_{DD} = 15V$		35	90	ns
t_{RCL}, t_{FCL}	Input Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			10	μs
		$V_{DD} = 15V$			8	μs
f_{CL}	Maximum Input Pulse Frequency	$V_{DD} = 5V$	1.5	5		MHz
		$V_{DD} = 10V$	4	12		MHz
		$V_{DD} = 15V$	5	15		MHz
t_{PHL}	Reset Propagation Delay Time	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
t_{WH}	Reset Minimum Pulse Width	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
C_{IN}	Input Capacitance (Note 4)	Any Input		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: To Q1 output.

Note 4: Capacitance is guaranteed by periodic testing.

CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

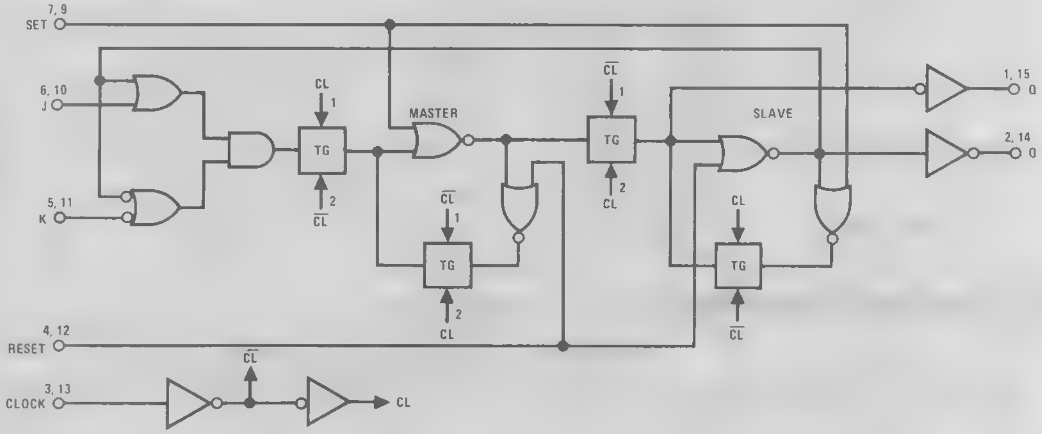
These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and "$\overline{Q}$" outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

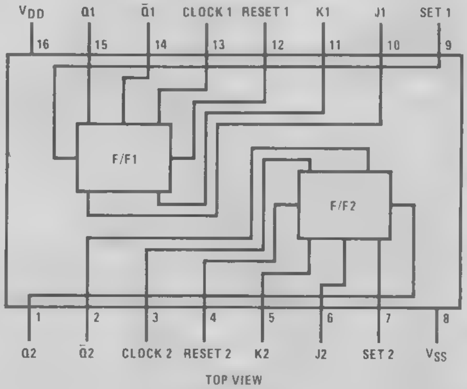
■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Low power	50 nW (typ.)
■ Medium speed operation	12 MHz (typ.) with 10 V supply

Schematic Diagram



Connection Diagram

Dual-In-Line and Flat Package



Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	–0.5 to +18 V_{DC}
V_{IN} Input Voltage	–0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	–65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4027BM	–55°C to +125°C
CD4027BC	–40°C to +85°C

DC Electrical Characteristics CD4027BM (Note 2)

PARAMETER		CONDITIONS	-55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1			1		30	μA
		V_{DD} = 10V		2			2		60	μA
		V_{DD} = 15V		4			4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	–0.64		–0.51	–0.88		–0.36		mA
		V_{DD} = 10V, V_O = 9.5V	–1.6		–1.3	–2.25		–0.9		mA
		V_{DD} = 15V, V_O = 13.5V	–4.2		–3.4	–8.8		–2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		–0.1		-10^{-5}	–0.1		–1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics (Cont'd.) CD4027BC (Note 2)

PARAMETER		CONDITIONS	-40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4			4		30	μA
		V_{DD} = 10V		8			8		60	μA
		V_{DD} = 15V		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics CD4027BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $t_{rCL} = t_{fCL} = 20\,ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Q or $\overline{Q}$	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Set to $\overline{Q}$ or Reset to Q	$V_{DD} = 5V$		170	340	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Set to Q or Reset to $\overline{Q}$	$V_{DD} = 5V$		110	220	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_s	Minimum Data Set-Up Time	$V_{DD} = 5V$		135	270	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Frequency (Toggle Mode)	$V_{DD} = 5V$	2.5	5		MHz
		$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		MHz
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	10			μs
		$V_{DD} = 15V$	5			μs
t_W	Minimum Clock Pulse Width ($t_{WH} = t_{WL}$)	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
t_{WH}	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		80	160	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Per Flip-Flop (Note 3)		35		pF

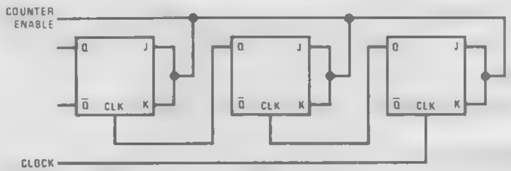
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

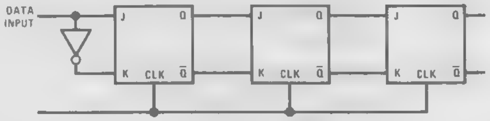
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

Typical Applications

Ripple Binary Counters



Shift Registers



Truth Table

$^{\bullet}t_{n-1}$ INPUTS						$^{\blacklozenge}t_n$ OUTPUTS		
CL$^{\blacktriangle}$	J	K	S	R	Q	Q	Q̄	
↑	I	X	O	O	O	I	O	
↑	X	O	O	O	I	I	O	
↑	O	X	O	O	O	O	I	
↑	X	I	O	O	I	O	I	
↓	X	X	O	O	X			(No change)
X	X	X	I	O	X	I	O	
X	X	X	O	I	X	O	I	
X	X	X	I	I	X	I	I	

Where: I = High Level
O = Low Level
▲ = Level Change
X = Don't Care
● = t_{n-1} refers to the time interval prior to the positive clock pulse transition
◆ = t_n refers to the time intervals after the positive clock pulse transition

CD4028BM/CD4028BC BCD-to-Decimal Decoder

General Description

The CD4028BM/CD4028BC is a BCD-to-decimal or binary-to-octal decoder consisting of 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the 4 inputs, A, B, C, and D, results in a high level at the selected 1-of-10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B, and C is decoded in octal at outputs 0–7. A high level signal at the D input inhibits octal decoding and causes outputs 0–7 to go low.

All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS}.

Features

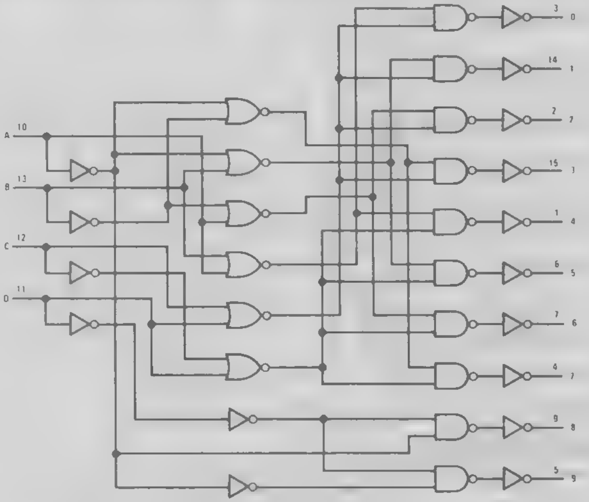
■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

- Low power
- Glitch free outputs
- "Positive logic" on inputs and outputs

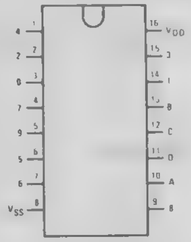
Applications

- Code conversion
- Address decoding
- Indicator-tube decoder

Logic and Connection Diagrams



Dual-In-Line and Flat Package



TOP VIEW

Truth Table

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	BCD States
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	Extraordinary States
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

1 = High level
0 = Low level

Absolute Maximum Ratings (Note 1)

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4028BM	-55°C to +125°C
CD4028BC	-40°C to +85°C

DC Electrical Characteristics CD4028BC (Note 2)

	PARAMETER	CONDITIONS	55 C		25 C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V, V_O = 4.6V	−0.25		0.2	−0.4		0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	1.0		0.35		mA
		V_{DD} = 15V, V_O = 13.5V	1.8		1.5	3.0		1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	0.1		1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{5}	0.1		1.0	μA

DC Electrical Characteristics CD4028BC (Note 2)

	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4028BC (Note 2)

PARAMETER		CONDITIONS	40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$I_O < 1\,\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.2		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−0.2		−0.16	−0.32		−0.12		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.5		−0.4	−0.8		−0.3		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2	−2.4		−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	−0.3			−0.3			−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$	0.3			0.3			1.0	μA

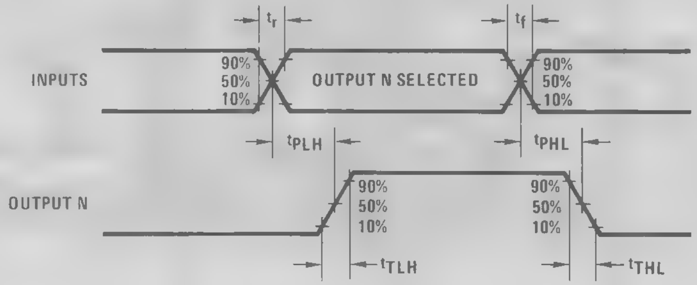
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay	$V_{CC} = 5V$		240	480	ns
		$V_{CC} = 10V$		100	200	ns
		$V_{CC} = 15V$		70	140	ns
t_{THL} or t_{TLH}	Transition Time	$V_{CC} = 5V$		175	350	ns
		$V_{CC} = 10V$		75	150	ns
		$V_{CC} = 15V$		60	110	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Switching Time Waveforms



National Semiconductor

CD4029BM/CD4029BC Presettable Binary/Decade Up/Down Counter

General Description

The CD4029BM/CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1," the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

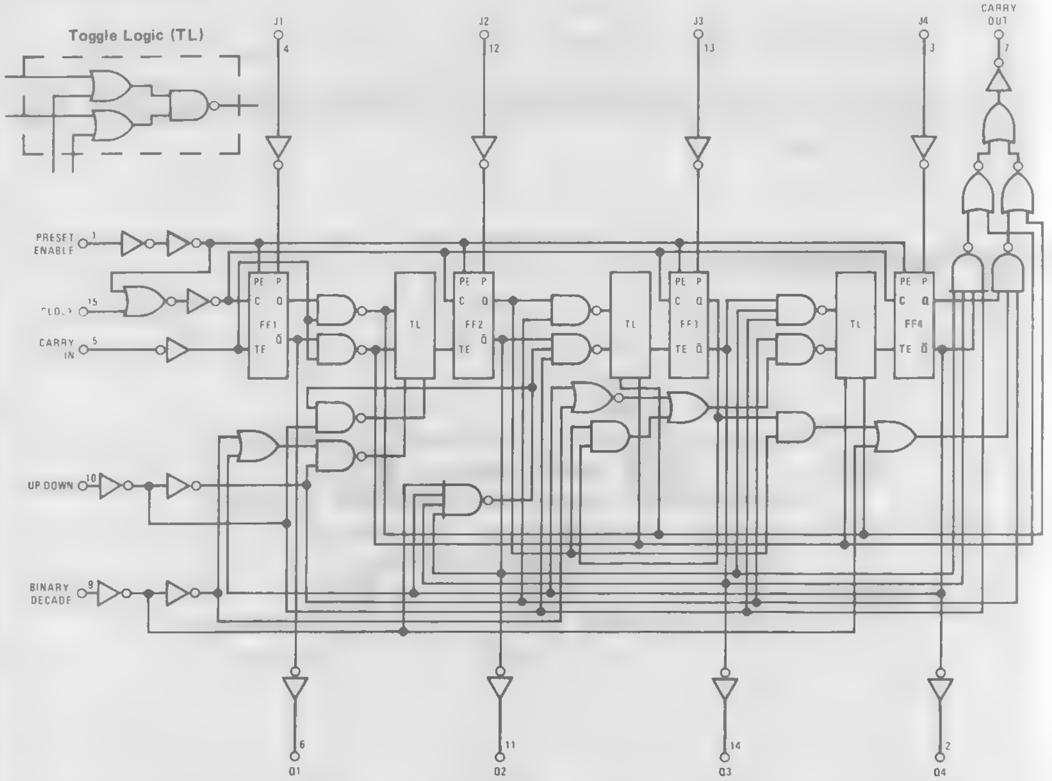
A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0." Advancement is inhibited when either or both of these two inputs is at logical "1." The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Parallel jam inputs	
■ Binary or BCD decade up/down counting	

Logic Diagram



V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4029BM	−55°C to +125°C
CD4029BC	−40°C to +85°C

DC Electrical Characteristics CD4029BM (Note 2)

PARAMETER		CONDITIONS	55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5	5	150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4029BC (Note 2)

PARAMETER		CONDITIONS	40 C		25°C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4029BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5 or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_{rCL} = t_{fCL} = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Outputs	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		70	140	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V		320	640	ns
		V_{DD} = 10V		135	270	ns
		V_{DD} = 15V		110	220	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V, C_L = 15 pF		285	570	ns
		V_{DD} = 10V, C_L = 15 pF		120	240	ns
		V_{DD} = 15V, C_L = 15 pF		95	190	ns
t_{THL} or t_{TLH}	Transition Time/Q or Carry Output	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH} or t_{WL}	Minimum Clock Pulse Width	V_{DD} = 5V		160	320	ns
		V_{DD} = 10V		70	135	ns
		V_{DD} = 15V		55	110	ns
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		180	360	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	3.1		MHz
		V_{DD} = 10V	3.7	7.4		MHz
		V_{DD} = 15V	4.5	9		MHz
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		65		pF
PRESET ENABLE OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Output	V_{DD} = 5V		285	570	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		95	195	ns

AC Electrical Characteristics (Cont'd.) $T_A = 25^\circ C$, $C_L = 50$ pF, $t_{rCL} = t_{fCL} = 20$ ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
PRESET ENABLE OPERATION (con't)						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$		400	800	ns
		$V_{DD} = 10V$		165	330	ns
		$V_{DD} = 15V$		135	260	ns
t_{WH}	Minimum Preset Enable Pulse Width	$V_{DD} = 5V$		80	160	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{REM}	Minimum Preset Enable Removal Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		60	120	ns
		$V_{DD} = 15V$		50	100	ns
CARRY INPUT OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$		265	530	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$, $C_L = 15$ pF		200	400	ns
		$V_{DD} = 10V$, $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$, $C_L = 15$ pF		70	140	ns

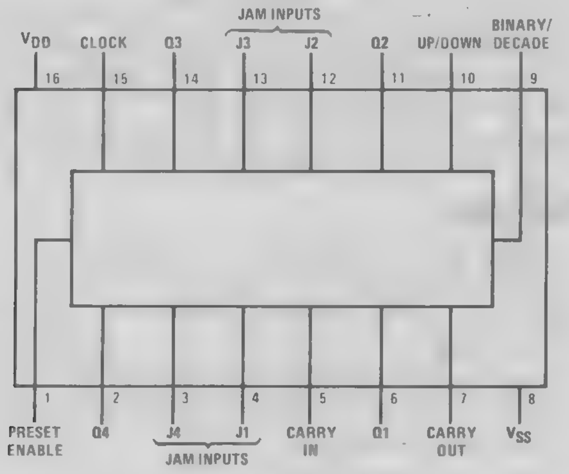
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Connection Diagram

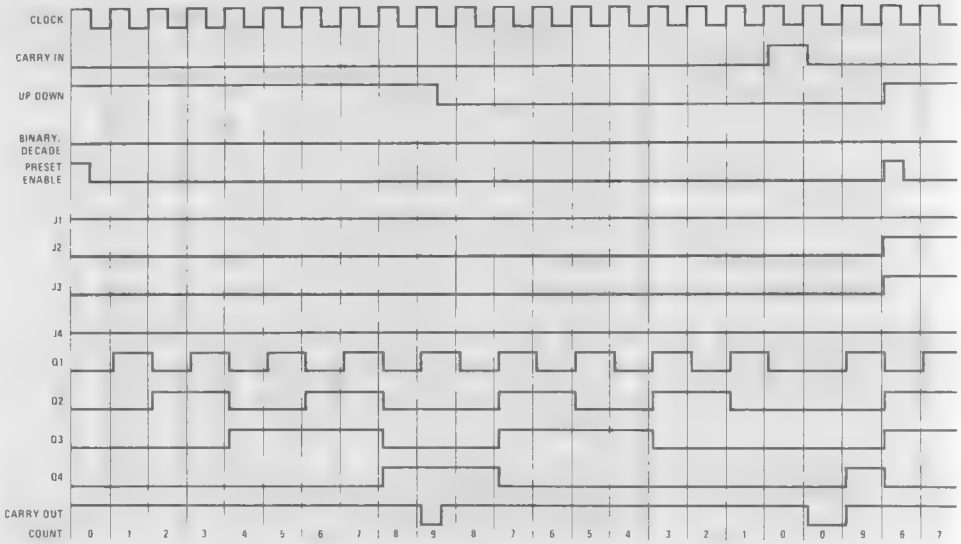
Dual-In-Line Package



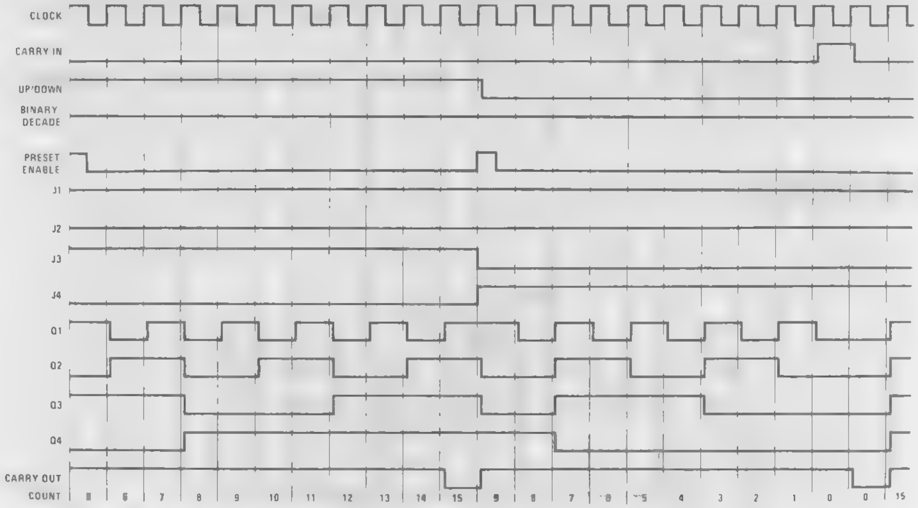
TOP VIEW

Logic Waveforms

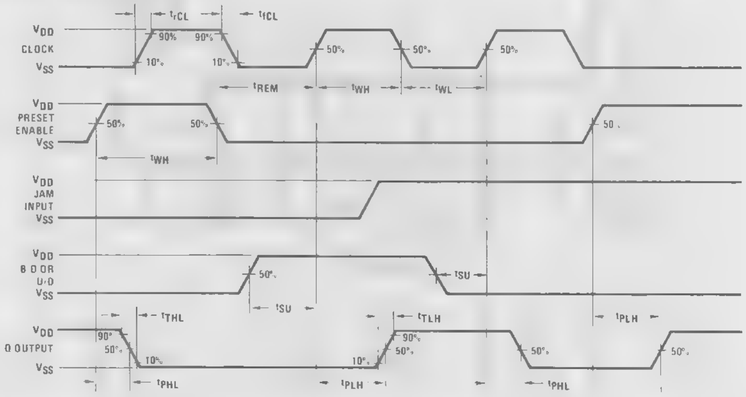
Decade Mode



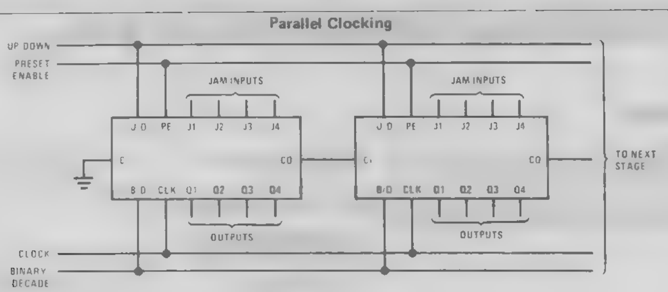
Binary Mode



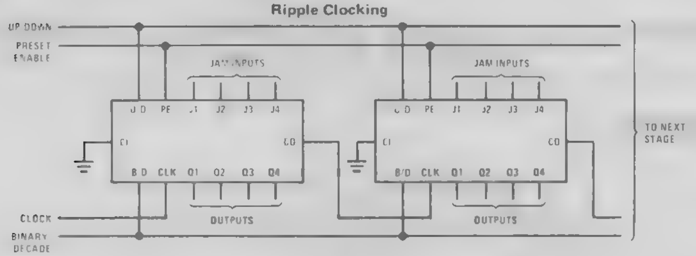
Switching Time Waveforms



Parallel Clocking



Ripple Clocking



Carry out lines at the 2nd or later stages may have a negative-going spike due to differential internal delays. These spikes do not affect counter operation, but if the carry out is used to trigger external circuitry the carry out should be gated with the clock.

National Semiconductor

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

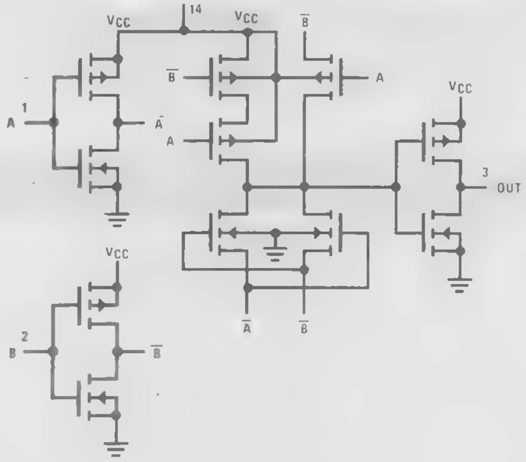
Features

- Wide supply voltage range 3.0 V to 15 V
- Low power 100 nW (typ.)
- Medium speed operation $t_{PHL} = t_{PLH} = 40$ ns (typ.) at $C_L = 15$ pF, 10 V supply
- High noise immunity 0.45 V_{CC} (typ.)

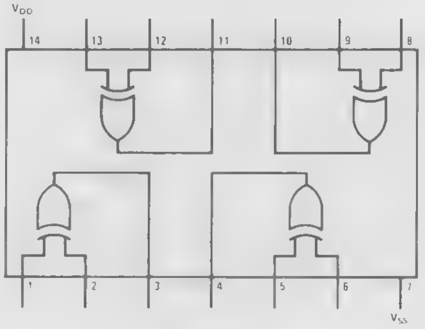
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

Schematic Diagram



Connection Diagram



TOP VIEW

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4030M	–55°C to +125°C
CD4030C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			2.5		0.025	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
	V_{DD} = 10V			0.05		0	0.05			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	V_{DD} = 10V	9.95			9.95	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
	V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	–0.45			-0.3	–0.6		–0.21			mA
	V_{DD} = 10V	–0.95			–0.65	–1.3		–0.45			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

DC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40 C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.05	5.0			70	μA
	V_{DD} = 10V			10		0.1	10			140	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		0.25	25			350	μW
	V_{DD} = 10V			100		1.0	100			1,400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V	–	–	0.05		0	0.05			0.05	V
	V_{DD} = 10V			0.05		0	0.05			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	V_{DD} = 10V	9.95			9.95	10		9.95			V
Noise Immunity (All Inputs)(V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0	0.35			0.3	1.2		0.25			mA
	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	-0.21			0.15	–0.6		–0.12			mA
	V_{DD} = 10V	-0.45			-0.32	-1.3		–0.25			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		100	200	ns
	V_{DD} = 10V		40	100	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 5.0V		100	200	ns
	V_{DD} = 10V		40	100	ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5.0V		70	150	ns
	V_{DD} = 10V		25	75	ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5.0V		80	150	ns
	V_{DD} = 10V		30	75	ns
Input Capacitance (C_I)	V_I = 0V or V_I = V_{DD}		5.0		pF

AC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		100	300	ns
	V_{DD} = 10V		40	150	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 5.0V		100	300	ns
	V_{DD} = 10V		40	150	ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5.0V		70	300	ns
	V_{DD} = 10V		25	150	ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5.0V		80	300	ns
	V_{DD} = 10V		30	150	ns
Input Capacitance (C_I)	V_I = 0V or V_I = V_{DD}		5.0		pF

Truth Table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

CD4031BM/CD4031BC 64-Stage Static Shift Register

General Description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

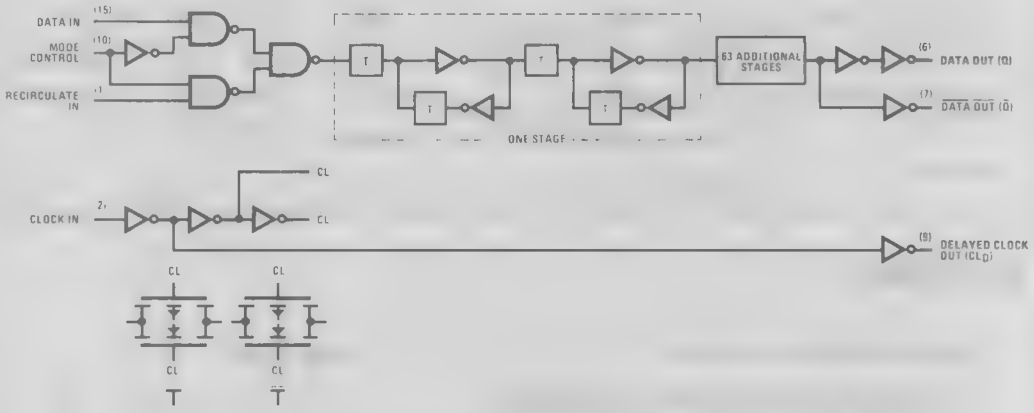
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) and $\overline{\text{DATA OUT}}$ ($\overline{Q}$) outputs are fully buffered.

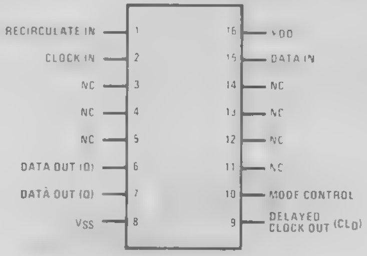
The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and present only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation DC to 8 MHz V_{DD} = 10 V (typ.)
- Fully buffered clock input 5 pF (typ.) input capacitance
- Single phase clocking requirements
- Delayed clock output for reduced clock drive requirements
- Fully buffered outputs
- High current sinking capability Q output 1.6 mA @ V_{DD} = 5 V and 25°C

Logic and Connection Diagrams





Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 V to V_{DD} + 0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD}	Supply Voltage	+3 V to +15 V
V_{IN}	Input Voltage	0 V to V_{DD}
T_A	Operating Temperature Range	
	CD4031BM	−55°C to +125°C
	CD4031BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) CD4031BM

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		5		0.01	5		150	μA
		V_{DD} = 10 V		10		0.01	10		300	μA
		V_{DD} = 15 V		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V; V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V; V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\,\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V; $\|I_O\| < 1\,\mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V; $\|I_O\| < 1\,\mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output	V_{DD} = 5 V, V_O = 0.4 V; V_{IH} = V_{DD}, V_{IL} = 0 V	2.3		1.9	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V	5.1		4.2	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V	10.5		8.8	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs	V_{DD} = 5 V, V_O = 0.4 V; V_{IH} = V_{DD}, V_{IL} = 0 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O − 0.5 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs	V_{DD} = 5 V, V_O = 4.6 V; V_{IH} = V_{DD}, V_{IL} = 0 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

Truth Tables

MODE CONTROL (data selection)

MODE CONTROL	DATA IN	RECIRCULATE IN	DATA INTO FIRST STAGE
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

EACH STAGE

D_n	CL	Q_n
0	↗	0
1	↗	1
X	↘	NC

X = irrelevant
NC = no change
↗ = Low to High level transition
↘ = High to Low level transition

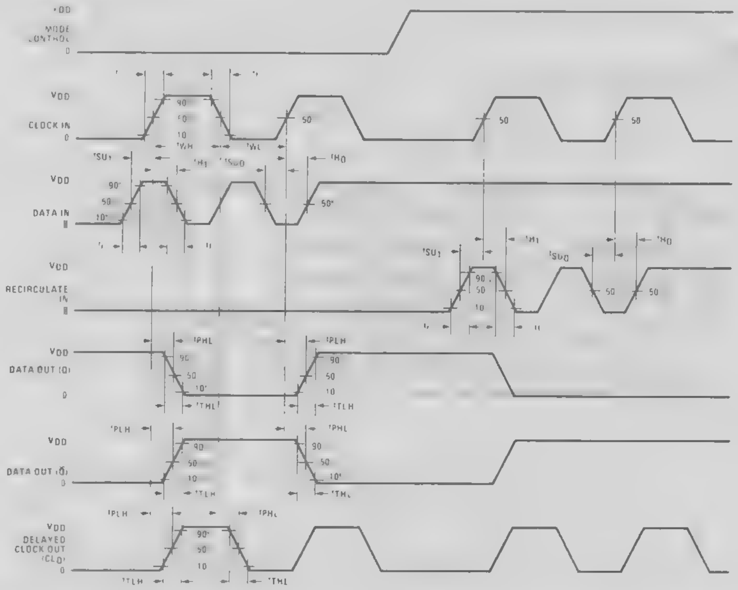
DC Electrical Characteristics (Note 2) CD4031BC

PARAMETER		CONDITIONS		–40°C		+25°C			+85°C		UNITS
				MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V			20		0.01	20		150	μA
		V_{DD} = 10 V			40		0.01	40		300	μA
		V_{DD} = 15 V			80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V	V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V			0.05		0	0.05		0.05	V
		V_{DD} = 15 V			0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10 V		9.95		9.95	10		9.95		V
		V_{DD} = 15 V		14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	$\|I_O\| < 1\ \mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V			3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V			4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	$\|I_O\| < 1\ \mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output	V_{DD} = 5 V, V_O = 0.4 V	V_{IH} = V_{DD} V_{IL} = 0 V	1.8		1.6	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V		4.0		3.5	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V		8.7		7.5	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs	V_{DD} = 5 V, V_O = 0.4 V	V_{IH} = V_{DD} V_{IL} = 0 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V		1.3		1.1	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V		3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs	V_{DD} = 5 V, V_O = 4.6 V	V_{IH} = V_{DD} V_{IL} = 0 V	–0.52		–0.44	–0.88		–0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V		–1.3		–1.1	–2.25		–0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V		–3.6		–3.0	–8.8		–2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V			–0.3		-10^{-5}	–0.3		–1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V			0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Switching Time Waveforms



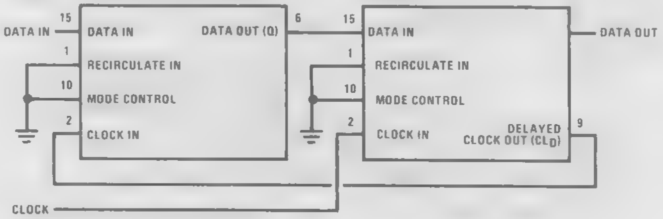
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to Q and $\overline{Q}$	$V_{CC} = 5\,V$		300	600	ns
		$V_{CC} = 10\,V$		125	250	ns
		$V_{CC} = 15\,V$		100	200	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to CL_D	$V_{CC} = 5\,V$		125	250	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
t_{THL}, t_{TLH}	Output Transition Time, All Outputs	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{SU_0} t_{SU_1}	Minimum Data Setup Time, DATA IN or RECIRCULATE IN to Clock	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{H_0} t_{H_1}	Minimum Data Hold Time, Clock to DATA IN or RECIRCULATE IN	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{CC} = 5\,V$		150	300	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
f_{CL}	Maximum Clock Frequency	$V_{CC} = 5\,V$	1.6	3.2		MHz
		$V_{CC} = 10\,V$	4.0	8.0		MHz
		$V_{CC} = 15\,V$	5.0	10		MHz
t_{RCL}, t_{FCL}	Maximum Clock Input Rise and Fall Times (Note 3)	$V_{CC} = 5\,V$	15			μs
		$V_{CC} = 10\,V$	10			μs
		$V_{CC} = 15\,V$	5			μs
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 3: When clocking cascaded packages in parallel, one should insure that: $t_r\,CL \leq 2(t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

Block Diagram

cascading packages using DELAYED CLOCK (CL_D) output



CD4034BM/CD4034BC 8-State TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

A ENABLE (AE): "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B): This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

ASYNCHRONOUS/SYNCHRONOUS (A/S): When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

PARALLEL/SERIAL (P/S): A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

CLOCK: Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

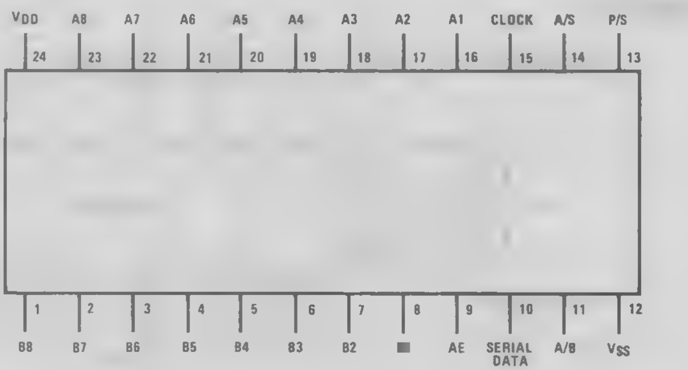
Features

■ Wide supply voltage range	3.0 to 18 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ RCA CD4034B second source	

Applications

- Parallel Input/Parallel Output
  Parallel Input/Serial Output
  Serial Input/Parallel Output
  Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

Connection Diagram



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD}	DC Supply Voltage	$+3\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4034BM	−55°C to +125°C
	CD4034BC	−40°C to +85°C

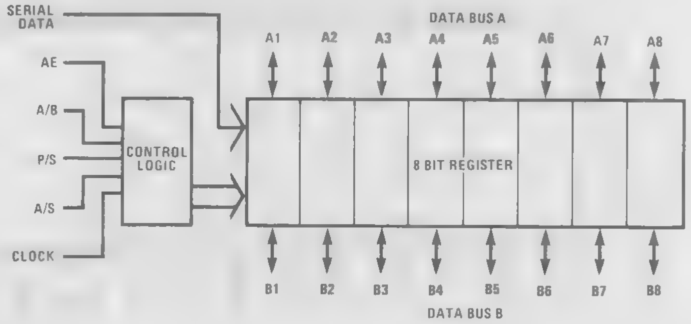
DC Electrical Characteristics CD4034BM (Note 2)

PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5\ V$		5			5		150	μA
	$V_{DD} = 10\ V$		10			10		300	μA
	$V_{DD} = 15\ V$		20			20		600	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5\ V$		0.05			0.05		0.05	V
	$V_{DD} = 10\ V$		0.05			0.05		0.05	V
	$V_{DD} = 15\ V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5\ V$	4.95		4.95			4.95		V
	$V_{DD} = 10\ V$	9.95		9.95			9.95		V
	$V_{DD} = 15\ V$	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ or $4.5\ V$		1.5			1.5		1.5	V
	$V_{DD} = 10\ V$, $V_O = 1.0\ V$ or $9.0\ V$		3.0			3.0		3.0	V
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$ or $13.5\ V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ or $4.5\ V$	3.5		3.5			3.5		V
	$V_{DD} = 10\ V$, $V_O = 1.0\ V$ or $9.0\ V$	7.0		7.0			7.0		V
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$ or $13.5\ V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5\ V$, $V_O = 0.4\ V$	0.64		0.51			0.36		mA
	$V_{DD} = 10\ V$, $V_O = 0.5\ V$	1.6		1.3			0.9		mA
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$	4.2		3.4			2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5\ V$, $V_O = 4.6\ V$	−0.64		−0.51			−0.36		mA
	$V_{DD} = 10\ V$, $V_O = 9.5\ V$	−1.6		−1.3			−0.9		mA
	$V_{DD} = 15\ V$, $V_O = 13.5\ V$	−4.2		−3.4			−2.4		mA
I_{IN} Input Current	$V_{DD} = 15\ V$, $V_{IN} = 0\ V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\ V$, $V_{IN} = 15\ V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ} Tri-State Leakage Current	$V_{DD} = 15\ V$, $V_O = 0\ V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\ V$, $V_O = 15\ V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0\ V$ unless otherwise specified.

Logic Diagram



DC Electrical Characteristics CD4034BC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		20			20		150	μA
		V_{DD} = 10 V		40			40		300	μA
		V_{DD} = 15 V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
		V_{DD} = 15 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
		V_{DD} = 15 V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44			0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1			0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0			2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	Tri-State Leakage Current	V_{DD} = 15 V, V_O = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_O = 15 V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, Input $t_r = t_f$ = 20 ns, unless otherwise specified

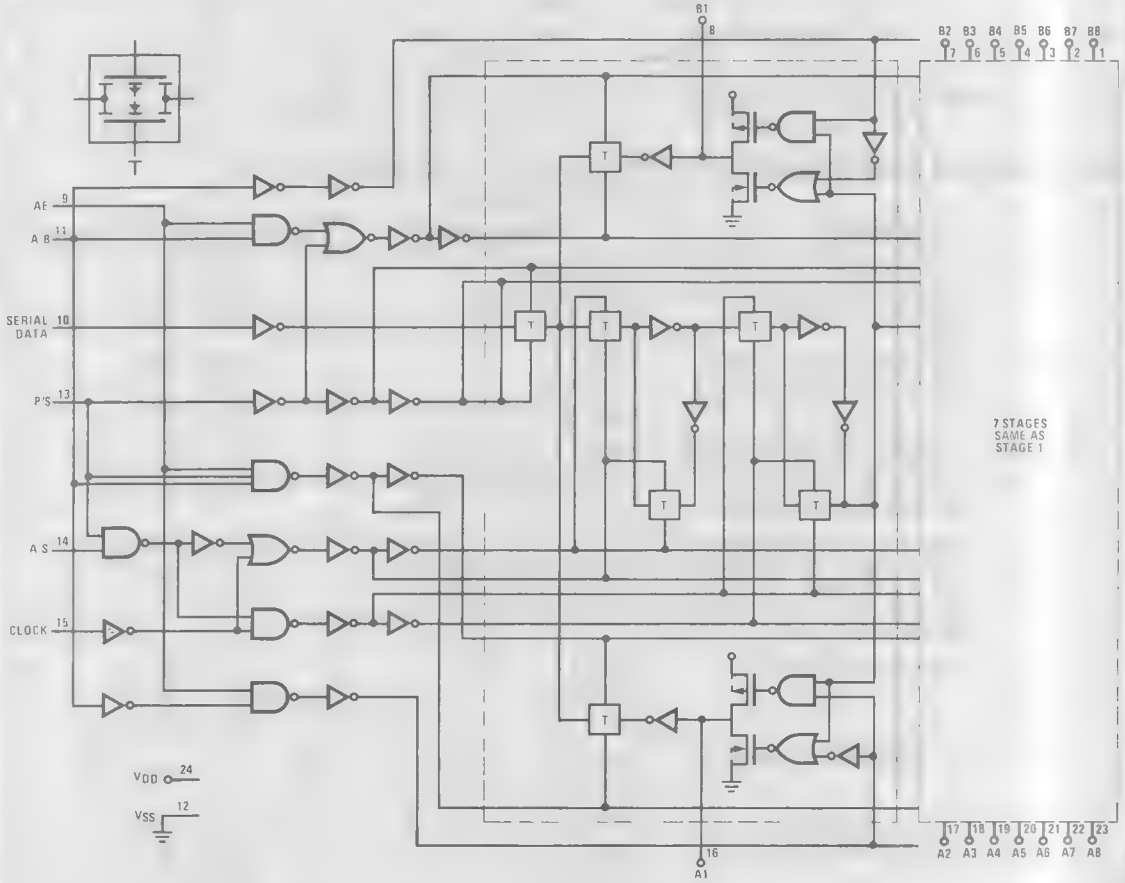
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) Synchronous Parallel Data or Serial Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) A(B) Asynchronous Parallel Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		95	220	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		60	130	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		45	100	ns
t_{PZH}, t_{PZL}	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		180	480	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		75	190	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		55	140	ns
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5 V	2	4		MHz
		V_{DD} = 10 V	5	10		MHz
		V_{DD} = 15 V	7	14		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5 V		125	250	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		35	70	ns

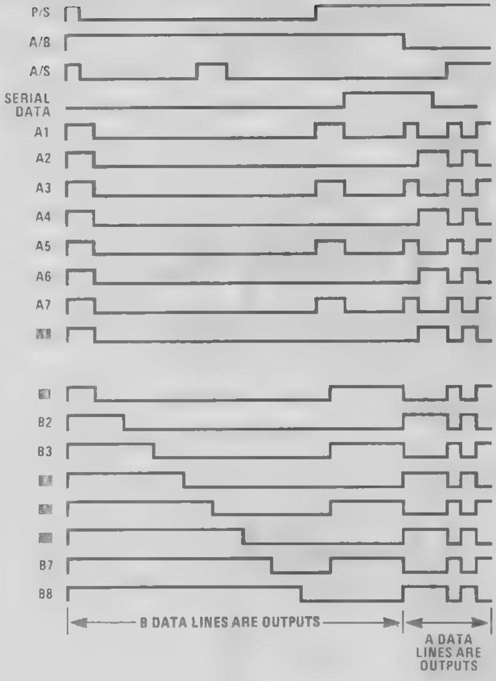
AC Electrical Characteristics (Cont'd.)

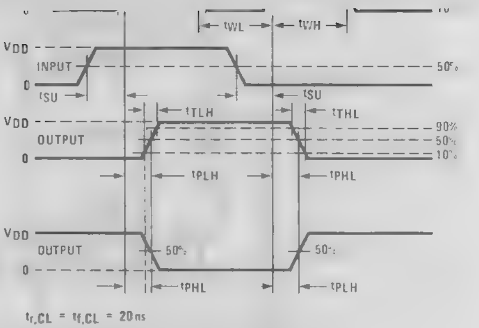
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{RCL}, t_{FCL}	Maximum Clock Rise & Fall Time	V_{DD} = 5 V	15			μs
		V_{DD} = 10 V	15			μs
		V_{DD} = 15 V	15			μs
t_{SU}	Parallel (A or B) and Serial Data Setup Time	V_{DD} = 5 V		25	70	ns
		V_{DD} = 10 V		10	30	ns
		V_{DD} = 15 V		7	20	ns
t_{SU}	Control Inputs AE, A/B, P/S, A/S Setup Time	V_{DD} = 5 V		110	280	ns
		V_{DD} = 10 V		35	100	ns
		V_{DD} = 15 V		20	60	ns
t_{WH}	Minimum High Level AE, A/B, P/S, A/S Pulse Width	V_{DD} = 5 V		160	400	ns
		V_{DD} = 10 V		70	160	ns
		V_{DD} = 15 V		40	90	ns
C_{IN}	Average Input Capacitance	A and B Data I/O and A/B Control Input		7	15	pF
		Any Other Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		155		pF

Note 3: C_{PD} determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

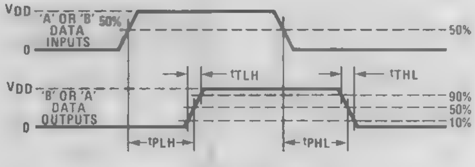
Schematic Diagram



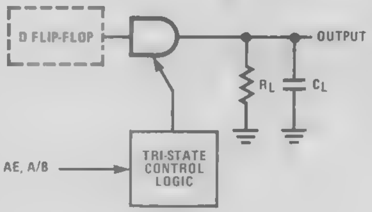


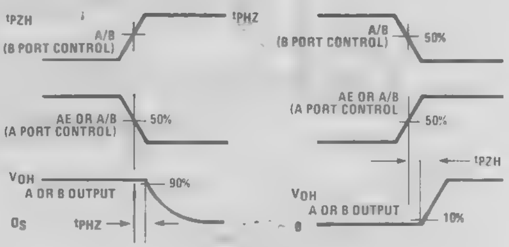


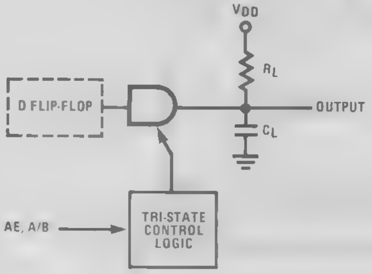
Synchronous Operation

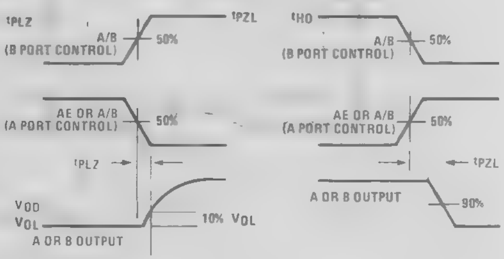


Asynchronous Operation

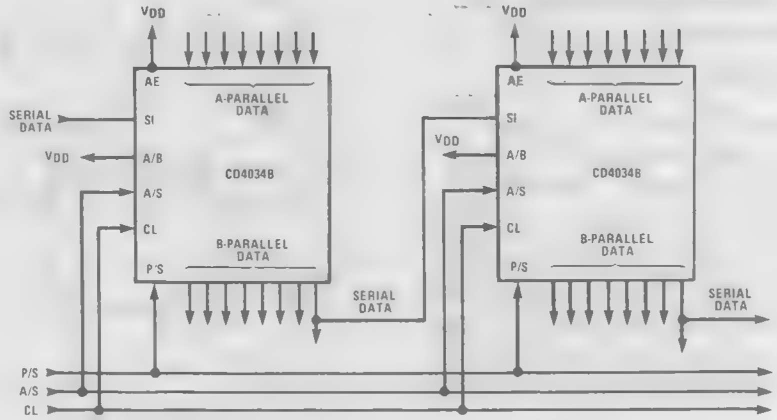




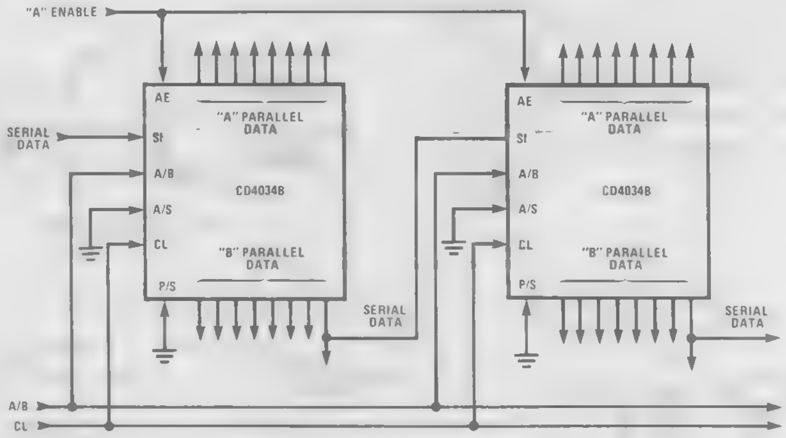




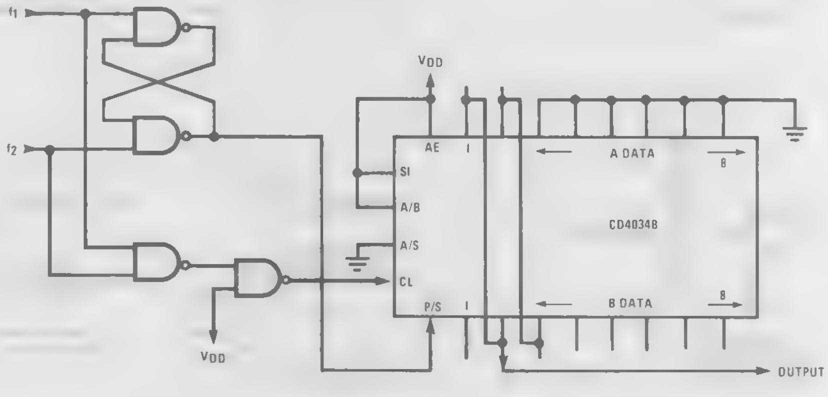
Applications



16-Bit parallel in/parallel out,parallel in/ serial out, serial in/parallel out, serial in/ serial out register.

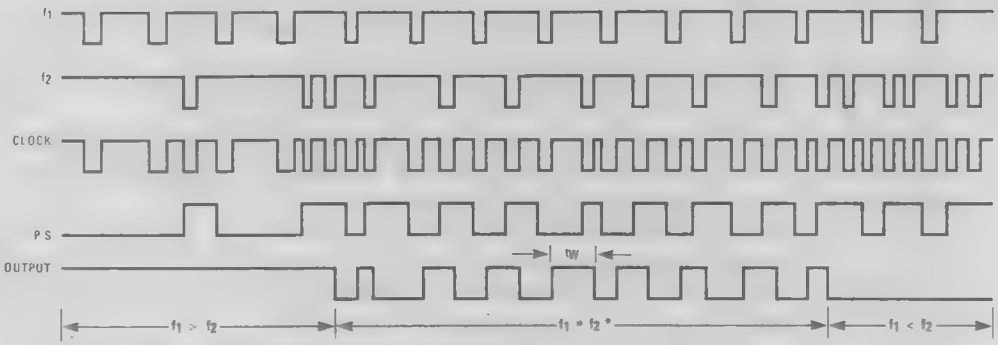


16-Bit serial in/gated parallel out register.

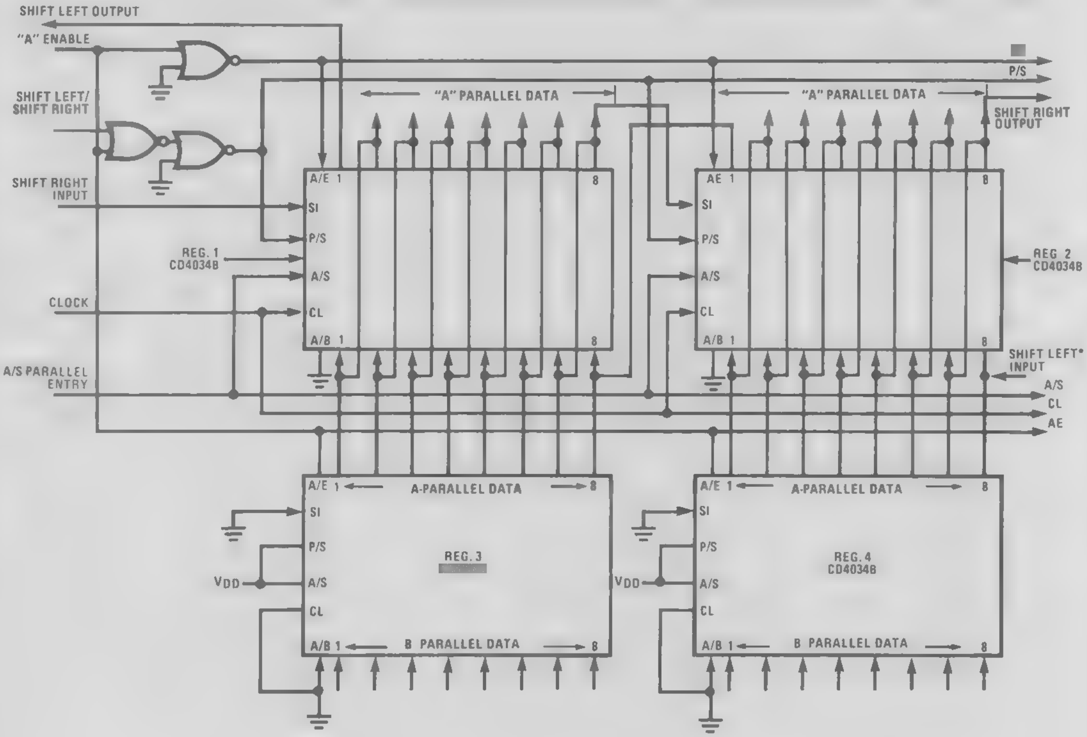


Frequency and Phase Comparator

Applications (Cont'd.)



*WHEN $f_1 = f_2$, t_W IS PROPORTIONAL TO THE PHASE OF f_1 WITH RESPECT TO f_2



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Shift Right/Shift Left with Parallel Inputs

Truth Table

"A" ENABLE	P/S	A/B	A/S	MODE	OPERATION*
0	0	0	X	Serial	Synchronous Serial data input, A- and B-Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.

CD4035BM/CD4035BC 4-Bit Parallel-In/Parallel-Out Shift Register

General Description

The CD4035B 4-bit parallel-in/parallel-out shift register is a monlithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. This shift register is a 4-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (parallel/serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the parallel/serial control is "high".

In the parallel or serial mode, information is transferred on positive clock transitions.

When the true/complement control is "high", the true contents of the register are available at the output terminals. When the true/complement control is "low", the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

J$\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

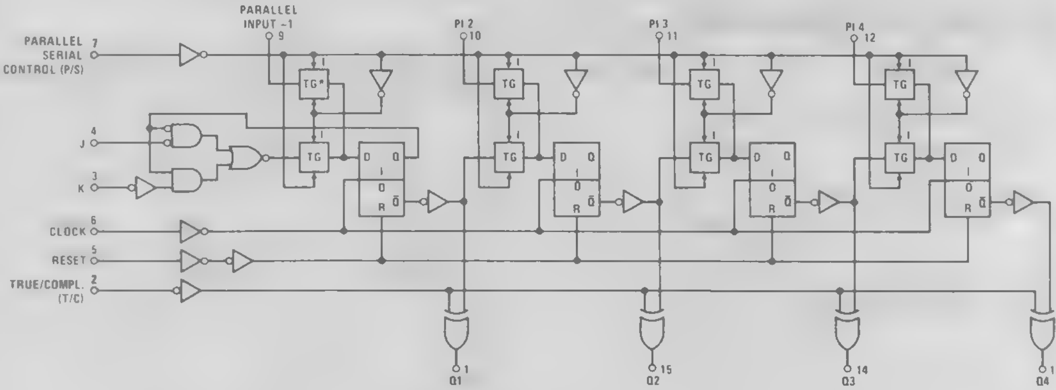
Features

Wide supply voltage range	3.0V to 15V
High noise immunity	0.45 V_{DD} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
4-stage clocked operation	
Synchronous parallel entry on all 4 stages	
J$\overline{K}$ inputs on first stage	
Asynchronous true/complement control on all outputs	
Reset Control	
Static flip-flop operation; master/slave configuration	
Buffered outputs	
Low power dissipation	5 μW (typ.) (ceramic)
High speed	to 5 MHz

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

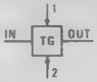
Logic Diagram



P/S = 0 = serial mode

T/C = 1 = true outputs

*TG = transmission gate



Input to output is:

a) A bidirectional low impedance when control input 1 is low and control input 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4035BM	−55°C to +125°C
CD4035BC	−40°C to +85°C

DC Electrical Characteristics CD4035BM (Note 2)

PARAMETER		CONDITIONS	55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1.0\,\mu A$								
		V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1.0\,\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$I_O < 1.0\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1.0\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		0.2	0.36		0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		0.5	0.9		0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4035BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V

DC Electrical Characteristics (Cont'd.) CD4035BC (Note 2)

PARAMETER		CONDITIONS		−40°C		25°C			85°C		UNITS
				MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V,	V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V,	V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V,	V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V,	V_O = 4.6V	−0.2		−0.16	0.36		−0.12		mA
		V_{DD} = 10V,	V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V,	V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V,	V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V,	V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_r and $t_f = 20$ ns, unless otherwise specified.

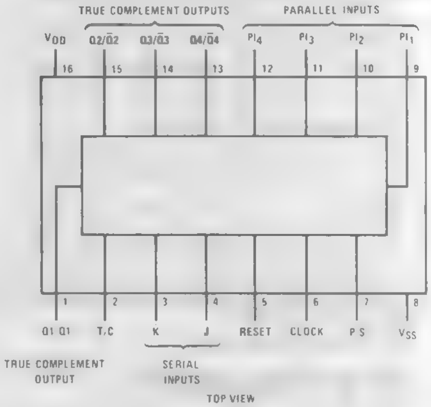
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}	Transition Time High Low to High	V_{DD} = 5V		90	175	ns
		V_{DD} = 10V		50	75	ns
		V_{DD} = 15V		40	60	ns
t_{TLH}	Transition Time Low to High	V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		60	120	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V	335	135		ns
		V_{DD} = 10V	165	50		ns
		V_{DD} = 15V	100	40		ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	µs
		V_{DD} = 10V			10	µs
		V_{DD} = 15V			5	µs
t_S	Minimum Set-up Time					
	$J/\overline{K}$ Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_S	Parallel-In Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_S	P/S Control	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	60	ns
f_{MAX}	Maximum Clock Frequency	V_{DD} = 5V	1.5	2.5		MHz
		V_{DD} = 10V	3	6		MHz
		V_{DD} = 15V	5	9		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	500	ns
		V_{DD} = 10V		150	200	ns
		V_{DD} = 15V		85	150	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		75	250	ns
		V_{DD} = 10V		30	110	ns
		V_{DD} = 15V		25	80	ns

Truth Table

C_L	$t_n - 1$ (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑	0	X	0	0	0
↑	I	X	0	0	I
↑	X	0	0	I	0
↑	I	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↑	X	I	0	I	I
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	I	X	0

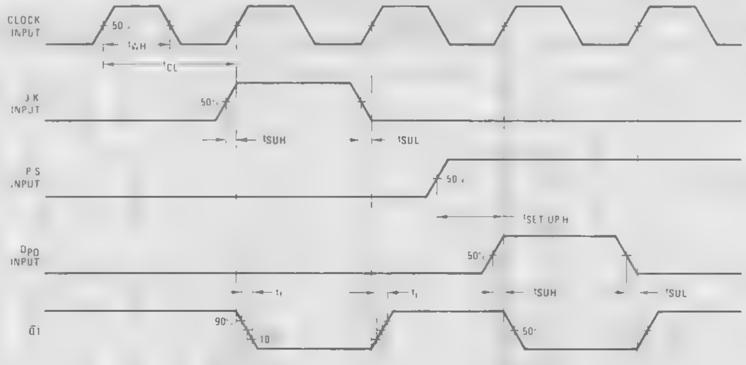
Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Switching Time Waveforms



T/C Input Low
Reset Input Low

CD4041M/CD4041C Quad True/Complement Buffer

General Description

The CD4041M/CD4041C is a quad true/complement buffer consisting of N- and P-channel enhancement mode transistors having low-channel resistance and high current (sourcing and sinking) capability. The CD4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver.

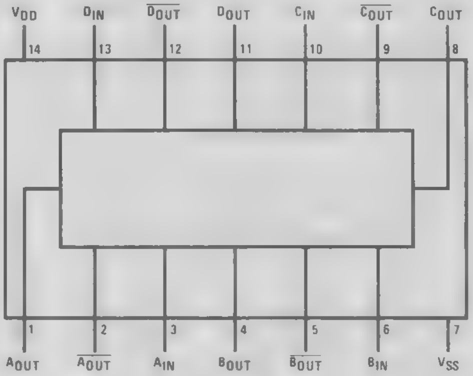
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 40% V_{DD} (typ.)
- True output
  High current source and sink capability
  8 mA (typ.) @ $V_O = 9.5\,V$, $V_{DD} = 10\,V$
  3.2 mA (typ.) @ $V_O = 0.4\,V$, $V_{DD} = 5\,V$ (two TTL loads)
- Complement output
  Medium current source and sink capability
  3.6 mA (typ.) @ $V_O = 9.5\,V$, $V_{DD} = 10\,V$
  1.6 mA (typ.) @ $V_O = 0.4\,V$, $V_{DD} = 5\,V$

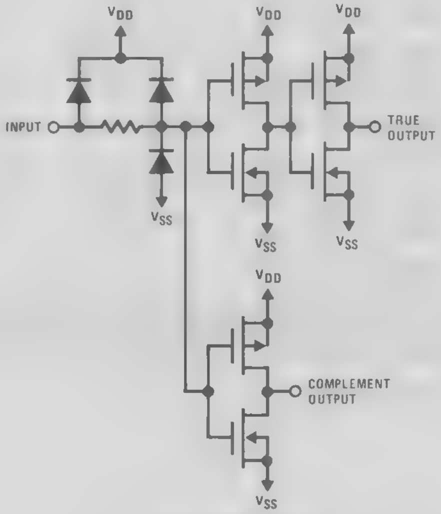
Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Schematic Diagram



1 of 4 Identical Units

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4041M	−55°C to +125°C
CD4041C	−40°C to +85°C

DC Electrical Characteristics CD4041M (Note 2)

	PARAMETER	CONDITIONS	55 C		25 C			125 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.01	1		30	μA
		V_{DD} = 10V		2		0 01	2		60	μA
		V_{DD} = 15V		4		0.01	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0 05		0	0 05		0.05	V
		V_{DD} = 10V		0.05		0	0 05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V	4 95		4.95	5		4.95		V
		V_{DD} = 10V	9 95		9 95	10		9 95		V
		V_{DD} = 15V	14 95		14 95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1 0		2	1.0		1.0	V
		V_{DD} = 10V, V_O = 1V or 9V		2.0		4	2 0		2.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		3 0		6	3.0		3 0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	4 0		4 0	3		4.0		V
		V_{DD} = 10V, V_O = 1V or 9V	8 0		8 0	6		8.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current True Output	V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	2 1		1 6	3.2		1.2		mA
		V_{DD} = 10V, V_O = 0.5V	6 25		5.0	10		3 5		mA
		V_{DD} = 15V, V_O = 1.5V	14		12	24		8		mA
I_{OL}	Low Level Output Current Complement Output	V_{IH} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	1.0		0.8	1.6		0.55		mA
		V_{DD} = 10V, V_O = 0.5V	2.5		2	4.0		1 4		mA
		V_{DD} = 15V, V_O = 1.5V	5.5		4 5	9.0		3.0		mA
I_{OH}	High Level Output Current True Output	V_{IH} = V_{DD}								
		V_{DD} = 5V, V_O = 4.6V	−1 75		−1 4	2 8		1 0		mA
		V_{DD} = 10V, V_O = 9.5V	−5.0		−4 0	−8 0		2 8		mA
		V_{DD} = 15V, V_O = 13.5V	−11		9	−18		6		mA
I_{OH}	High Level Output Current Complement Output	V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	0 75		0 6	1 2		0 4		mA
		V_{DD} = 10V, V_O = 9.5V	2 25		1 8	3 6		1 25		mA
		V_{DD} = 15V, V_O = 13.5V	4 8		−4	−8		2 7		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0 1		10^{5}	−0 1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0 1		10^{5}	0 1		1 0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

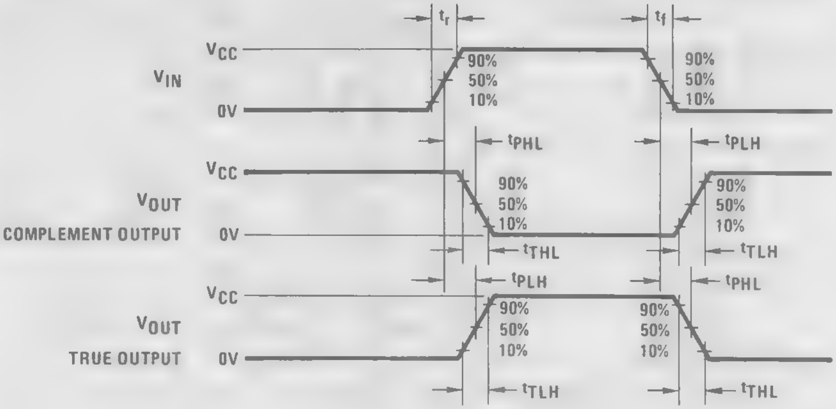
DC Electrical Characteristics CD4041C (Note 2)

	PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		4		0.01	4		30	μA
		$V_{DD} = 10V$		8		0.01	8		60	μA
		$V_{DD} = 15V$		16		0.01	16		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$, $V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$, $V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.0		2	1.0		1.0	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		2.0		4	2.0		2.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	4.0		4.0	3		4.0		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	8.0		8.0	6		8.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current True Output	$V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	1.7		1.5	3.2		1.2		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	4.9		4.3	10		3.5		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	11		10	24		8		mA
I_{OL}	Low Level Output Current Complement Output	$V_{IH} = V_{DD}$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.75		0.68	1.6		0.55		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	2.0		1.8	4.0		1.4		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.4		3.8	9.0		3.0		mA
I_{OH}	High Level Output Current True Output	$V_{IH} = V_{DD}$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−1.5		−1.3	−2.8		−1.0		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−4.0		−3.5	−8.0		−2.8		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−8.7		−7.5	−18		−6		mA
I_{OH}	High Level Output Current Complement Output	$V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−0.57		−0.50	−1.2		−0.4		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.8		−1.6	−3.6		−1.25		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.9		−3.4	−8.0		−2.7		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time True Output	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		35	70	ns
		$V_{DD} = 15V$		25	50	ns
t_{PHL} or t_{PLH}	Propagation Delay Time Complement Output	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	65	ns
t_{THL} or t_{TLH}	Output Transition Time True Output	$V_{DD} = 5V$		55	110	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{THL} or t_{TLH}	Output Transition Time Complement Output	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		45	90	ns
		$V_{DD} = 15V$		35	75	ns
C_{IN}	Input Capacitance	Any Input		10	15	pF

Switching Time Waveforms



CD4042BM/CD4042BC Quad Clocked D Latch

General Description

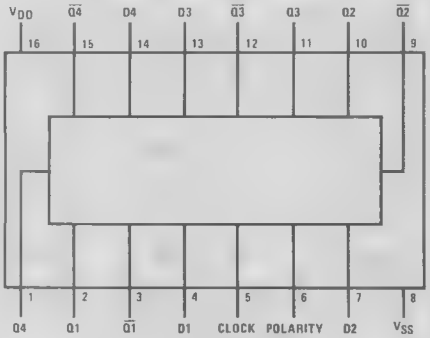
The CD4042BM/CD4042BC quad clocked "D" latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. The outputs Q and $\overline{Q}$ either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity = 0; the information present at the data input is transferred to Q and $\overline{Q}$ during 0 clock level; and for polarity = 1, the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity = 0 and negative for polarity = 1), the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Clock polarity control	
■ Fully buffered data inputs	
■ Q and $\overline{Q}$ outputs	

Connection Diagram

Dual-In-Line and Flat Package

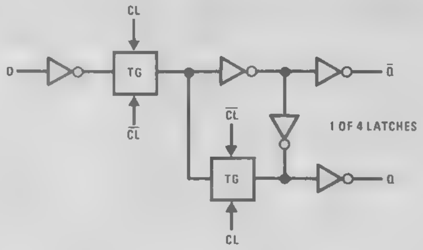


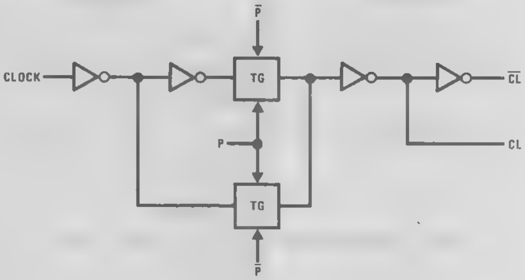
TOP VIEW

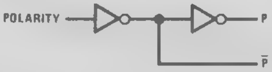
Truth Table

CLOCK	POLARITY	Q
0	0	D
↑	0	Latch
1	1	D
↓	1	Latch

Logic Diagrams







Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4042BM	−55°C to +125°C
CD4042BC	−40°C to +85°C

DC Electrical Characteristics CD4042BM (Note 2)

PARAMETERS		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.02	1		30	μA
		V_{DD} = 10V		2		0.02	2		60	μA
		V_{DD} = 15V		4		0.02	4		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4042BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.02	4		30	μA
		V_{DD} = 10V		8		0.02	8		60	μA
		V_{DD} = 15V		16		0.02	16		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\,\mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4042BC (Note 2)

PARAMETER		CONDITIONS	40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\,\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	0.52		−0.44	0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

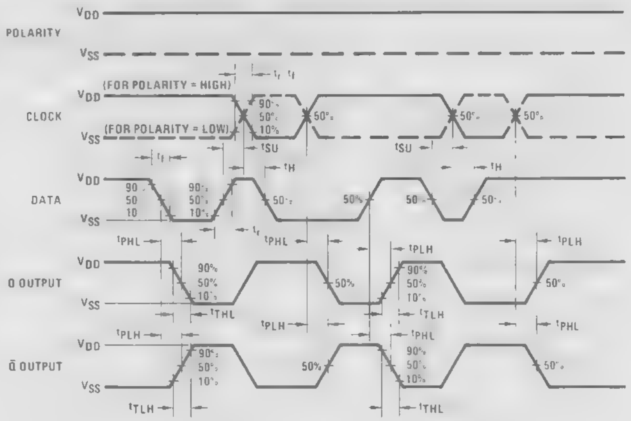
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to Q	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to $\overline{Q}$	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to $\overline{Q}$	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		90	180	ns
t_H	Minimum Hold Time	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		0	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	25	ns
t_W	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		30	60	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Switching Time Waveforms



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CD4043BM/CD4043BC Quad TRI-STATE® NOR R/S Latches
CD4044BM/CD4044BC Quad TRI-STATE® NAND R/S Latches

General Description

CD4043BM/CD4043BC are quad cross-couple TRI-STATE CMOS NOR latches, and CD4044BM/CD4044BC are quad cross-couple TRI-STATE CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. There is a common TRI-STATE ENABLE input for all four latches. A logic "1" on the ENABLE input connects the latch states to the Q outputs. A logic "0" on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The TRI-STATE feature allows common bussing of the outputs.

TRI-STATE is a trademark of National Semiconductor Corp.

Features

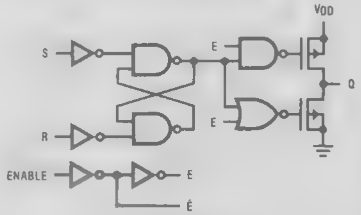
- Wide supply voltage range 3 V to 15 V
- Low power 100 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)
- Separate SET and RESET inputs for each latch
- NOR and NAND configuration
- TRI-STATE output with common output enable

Applications

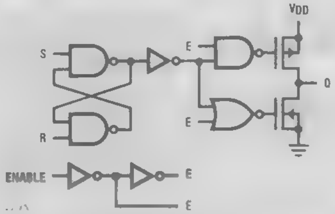
- Multiple bus storage
- Stobed register
- Four bits of independent storage with output enable
- General digital logic

Schematic and Connection Diagrams

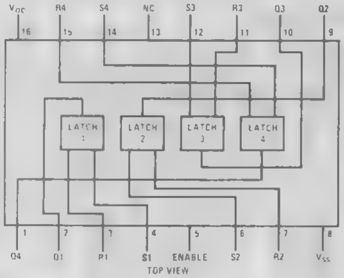
CD4043M/CD4043C



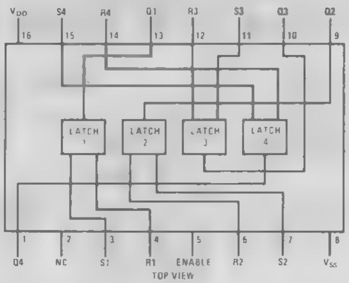
CD4044M/CD4044C



CD4043BM/CD4043BC
Dual-In-Line and Flat Packages



CD4044BM/CD4044BC
Dual-In-Line and Flat Packages



Truth Table

CD4043BM/CD4043BC

S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

CD4044BM/CD4044BC

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

OC – TRI-STATE
NC – No change
X Don't care
Δ – Dominated by S=1 input
ΔΔ – Dominated by R=0 input

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18 V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3.0 to 15 V
V_{IN} Input Voltage	0 to V_{DD} V
T_A Operating Temperature Range	
CD4043BM, CD4044BM	−55°C to +125°C
CD4043BC, CD4044BC	−40°C to +85°C

DC Electrical Characteristics CD4043BM/CD4044BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD} = 5.0\,V$		5.0		0.01	5.0		150	μA
	$V_{DD} = 10\,V$		10		0.01	10		300	μA
	$V_{DD} = 15\,V$		20		0.02	20		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$, $V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15\,V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$, $V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0\,V$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10\,V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15\,V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\lvert I_O \rvert \leq 1\,\mu A$								
	$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$\lvert I_O \rvert \leq 1\,\mu A$								
	$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 5.0\,V$, $V_O = 1.0\,V$ or $9.0\,V$	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$	11		11	8.25		11		V
I_{OL} Low Level Output Current	$V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$	0.64		0.51	1.0		0.36		mA
	$V_{DD} = 10\,V$, $V_O = 0.5\,V$	1.6		1.3	2.6		0.9		mA
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$	4.2		3.4	6.8		2.4		mA
I_{OH} High Level Output Current	$V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0\,V$, $V_O = 4.6\,V$	−0.25		−0.2	−0.4		−0.14		mA
	$V_{DD} = 10\,V$, $V_O = 9.5\,V$	−0.62		−0.5	−1.0		−0.35		mA
	$V_{DD} = 15\,V$, $V_O = 13.5\,V$	−1.8		−1.5	−3.0		−1.1		mA
I_{IN} Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$		−0.1		-10^{-5}	−0.1		−1.0	μA
	$V_{DD} = 15\,V$, $V_{IN} = 15\,V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4043BC/CD4044BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD} = 5.0\,V$		20		0.01	20		150	μA
	$V_{DD} = 10\,V$		40		0.01	40		300	μA
	$V_{DD} = 15\,V$		80		0.02	80		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$, $V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15\,V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$, $V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0\,V$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10\,V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15\,V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4043BC/CD4044BC (cont'd)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{IL} Low Level Input Voltage	$\lvert I_O \rvert \leq 1\mu A$								
	$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$\lvert I_O \rvert \leq 1\mu A$								
	$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
	$V_{DD} = 5.0V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11		11			11		V
I_{OL} Low Level Output Current	$V_{IL} = 0V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
	$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.2		0.9		mA
	$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	6.0		2.4		mA
I_{OH} High Level Output Current	$V_{IL} = 0V$, $V_{IH} = V_{DD}$								
	$V_{DD} = 5.0V$, $V_O = 4.6V$	−0.2		−0.16	−0.32		−0.12		mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−0.5		−0.4	−0.8		−0.3		mA
	$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2	−2.4		−1.0		mA
I_{IN} Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	−0.3			−0.3			−1.0	μA
	$V_{DD} = 15V$, $V_{IN} = 15V$	0.3			0.3			1.0	

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, Input $t_r = t_f = 20ns$, unless otherwise noted.

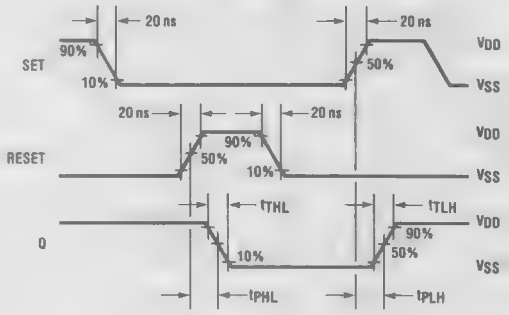
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PLH}, t_{PHL}	Propagation Delay S or R to Q	$V_{DD} = 5.0V$		175	350	ns
		$V_{DD} = 10V$		75	175	ns
		$V_{DD} = 15V$		60	120	ns
t_{PZH}, t_{PHZ}	Propagation Delay Enable to Q (High)	$V_{DD} = 5.0V$		115	230	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		40	80	ns
t_{PZL}, t_{PLZ}	Propagation Delay Enable to Q (Low)	$V_{DD} = 5.0V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5.0V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WO}	Minimum SET or RESET Pulse Width	$V_{DD} = 5.0V$		80	160	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		20	40	ns
C_{IN}	Input Capacitance			5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

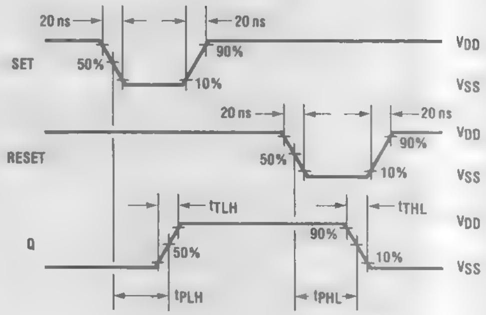
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Timing Waveforms

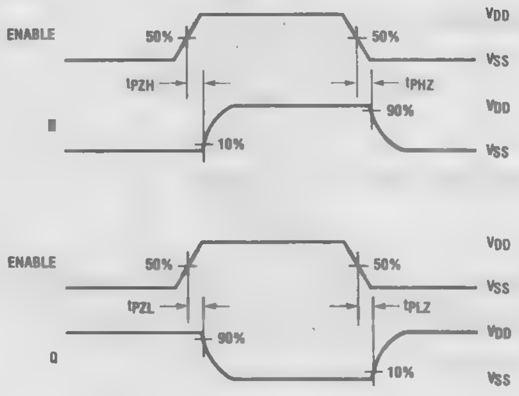
CD4043B



CD4044B



Enable Timing



National Semiconductor

CD4046BM/CD4046BC Micropower Phase-Locked Loop

General Description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

Features

Wide supply voltage range	3.0 V to 18 V
Low dynamic power consumption	70 μW (typ.) at $f_o = 10$ kHz, $V_{DD} = 5$ V
VCO frequency	1.3 MHz (typ.) at $V_{DD} = 10$ V
Low frequency drift with temperature	0.06%/°C at $V_{DD} = 10$ V
High VCO linearity	1% (typ.)

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

Block and Connection Diagrams

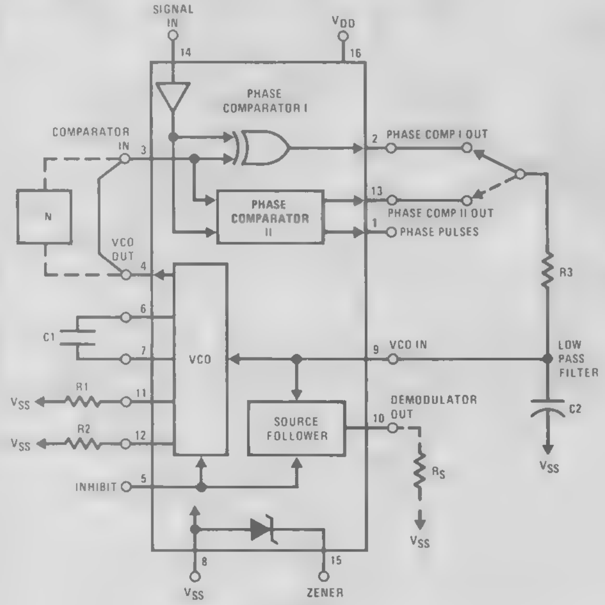
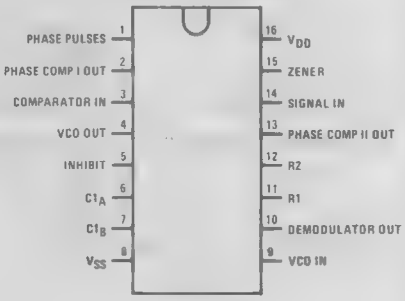


FIGURE 1

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4046BM	−55°C to +125°C
CD4046BC	−40°C to +85°C

DC Electrical Characteristics CD4046BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	PIN 5 = V_{DD}, PIN 14 = V_{DD}, PIN 3, 9 = V_{SS}								
	V_{DD} = 5V		5		0.005	5		150	μA
	V_{DD} = 10V		10		0.01	10		300	μA
	V_{DD} = 15V		20		0.015	20		600	μA
	PIN 5 = V_{DD}, PIN 14 = Open PIN 3,2 = V_{SS}								
	V_{DD} = 5V		45		5	35		185	μA
	V_{DD} = 10V		450		20	350		650	μA
	V_{DD} = 15V		1200		50	900		1500	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH} High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	All Inputs Except Signal Input								
	V_{DD} = 14V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
C_{IN} Input Capacitance	Any Input, (Note 3)							7.5	pF
P_T Total Power Dissipation	f_o = 10kHz, R1 = 1MΩ R2 = ∞, VCO_{IN} = $V_{DD}/2$								
	V_{DD} = 5V				0.07				mW
	V_{DD} = 10V				0.6				mW
	V_{DD} = 15V				2.4				mW

DC Electrical Characteristics CD4046BC (Note 2)

Parameter		Conditions	-40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	PIN 5 = V_{DD}, PIN 14 = V_{DD}, PIN 3,9 = V_{SS}								
		V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
		PIN 5 = V_{DD}, PIN 14 = Open, PIN 3,9 = V_{SS}								
		V_{DD} = 5V		70		5	55		205	μA
		V_{DD} = 10V		530		20	410		710	μA
		V_{DD} = 15V		1500		50	1200		1800	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V_{DD} = 10V, V_O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V_{DD} = 15V, V_O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 15V, V_{IN} = 0V		-0.3		-10^{-5}	-0.3		-1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
C_{IN}	Input Capacitance	Any Input, (Note 3)					7.5			pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = $V_{DD}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

AC Electrical Characteristics CD4046BM/CD4046BC $T_A = 25°C$, $C_L = 50\,pF$

Parameter	Conditions	Min	Typ	Max	Units
VCO Section					
Operating Current I_{DD}	f_o = 10kHz, R1 = 1MΩ R2 = ∞, $VCO_{IN} = V_{DD}/2$				
	V_{DD} = 5V		20		μA
	V_{DD} = 10V		90		μA
	V_{DD} = 15V		200		μA
f_{MAX} = Maximum Operating Frequency	C1 = 50 pF, 41 = 10kΩ, R2 = ∞, $VCO_{IN} = V_{DD}$				
	V_{DD} = 5V	0.4	0.8		MHz
	V_{DD} = 10V	0.6	1.2		MHz
	V_{DD} = 15V	1.0	1.6		MHz
Linearity	VCO_{IN} = 2.5V ∓0.3V, R1 ⩾ 10kΩ, V_{DD} = 5V		1		%
	VCO_{IN} = 5V ±2.5V, R1⩾400kΩ, V_{DD} = 10V		1		%
	VCO_{IN} = 7.5V ±5V, R1 ⩾ 1 MΩ, V_{DD} = 15V		1		%
Temperature-Frequency Stability No Frequency Offset, $f_{MIN} = 0$	$\%/°C \propto 1/f.\ V_{DD}$ R2 = ∞				
	V_{DD} = 5V		0.12–0.24		%/°C
	V_{DD} = 10V		0.04–0.08		%/°C
	V_{DD} = 15V		0.015–0.03		%/°C
Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
	V_{DD} = 10V		0.05–0.1		%/°C
	V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN} Input Resistance (VCO_{IN})	V_{DD} = 5V		10^6		MΩ
	V_{DD} = 10V		10^6		MΩ
	V_{DD} = 15V		10^6		MΩ
VCO Output Duty Cycle	V_{DD} = 5V		50		%
	V_{DD} = 10V		50		%
	V_{DD} = 15V		50		%
t_{THL} VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}	V_{DD} = 10V		50	100	ns
	V_{DD} = 15V		45	80	ns
Phase Comparators Section					
R_{IN} Input Resistance					
Signal Input	V_{DD} = 5V	1	3		MΩ
	V_{DD} = 10V	0.2	0.7		MΩ
	V_{DD} = 15V	0.1	0.3		MΩ
Comparator Input	V_{DD} = 5V		10^6		MΩ
	V_{DD} = 10V		10^6		MΩ
	V_{DD} = 15V		10^6		MΩ
AC-Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF f = 50 kHz				
	V_{DD} = 5V		200	400	mV
	V_{DD} = 10V		400	800	mV
	V_{DD} = 15V		700	1400	mV
Demodulator Output					
Offset Voltage ($VCO_{IN} - V_{DEM}$)	RS ⩾ 10 kΩ, V_{DD} = 5V		1.50	2.2	V
	RS ⩾ 10 kΩ, V_{DD} = 10V		1.50	2.2	V
	RS ⩾ 50 kΩ, V_{DD} = 15V		1.50	2.2	V
Linearity	RS ⩾ 50 kΩ				
	VCO_{IN} = 2.5 ±0.3V, V_{DD} = 5V		0.1		%
	VCO_{IN} = 5 ±2.5V, V_{DD} = 10V		0.6		%
	VCO_{IN} = 7.5 ±5V, V_{DD} = 15V		0.8		%
Zener Diode					
V_Z Zener Diode Voltage					
CD4046BM	I_Z = 50μA	6.7	7.0	7.3	V
CD4046BC		6.3	7.0	7.7	V
R_Z Zener Dynamic Resistance	I_Z = 1mA		100		Ω

Phase Comparator State Diagrams

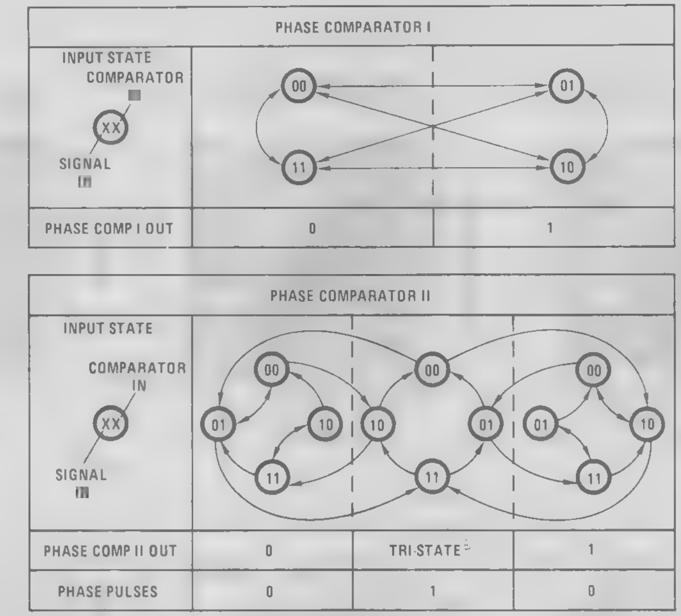


FIGURE 2

Typical Waveforms

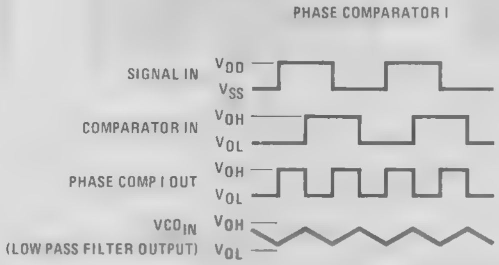


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

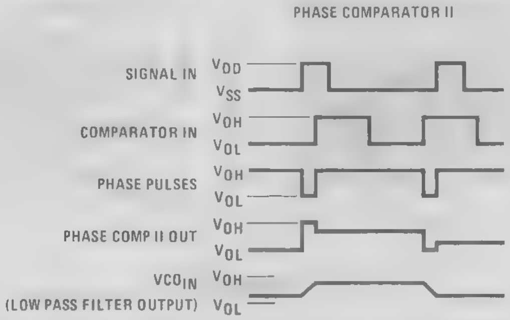


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

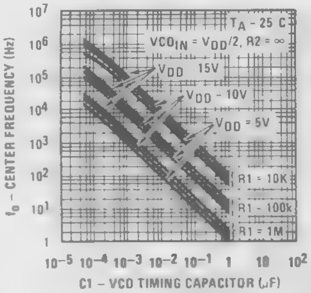

Typical Center Frequency vs C1 for R1 = 10 kΩ, 100 kΩ and 1 MΩ

FIGURE 5a

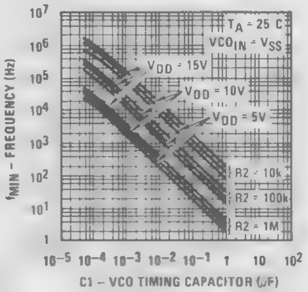

Typical Frequency Offset vs C1 for R2 = 10 kΩ, 100 kΩ and 1 MΩ

FIGURE 5b

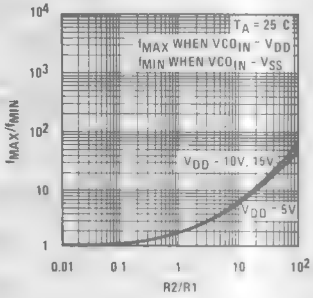

Typical f_{MAX}/f_{MIN} vs R2/R1

FIGURE 5c

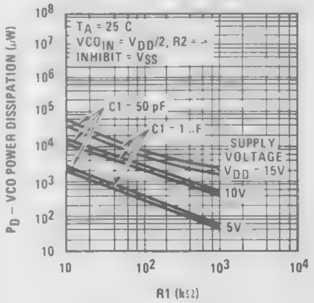

Typical VCO Power Dissipation at Center Frequency vs R1

FIGURE 6a

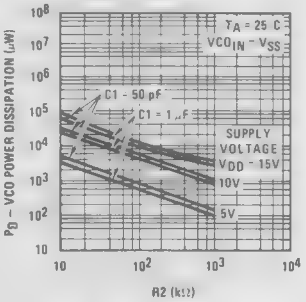

Typical VCO Power Dissipation at f_{MIN} vs R2

FIGURE 6b

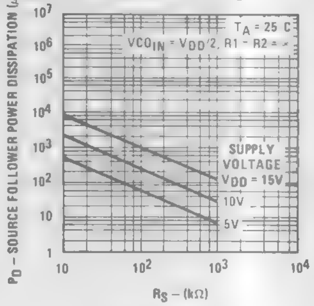

Typical Source Follower Power Dissipation vs R_S

FIGURE 6c

Typical VCO Linearity vs R1 and C1

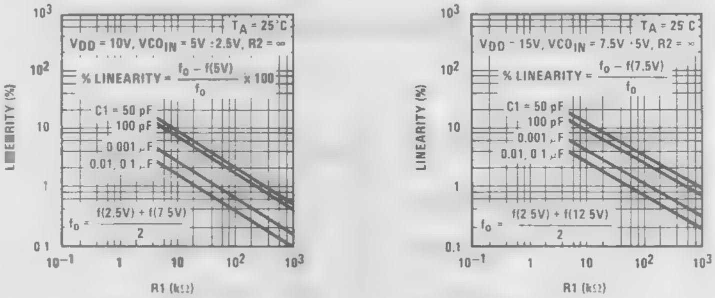
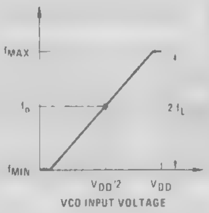
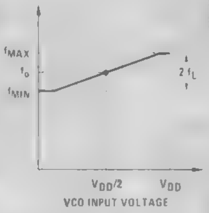
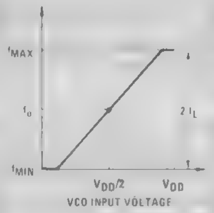
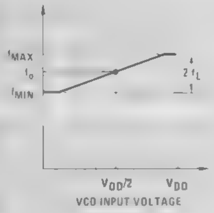
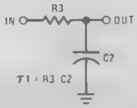
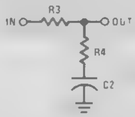


FIGURE 7

Note. To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

locked-loop system. The selected external components must be within the following ranges: R1, R2 $\geq$ 10 kΩ, $R_S \geq$ 10 kΩ, C1 $\geq$ 50 pF.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$		$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref.			
Phase Angle Between Signal and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	–Given: f_o –Use f_o with *Figure 5a* to determine R1 and C1	–Given: f_o and f_L –Calculate f_{min} from the equation $f_{min} = f_o - f_L$ –Use f_{min} with *Figure 5b* to determine R2 and C1 –Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ –Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1	–Given: f_{max} –Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with *Figure 5a* to determine R1 and C1	–Given: f_{min} and f_{max} –Use f_{min} with *Figure 5b* to determine R2 and C1 –Calculate $\frac{f_{max}}{f_{min}}$ –Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1

REF. G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
Floyd Gardner, "Phaselock Techniques," John Wiley & Sons, 1966.

National Semiconductor

CD4047BM/CD4047BC Low Power Monostable/Astable Multivibrator

General Description

CD4047B is capable of operating in either the monostable or astable mode. It requires an external capacitor (between pins 1 and 3) and an external resistor (between pins 2 and 3) to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the $\overline{\text{astable}}$ input. The output frequency (at 50% duty cycle) at Q and $\overline{Q}$ outputs is determined by the timing components. A frequency twice that of Q is available at the Oscillator Output; a 50% duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by low-to-high transition at + trigger input or high-to-low transition at − trigger input. The device can be retriggered by applying a simultaneous low-to-high transition to both the + trigger and retrigger inputs.

A high level on Reset input resets the outputs Q to low, $\overline{Q}$ to high.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

SPECIAL FEATURES

- Low power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

MONOSTABLE MULTIVIBRATOR FEATURES

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

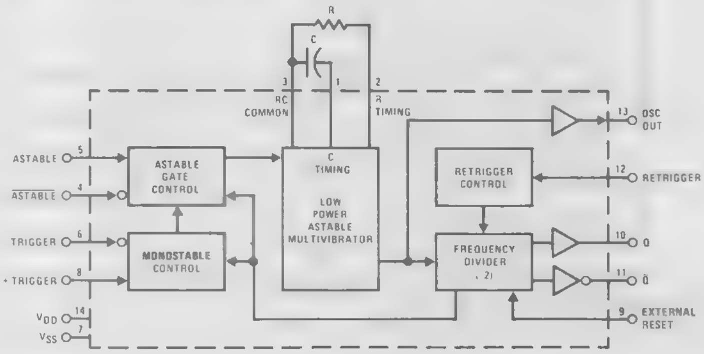
ASTABLE MULTIVIBRATOR FEATURES

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability
  typical frequency deviation = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits trimmed to frequency V_{DD} = 10 V ± 10%)

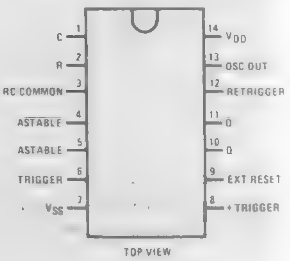
Applications

- Frequency discriminators
- Timing circuits
- Time-delay applications
- Envelope detection
- Frequency multiplication
- Frequency division

Block and Connection Diagrams



Dual-In-Line and Flat Package



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4047BM	−55°C to +125°C
CD4047BC	−40°C to +85°C

DC Electrical Characteristics CD4047BM (Note 2)

PARAMETER		CONDITIONS	55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4047BC (Note 2)

PARAMETER		CONDITIONS	40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics (Cont'd.) CD4047BC (Note 2)

PARAMETER		CONDITIONS	40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

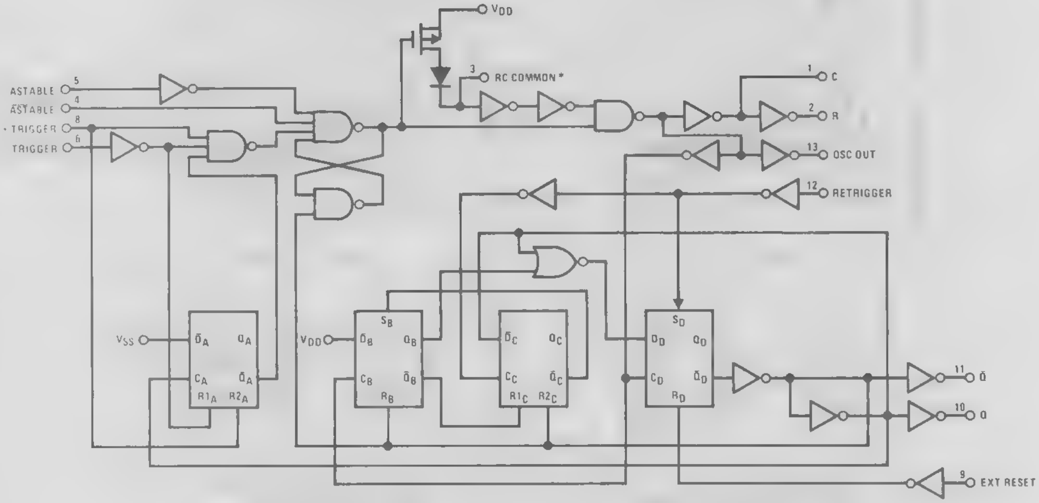
Note 2: $V_{SS} = 0V$ unless otherwise specified.

AC Electrical Characteristics CD4047B

$T_A = 25°C$, $C_L = 50\ pF$, $R_L = 200k$, Input $t_r = t_f = 20\ ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Astable, $\overline{\text{Astable}}$ to Osc Out	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
t_{PHL}, t_{PLH}	Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	$V_{DD} = 5V$		550	900	ns
		$V_{DD} = 10V$		250	500	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	+ Trigger, − Trigger to Q, $\overline{Q}$	$V_{DD} = 5V$		700	1200	ns
		$V_{DD} = 10V$		300	600	ns
		$V_{DD} = 15V$		240	480	ns
t_{PHL}, t_{PLH}	+ Trigger, Retrigger to Q, $\overline{Q}$	$V_{DD} = 5V$		300	600	ns
		$V_{DD} = 10V$		175	300	ns
		$V_{DD} = 15V$		150	250	ns
t_{PHL}, t_{PLH}	Reset to Q, $\overline{Q}$	$V_{DD} = 5V$		300	600	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q, $\overline{Q}$, Osc Out	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Duration	Any Input				
		$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{RCL}, t_{FCL}	+ Trigger, Retrigger, Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			5	μs
		$V_{DD} = 15V$			5	μs
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

Logic Diagram


V_{DD}
3 RC COMMON*
ASTABLE 5
ASTABLE 4
+TRIGGER 8
TRIGGER 6
1 C
2 R
13 OSC OUT
12 RETRIGGER
VSS
VDD
S_B
D_A Q_A C_A Q̄_A R1_A R2_A
D_B Q_B C_B Q̄_B R_B
D_C Q_C C_C Q̄_C R1_C R2_C
S_D D_D Q_D C_D Q̄_D R_D
11 Q̄
10 Q
9 EXT RESET

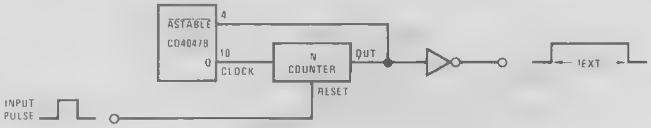
*Special input protection circuit to permit larger input-voltage swings

Truth Table

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	TYPICAL OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator					
Free-Running	4, 5, 6, 14	7, 8, 9, 12		10, 11, 13	$t_A(10, 11) = 4.40\ RC$
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A(13) = 2.20\ RC$
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	$t_M(10, 11) = 2.48\ RC$
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	(See Figure)	(See Figure)	(See Figure)

Note: External resistor between terminals 2 and 3. External capacitor between terminals 1 and 3.

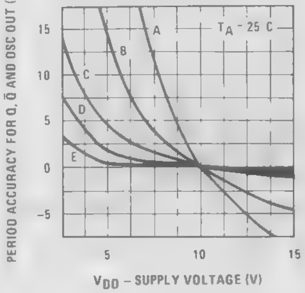
***Typical Implementation of External Countdown Option**



$$t_{EXT} = (N - 1)\ t_A + (t_M + t_A/2)$$

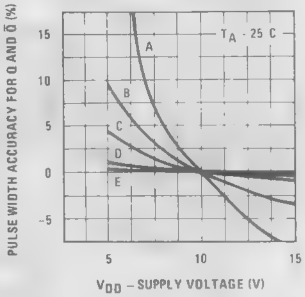
Typical Performance Characteristics

Typical Q, $\overline{Q}$, Osc Out Period Accuracy vs Supply Voltage (Astable Mode Operation)



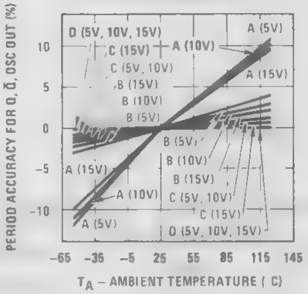
	$f_{Q, \overline{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF
E	100 Hz	2.2M	1000 pF

Typical Q, $\overline{Q}$, Pulse Width Accuracy vs Supply Voltage Monostable Mode Operation



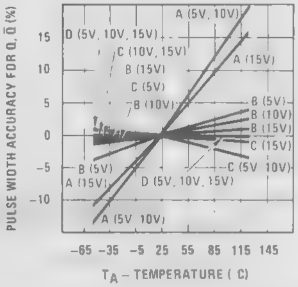
	t_M	R	C
A	2 µs	22k	10 pF
B	7 µs	22k	100 pF
C	60 µs	220k	100 pF
D	550 µs	220k	1000 pF
E	5.5 ms	2.2M	1000 pF

Typical Q, $\overline{Q}$ and Osc Out Period Accuracy vs Temperature Astable Mode Operation



	$f_{Q, \overline{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF

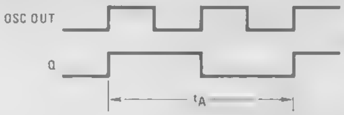
Typical Q and $\overline{Q}$ Pulse Width Accuracy vs Temperature Monostable Mode Operation



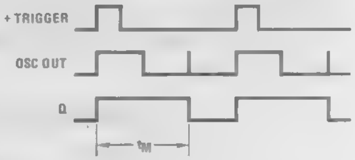
	t_M	R	C
A	2 µs	22k	10 pF
B	7 µs	22k	100 pF
C	60 µs	220k	100 pF
D	550 µs	220k	1000 pF

Timing Diagram

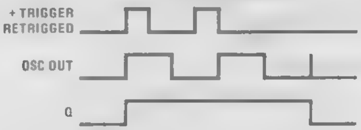
Astable Mode



Monostable Mode



Retrigger Mode



CD4048BM/CD4048BC TRI-STATE® Expandable 8-Function 8-Input Gate

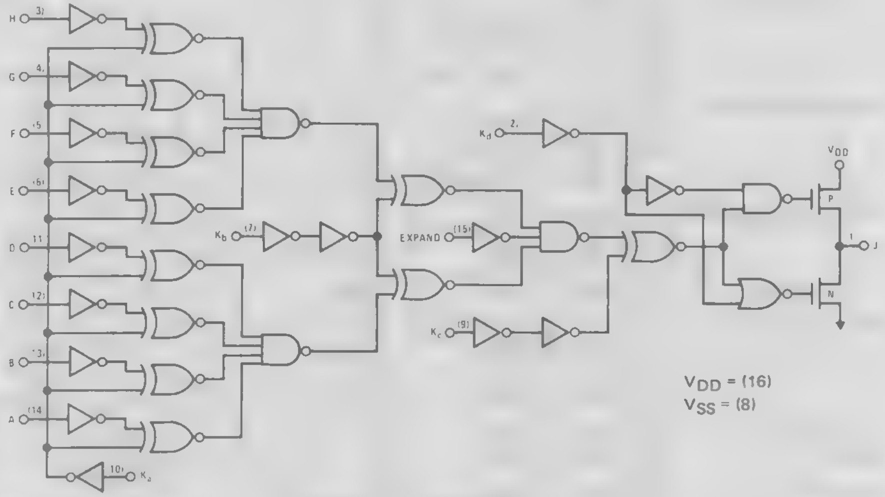
General Description

The CD4048BM/CD4048BC is a progammable 8-input gate. Three binary control lines K_a, K_b, and K_c determine the 8 different logic functions of the gate. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR. A fourth input, K_d, is a TRI-STATE control. When K_d is high, the output is enabled; when K_d is low, the output is a high impedance. This feature enables the user to connect the device to a common bus line. The Expand input permits the user to increase the number of gate inputs. For example, two 8-input CD4048's can be cascaded into a 16-input multi-function gate. When the Expand input is not used, it should be connected to V_{SS}. All inputs are buffered and protected against electrostatic effects.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- High sink and source current capability
- TTL compatibility drives 1 standard TTL load at V_{CC} = 5V, over full temperature range
- Many logic functions in one package

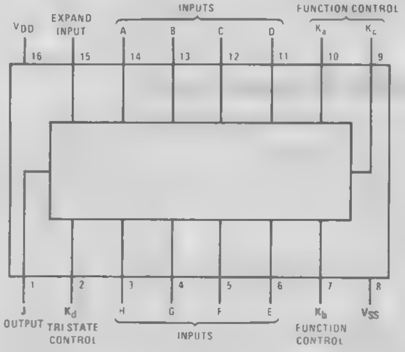
Logic Diagram



V_{DD} = (16)
V_{SS} = (8)

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4048BM	−55°C to +125°C
CD4048BC	−40°C to +85°C

DC Electrical Characteristics CD4048BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.01	5.0		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O\rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O\rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	2.8		2.3	4.0		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	6.4		5.2	11		3.6		mA
		V_{DD} = 15V, V_O = 1.5V	14		11.5	23		8.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−2.8		−2.3	4.0		−1.6		mA
		V_{DD} = 10V, V_O = 9.5V	−6.4		−5.2	11		−3.6		mA
		V_{DD} = 15V, V_O = 13.5V	14		−11.5	23		−8.0		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V, V_O = 0V		−0.2		−0.002	−0.2		−2	μA
		V_{DD} = 15V, V_O = 15V		0.2		0.002	0.2		2	μA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4048BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O\rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics (Cont'd.) CD4048BC (Note 2)

PARAMETER		CONDITIONS	40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	2.3		2.0	4.0			1.6	mA
		$V_{DD} = 10V$, $V_O = 0.5V$	5.2		4.5	11			3.6	mA
		$V_{DD} = 15V$, $V_O = 1.5V$	11.5		9.8	23			8.0	mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	2.3		2.0	-4.0			-1.6	mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-5.2		-4.5	-11			-3.6	mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-11.5		-9.8	-23			8.0	mA
I_{TL}	TRI-STATE Leakage Current	$V_{DD} = 15V$, $V_O = 0V$		-0.6		-0.005	-0.6		-2	μA
		$V_{DD} = 15V$, $V_O = 15V$		0.6		0.005	0.6		2	μA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		0.3		10^{-5}	-0.3		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, and $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		425	850	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, K_d to High Impedance (From Active Low or High Level)	$R_L = 1.0k\Omega$				
		$V_{DD} = 5V$		175	350	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		100	200	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, K_d to Active High or Low Level (From High Impedance)	$R_L = 1.0k\Omega$				
		$V_{DD} = 5V$		225	450	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{OUT}	Tristate output Capacitance				22.5	pF

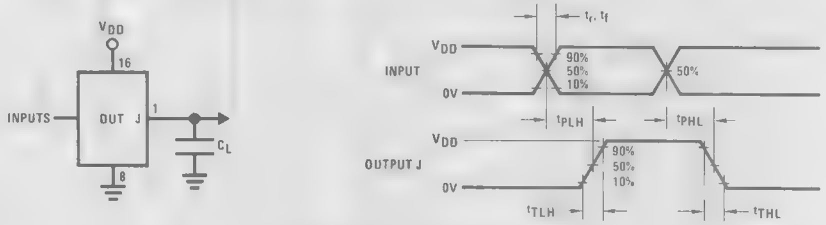
Truth Table

OUTPUT FUNCTION	BOOLEAN EXPRESSION	CONTROL INPUTS				UNUSED INPUTS
		K_a	K_b	K_c	K_d	
NOR	$J = \overline{A + B + C + D + E + F + G + H}$	0	0	0	1	V_{SS}
OR	$J = A + B + C + D + E + F + G + H$	0	0	1	1	V_{SS}
OR/AND	$J = (A + B + C + D) \cdot (E + F + G + H)$	0	1	0	1	V_{SS}
OR/NAND	$J = \overline{(A + B + C + D) \cdot (E + F + G + H)}$	0	1	1	1	V_{SS}
AND	$J = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$	1	0	1	1	V_{DD}
AND/NOR	$J = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$	1	1	0	1	V_{DD}
AND/OR	$J = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$	1	1	1	1	V_{DD}
Hi-Z		X	X	X	0	X

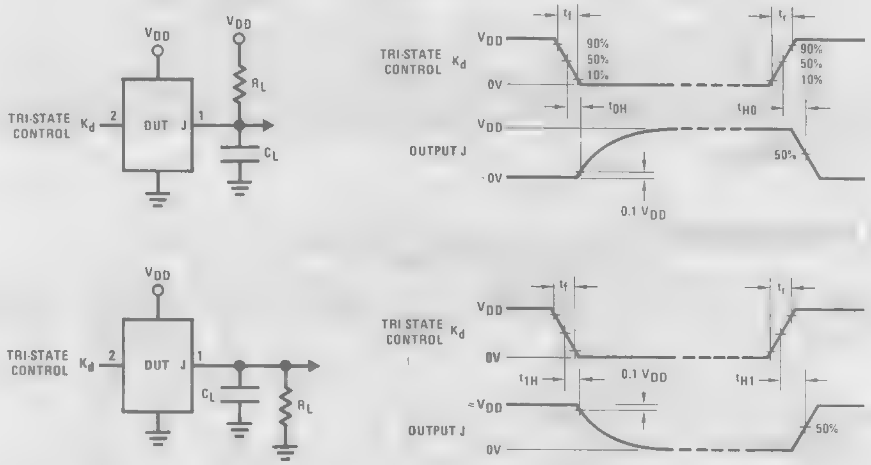
Positive logic: 0 = low level, 1 = high level, X = irrelevant, EXPAND input tied to V_{SS}.

AC Test Circuits and Switching Time Waveforms

Logic Propagation Delay Time Tests

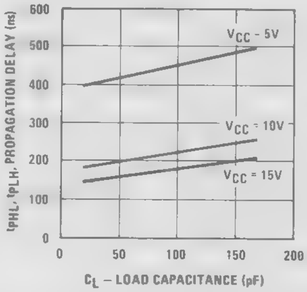


TRI-STATE Propagation Delay Time Tests

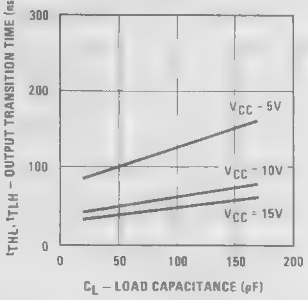


Typical Performance Characteristics

Propagation Delay vs Load Capactiance

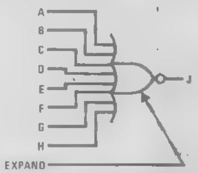


Output Transition Time vs Load Capacitance



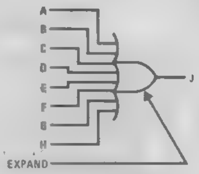
Basic Logic Configurations

NOR



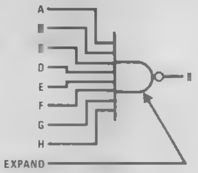
$K_aK_bK_c$ = 000

OR



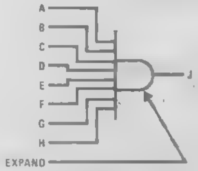
= 001

NAND



= 101

AND



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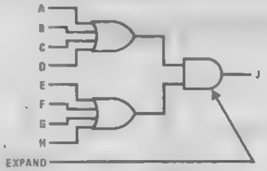
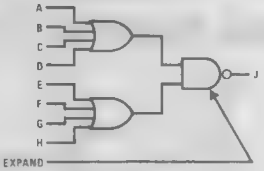
OR/AND



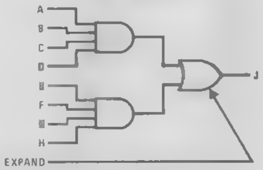
= 010

OR/NAND



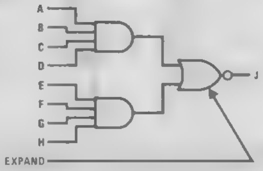
= 011

AND/OR



= 111

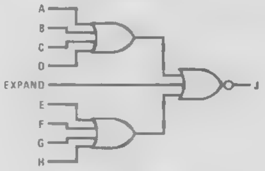
AND/NOR



= 110

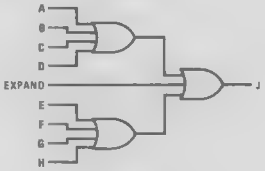
Actual Circuit Configurations

NOR



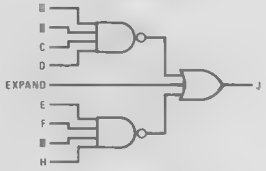
$K_aK_bK_c$ = 000

OR



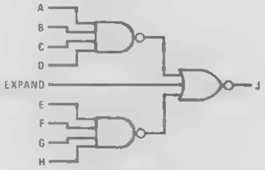
= 001

NAND



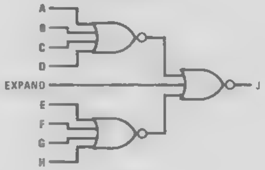
= 101

AND



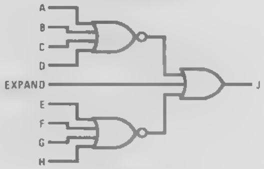
= 100

OR/AND



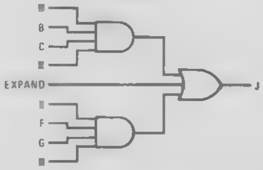
= 010

OR/NAND



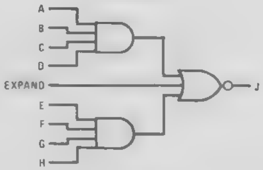
= 011

AND/OR



= 111

AND/NOR



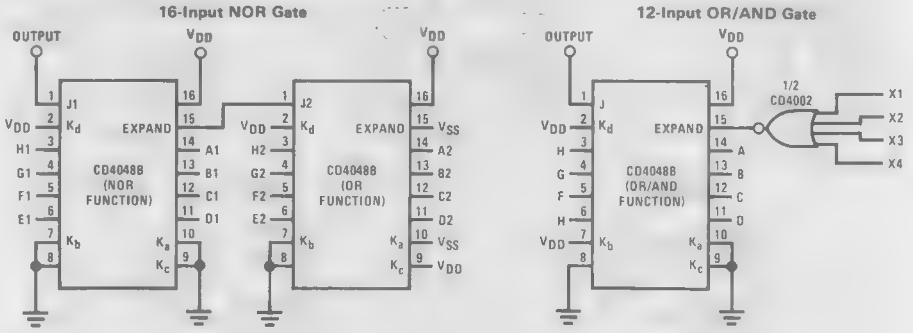
= 110

Truth Table for EXPAND Feature

COMBINED OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A + B + C + D + E + F + G + H) + (EXP)}$
OR	OR	$J = (A + B + C + D + E + F + G + H) + (EXP)$
AND	NAND	$J = (ABCDEFGH) \cdot (\overline{EXP})$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (\overline{EXP})}$
OR/AND	NOR	$J = (A + B + C + D) \cdot (E + F + G + H) \cdot (\overline{EXP})$
OR/NAND	NOR	$J = \overline{(A + B + C + D) \cdot (E + F + G + H) \cdot (\overline{EXP})}$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note. Positive logic is assumed. (EXP) represents the logic level present at the EXPAND input.

Typical Applications of EXPAND Feature



$$\text{Output} = \overline{A1 + B1 + C1 + D1 + E1 + F1 + G1 + H1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2}$$

Output = (A + B + C + D) • (E +
G + H) • (X1 + X2 + X3 + X4) F +

National Semiconductor

CD4049M/CD4049C Hex Inverting Buffer CD4050BM/CD4050BC Hex Non-Inverting Buffer

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at $V_{DD} = 5.0V$, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

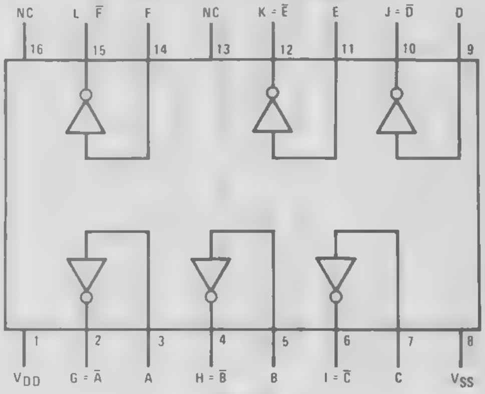
- Wide supply voltage range 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic level converter

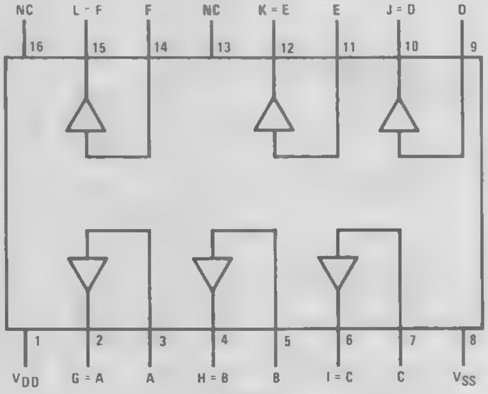
Connection Diagrams

CD4049M/CD4049C
Dual-In-Line and Flat Package



TOP VIEW

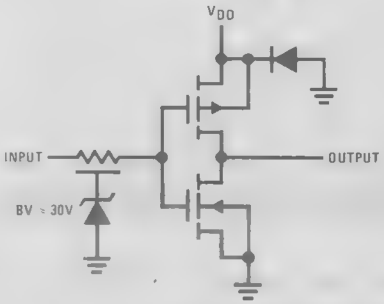
CD4050BM/CD4050BC
Dual-In-Line and Flat Package



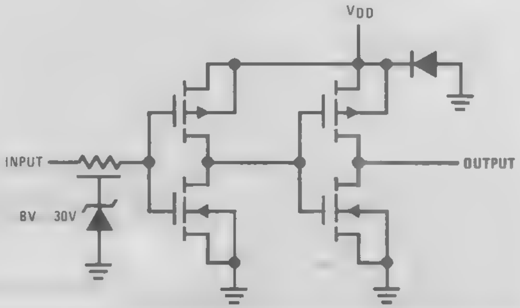
TOP VIEW

Schematic Diagrams

CD4049M/CD4049C
1 of 6 Identical Units



CD4050BM/CD4050BC
1 of 6 Identical Units



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to +18V
V_{OUT} Voltage at Any Output Pin	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to 15V
V_{OUT} Voltage at Any Output Pin	0 to V_{DD}
T_A Operating Temperature Range	
CD4049M, CD4050BM	−55°C to +125°C
CD4049C, CD4050BC	−40°C to +85°C

DC Electrical Characteristics CD4049M/CD4050BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	μA
		V_{DD} = 10V		2.0		0.01	2.0		60	μA
		V_{DD} = 15V		4.0		0.03	4.0		120	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BM Only)	$\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049M Only)	$\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BM Only)	$\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049M Only)	$\lvert I_O\rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	35		29	40		20		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−1.3		−1.1	1.6		−0.72		mA
		V_{DD} = 10V, V_O = 9.5V	−2.6		2.2	3.6		1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−8.0		7.2	12		5.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		0.1		10^{-5}	0.1		1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time.

DC Electrical Characteristics CD4049C/CD4050BC (Note 2)

PARAMETER	CONDITIONS	−40 C		25 C			85 C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		4		0.03	4.0		30	µA
	$V_{DD} = 10V$		8		0.05	8.0		60	µA
	$V_{DD} = 15V$		16		0.07	16.0		120	µA
V_{OL} Low Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0V$, $\lvert I_O \rvert < 1\,\mu A$								
	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0V$, $\lvert I_O \rvert < 1\,\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage (CD4050BC Only)	$\lvert I_O \rvert < 1\,\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V$, $V_O = 1V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V
V_{IL} Low Level Input Voltage (CD4049C Only)	$\lvert I_O \rvert < 1\,\mu A$								
	$V_{DD} = 5V$, $V_O = 4.5V$		1.0		1.5	1.0		1.0	V
	$V_{DD} = 10V$, $V_O = 9V$		2.0		2.5	2.0		2.0	V
	$V_{DD} = 15V$, $V_O = 13.5V$		3.0		3.5	3.0		3.0	V
V_{IH} High Level Input Voltage (CD4050BC Only)	$\lvert I_O \rvert < 1\,\mu A$								
	$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10V$, $V_O = 9V$	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	8.25		11.0		V
V_{IH} High Level Input Voltage (CD4049C Only)	$\lvert I_O \rvert < 1\,\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$	4.0		4.0	3.5		4.0		V
	$V_{DD} = 10V$, $V_O = 1V$	8.0		8.0	7.5		8.0		V
	$V_{DD} = 15V$, $V_O = 1.5V$	12.0		12.0	11.5		12.0		V
I_{OL} Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	$V_{DD} = 5V$, $V_O = 0.4V$	4.6		4.0	5		3.2		mA
	$V_{DD} = 10V$, $V_O = 0.5V$	9.8		8.5	12		6.8		mA
	$V_{DD} = 15V$, $V_O = 1.5V$	29		25	40		20		mA
I_{OH} High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	$V_{DD} = 5V$, $V_O = 4.6V$	−1.0		−0.9	1.6		−0.72		mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−2.1		1.9	−3.6		−1.5		mA
	$V_{DD} = 15V$, $V_O = 13.5V$	−7.1		−6.2	−12		5		mA
I_{IN} Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	0.3		0.3	-10^{-5}			1.0	µA
	$V_{DD} = 15V$, $V_{IN} = 15V$	0.3		0.3	10^{-5}			1.0	µA

AC Electrical Characteristics CD4049M/CD4049C

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified.

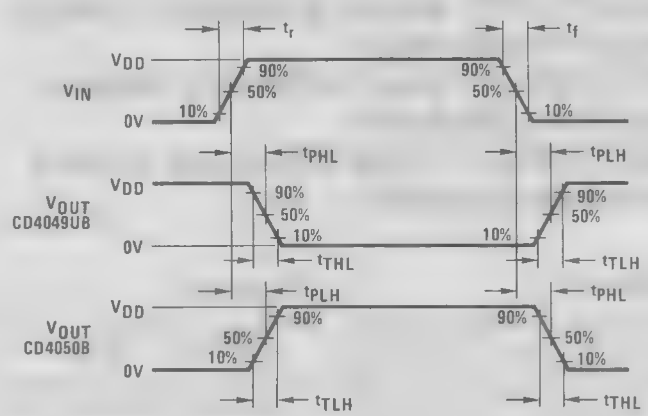
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		30	65	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		45	85	ns
		$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

AC Electrical Characteristics CD4050BM/CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified.

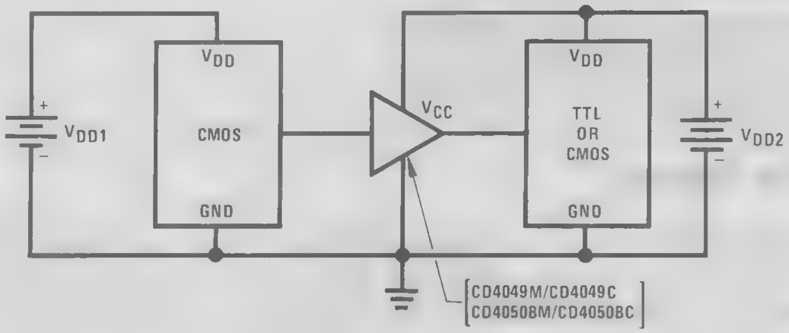
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		60	110	ns
		$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Switching Time Waveforms



Typical Applications

CMOS to TTL or CMOS at a Lower V_{DD}



Note: $V_{DD1} \geq V_{DD2}$

Note: In the case of the CD4049M/CD4049C the output drive capability increases with increasing input voltage. E.g., If V_{DD1} = 10V the CD4049M/CD4049C could drive 4 TTL loads.

National Semiconductor

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15 V_{p\text{-}p}$ can be achieved by digital signal amplitudes of 3-15 V. For example, if $V_{DD} = 5 V$, $V_{SS} = 0 V$ and $V_{EE} = -5 V$, analog signals from −5 V to +5 V can be controlled by digital inputs of 0-5 V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs. A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

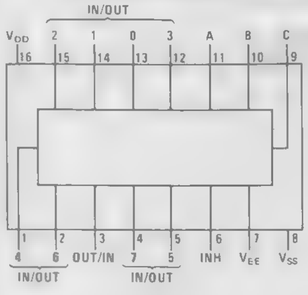
CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

- Wide range of digital and analog signal levels: digital 3-15 V, analog to $15 V_{p\text{-}p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15 V_{p\text{-}p}$ signal-input range for $V_{DD} - V_{EE} = 15 V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD} - V_{EE} = 10 V$
- Logic level conversion for digital addressing signals of 3-15 V ($V_{DD} - V_{SS} = 3\text{-}15 V$) to switch analog signals to $15 V_{p\text{-}p}$ ($V_{DD} - V_{EE} = 15 V$)
- Matched switch characteristics: $\Delta R_{ON} = 5\Omega$ (typ.) for $V_{DD} - V_{EE} = 15 V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10 V$
- Binary address decoding on chip

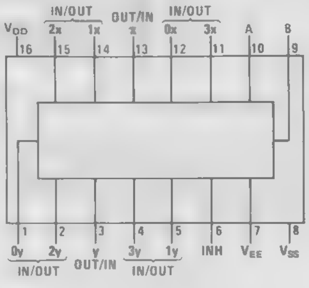
Connection Diagrams

CD4051BM/CD4051BC



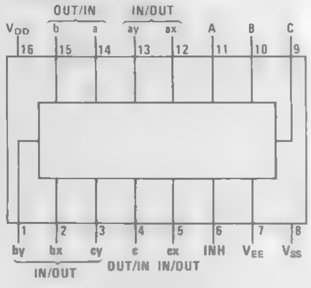
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

Absolute Maximum Ratings

V_{DD}	DC Supply Voltage	−0.5 Vdc to +18 Vdc
V_{IN}	Input Voltage	−0.5 Vdc to V_{DD} + 0.5 Vdc
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD}	DC Supply Voltage	+5 Vdc to +15 Vdc
V_{IN}	Input Voltage	0 V to V_{DD} Vdc
T_A	Operating Temperature Range	
	4051BM/4052BM/4053BM	−55°C to +125°C
	4051BC/4052BC/4053BC	−40°C to +85°C

DC Electrical Characteristics (Note 2)

	Parameter	Conditions		−55°C		+25°C			+125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V			5			5		150	μA
		V_{DD} = 10 V			10			20		600	μA
		V_{DD} = 15 V			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leqslant V_{IS} \leqslant V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V		2000		270	2500		3500	Ω
			V_{DD} = 5V V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V		310		120	400		580	Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V		220		80	280		400	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V				10				Ω
			V_{DD} = 5V, V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V				10				Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5V, V_{EE} = −7.5V O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V V_{DD} = 7.5V, V_{EE} = −7.5V, O/I = 0V, I/O = ±7.5V	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
			CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1kΩ to V_{SS} $I_{IS} < 2\mu A$ on all OFF channels V_{IS} = V_{DD} thru 1kΩ V_{DD} = 5V			1.5			1.5		1.5	V
		V_{DD} = 10V			3.0			3.0		3.0	V
		V_{DD} = 15V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15V, V_{EE} = 0V V_{IN} = 0V			−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{EE} = 0V V_{IN} = 15V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Cont'd.) (Note 2)

	Parameter	Conditions		−40°C		+25°C			+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$			20			20		150	µA
		$V_{DD} = 10V$			40			40		300	µA
		$V_{DD} = 15V$			80			80		600	µA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leqslant V_{IS} \leqslant V_{DD}$)	$R_L = 10\ k\Omega$ (any channel selected)	$V_{DD} = 2.5V$, $V_{EE} = -2.5V$ or $V_{DD} = 5V$, $V_{EE} = 0V$		2100		270	2500		3200	Ω
			$V_{DD} = 5V$, $V_{EE} = -5V$ or $V_{DD} = 10V$, $V_{EE} = 0V$		330		120	400		520	Ω
			$V_{DD} = 7.5V$, $V_{EE} = -7.5V$ or $V_{DD} = 15V$, $V_{EE} = 0V$		230		80	280		360	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	$R_L = 10\ k\Omega$ (any channel selected)	$V_{DD} = 2.5V$, $V_{EE} = -2.5V$ or $V_{DD} = 5V$, $V_{EE} = 0V$				10				Ω
			$V_{DD} = 5V$ $V_{EE} = -5V$ or $V_{DD} = 10V$, $V_{EE} = 0V$				10				Ω
			$V_{DD} = 7.5V$, $V_{EE} = -7.5V$ or $V_{DD} = 15V$, $V_{EE} = 0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD} = 7.5V$, $V_{EE} = -7.5V$ O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		$V_{DD} = 7.5V$, $V_{EE} = -7.5V$,	CD4052		±200		±0.04	±200		±2000	nA
		O/I = 0V I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE} = V_{SS}$ $R_L = 1\ k\Omega$ to V_{SS} $I_{IS} < 2\mu A$ on all OFF Channels $V_{IS} = V_{DD}$ thru 1kΩ									
		$V_{DD} = 5V$			1.5			1.5		1.5	V
		$V_{DD} = 10V$			3.0			3.0		3.0	V
		$V_{DD} = 15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5$		3.5		3.5			3.5		V
		$V_{DD} = 10$		7		7			7		V
		$V_{DD} = 15$		11		11			11		V
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{EE} = 0V$ $V_{IN} = 0V$			−0.1		-10^{-5}	−0.1		−1.0	µA
		$V_{DD} = 15V$, $V_{EE} = 0V$ $V_{IN} = 15V$			0.1		10^{-5}	0.1		1.0	µA

Note 1: "Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

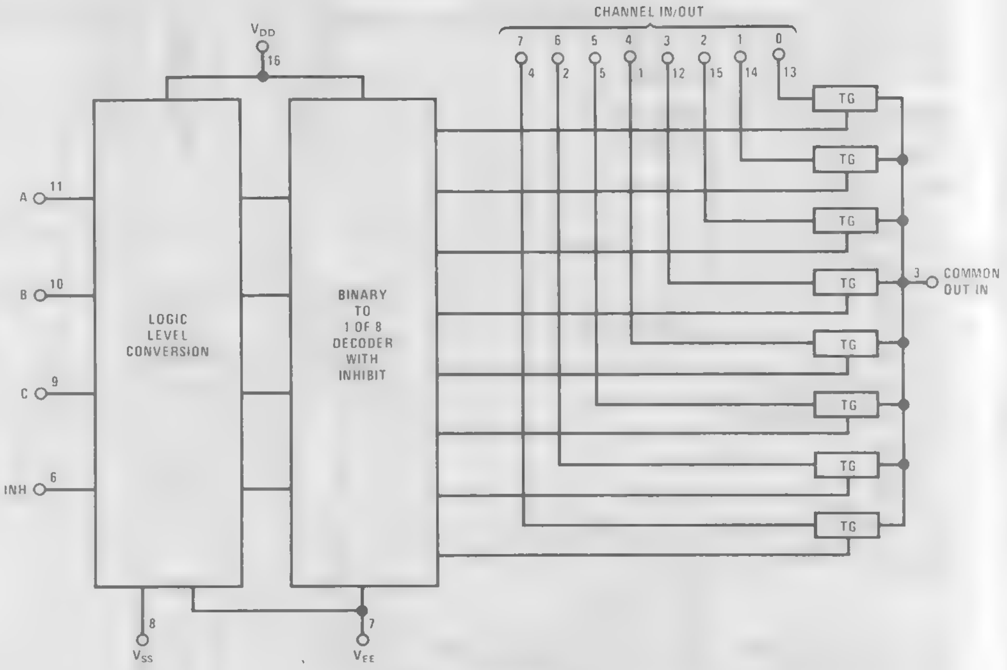
AC Electrical Characteristics

$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

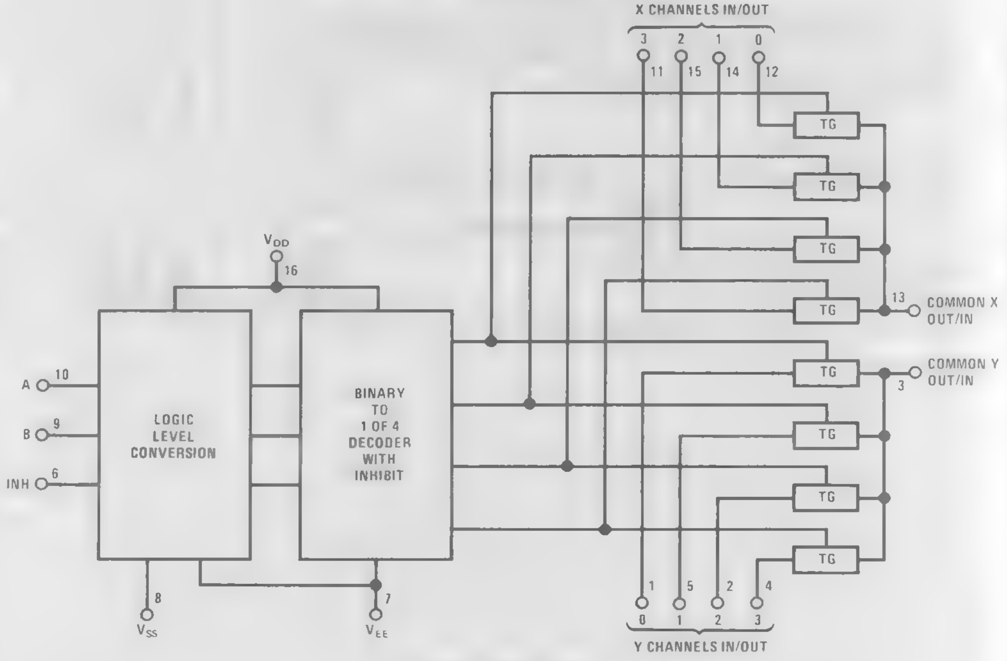
Parameter		Conditions	V_{DD}	Min	Typ	Max	Units
t_{PZH}, t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0V$	5V		600	1200	ns
		$R_L = 1\ k\Omega$	10V		225	450	ns
		$C_L = 50\ pF$	15V		160	320	ns
t_{PHZ} t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0V$	5V		210	420	ns
		$R_L = 1\ k\Omega$	10V		100	200	ns
		$C_L = 50\ pF$	15V		75	150	ns
C_{IN}	Input Capacitance						
	Control Input				5	7.5	pF
	Signal Input (IN/OUT)				10	15	pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051		10V		30		pF
	CD4052	$V_{EE} = V_{SS} = 0V$	10V		15		pF
	CD4053		10V		8		pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051				110		pF
	CD4052				140		pF
	CD4053				70		pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1\ kHz$ $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20\log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL}, t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$	5V		25	55	ns
		$C_L = 50\ pF$	10V		15	35	ns
			15V		10	25	ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$	5V		500	1000	ns
		$C_L = 50\ pF$	10V		180	360	ns
			15V		120	240	ns

Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

Block Diagrams

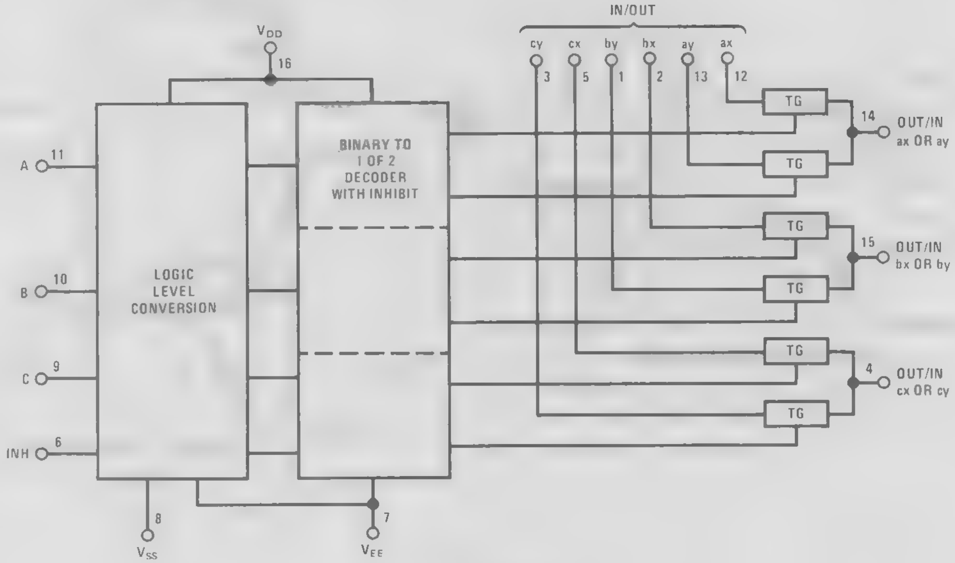


CD4051BM/CD4051BC



CD4052BM/CD4052BC

Block Diagrams (Cont'd.)



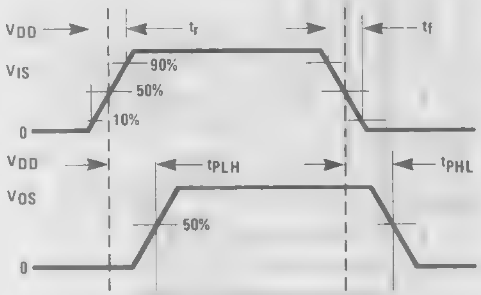
CD4053BM/CD4053BC

Truth Table

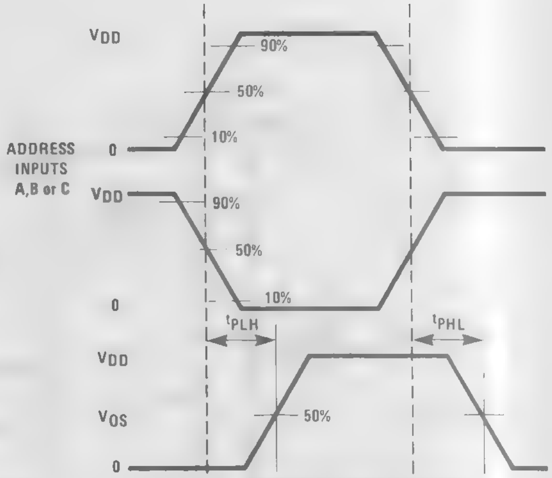
INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

*Don't Care condition

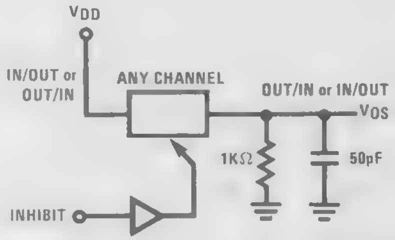
Switching Time Waveforms

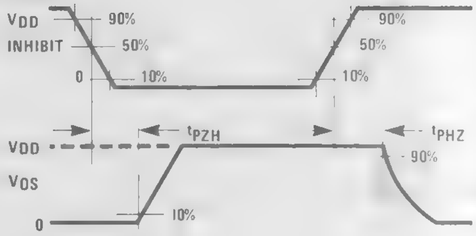


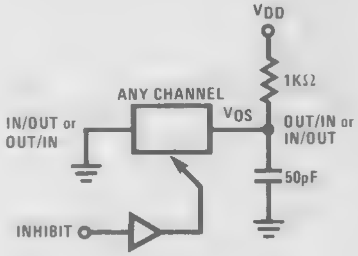
SIGNAL INPUT TO SIGNAL OUTPUT

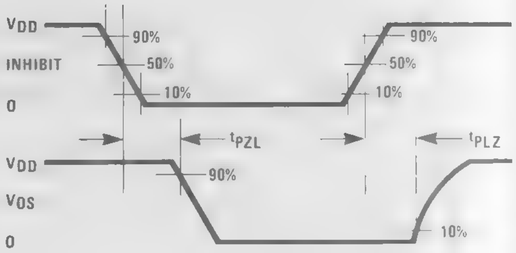


ADDRESS TO SIGNAL OUTPUT







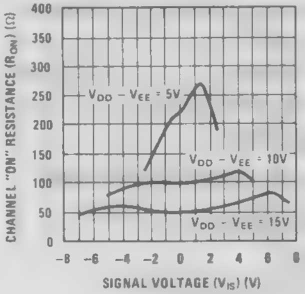


Special Considerations

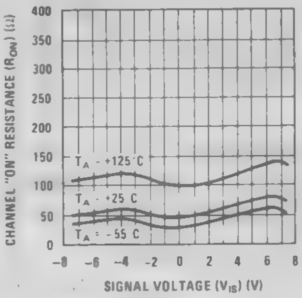
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6 V at $T_A \leqslant 25°C$, or 0.4 V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

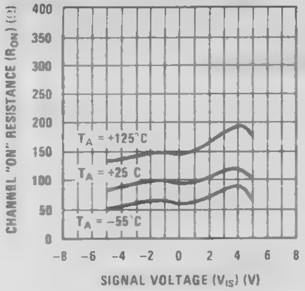
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



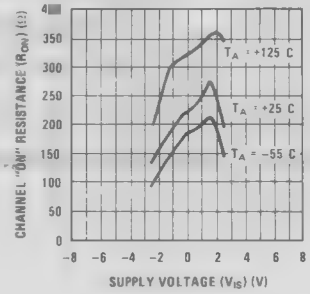
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

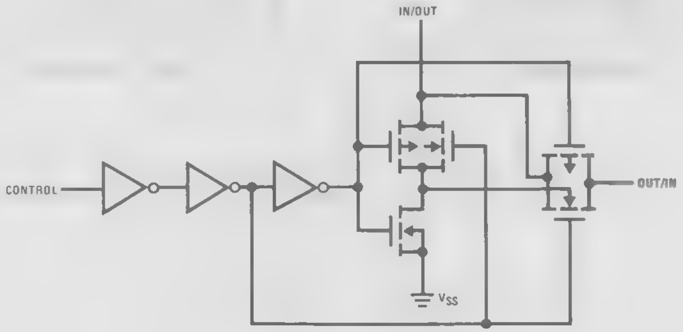
Features

■ Wide supply voltage range	3 V to 15 V
■ High noise immunity	$0.45\ V_{DD}$ (typ.)
■ Wide range of digital and analog switching	$\pm 7.5\ V_{PEAK}$
■ "ON" resistance for 15 V operation	80 Ω
■ Matched "ON" resistance over 15 V signal input	$\Delta R_{ON} = 5\ \Omega$ (typ.)
■ "ON" resistance flat over peak-to-peak signal range	
■ High "ON"/"OFF" output voltage ratio	65 dB (typ.) @ $f_{is} = 10\ kHz$, $R_L = 10\ k\Omega$
■ High degree linearity	0.1% distortion (typ.) @ $f_{is} = 1\ kHz$, $V_{is} = 5\ V_{p\text{-}p}$, $V_{DD} - V_{SS} = 10\ V$, $R_L = 10\ k\Omega$
■ Extremely low "OFF" switch leakage	0.1 nA (typ.) @ $V_{DD} - V_{SS} = 10\ V$, $T_A = 25°C$
■ Extremely high control input impedance	$10^{12}\ \Omega$ (typ.)
■ Low crosstalk between switches	−50 dB (typ.) @ $f_{is} = 0.9\ MHz$, $R_L = 1\ k\Omega$
■ Frequency response, switch "ON"	40 MHz (typ.)

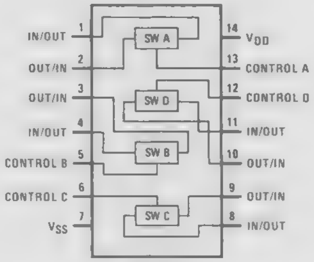
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	µA
		V_{DD} = 10V		0.5		0.01	0.5		15	µA
		V_{DD} = 15V		1.0		0.01	1.0		30	µA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		V_{DD} = 5V		2000		270	2500		3500	Ω
		V_{DD} = 10V		400		120	500		550	Ω
		V_{DD} = 15V		220		80	280		320	Ω
ΔR_{ON}	Δ "ON" Resistance Between any 2 of 4 Switches	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		V_{DD} = 10V				10				Ω
		V_{DD} = 15V				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	V_C = 0 V_{IS} = 15V and 0V, V_{OS} = 0V and 15V		±50		±0.1	±50		±500	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10\mu A$								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V (see note 6)	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} - V_{SS}$ = 15V $V_{DD} \geqslant V_{IS} \geqslant V_{SS}$ $V_{DD} \geqslant V_C \geqslant V_{SS}$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	µA

DC Electrical Characteristics CD4066BC (Note 2)

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	µA
		V_{DD} = 10V		2.0		0.01	2.0		15	µA
		V_{DD} = 15V		4.0		0.01	4.0		30	µA

DC Electrical Characteristics (Cont'd.) CD4066BC (Note 2)

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L = 10\,k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C = V_{DD}$, V_{SS} to V_{DD}								
		$V_{DD} = 5V$		2000		270	2500		3200	Ω
		$V_{DD} = 10V$		450		120	500		520	Ω
		$V_{DD} = 15V$		250		80	280		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\,k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		$V_{DD} = 10V$				10				Ω
		$V_{DD} = 15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C = 0$		±50		±0.1	±50		±200	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10\mu A$								
		$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$ (See note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} - V_{SS} = 15V$ $V_{DD} \geqslant V_{IS} \geqslant V_{SS}$ $V_{DD} \geqslant V_C \geqslant V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	µA

AC Electrical Characteristics $T_A = 25°C$, $t_r = t_f = 20\,ns$ and $V_{SS} = 0V$ unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50\,pF$, *(Figure 1)* $R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\,k\Omega$, $C_L = 50\,pF$, *(Figures 2 and 3)*				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$R_L = 1.0\,k\Omega$, $C_L = 50\,pF$, *(Figures 2 and 3)*				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$ $R_L = 10\,k\Omega$, $V_{IS} = 5\,V_{p-p}$, $f = 1\,kHz$, *(Figure 4)*		0.1		%
	Frequency Response-Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\,k\Omega$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{OS}(1kHz)$–dB, *(Figure 4)*		40		MHz

AC Electrical Characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20\,ns$ and $V_{SS} = 0\,V$ unless otherwise noted

	Parameter	Conditions	Min.	Typ.	Max.	Units
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5.0\,V$, $V_{CC} = V_{SS} = -5.0\,V$, $R_L = 1\,k\Omega$, $V_{IS} = 5.0\,V_{p\text{-}p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50\,dB$, *(Figure 4)*		1.25		
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5.0\,V$; $V_{SS} = V_{C(B)} = -5.0\,V$, $R_L = 1\,k\Omega$, $V_{IS(A)} = 5.0\,V_{p\text{-}p}$, 20 Log_{10}, $V_{OS(B)}/V_{IS(A)} = -50\,dB$, *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10\,V$, $R_L = 10\,k\Omega$, $R_{IN} = 1.0\,k\Omega$, $V_{CC} = 10\,V$ Square Wave, $C_L = 50\,pF$ *(Figure 6)*		150		$mV_{p\text{-}p}$
	Maximum Control Input	$R_L = 1.0\,k\Omega$, $C_L = 50\,pF$, *(Figure 7)* $V_{OS(f)} = ½V_{OS}(1.0\,kHz)$				
		$V_{DD} = 5.0\,V$		6.0		MHz
		$V_{DD} = 10\,V$		8.0		MHz
		$V_{DD} = 15\,V$		8.5		MHz
C_{is}	Signal Input Capactance			8.0		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10\,V$		8.0		pF
C_{ios}	Feedthrough Capacitance	$V_C = 0\,V$		0.5		pF
C_{IN}	Control Input Capacitance			5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\,V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}:
a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0\,V$, I_{OL} = standard B series I_{OL}.

AC Test Circuits and Switching Time Waveforms

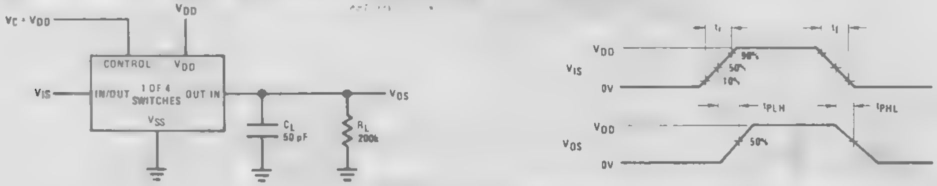


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

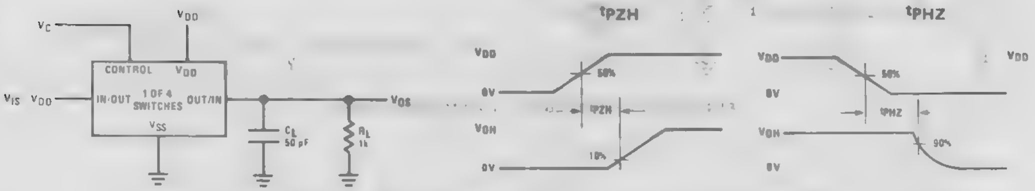


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

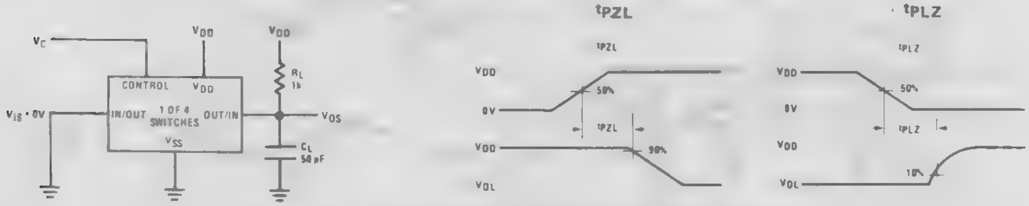
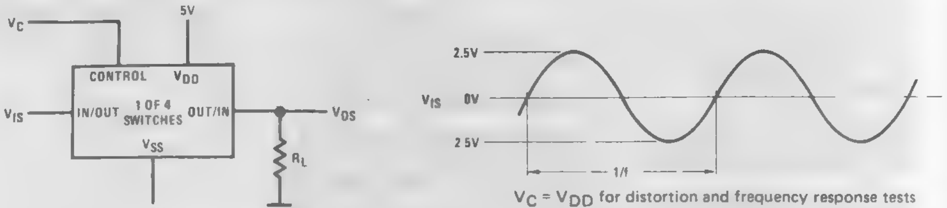


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Cont'd.)



$V_C = V_{DD}$ for distortion and frequency response tests

$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

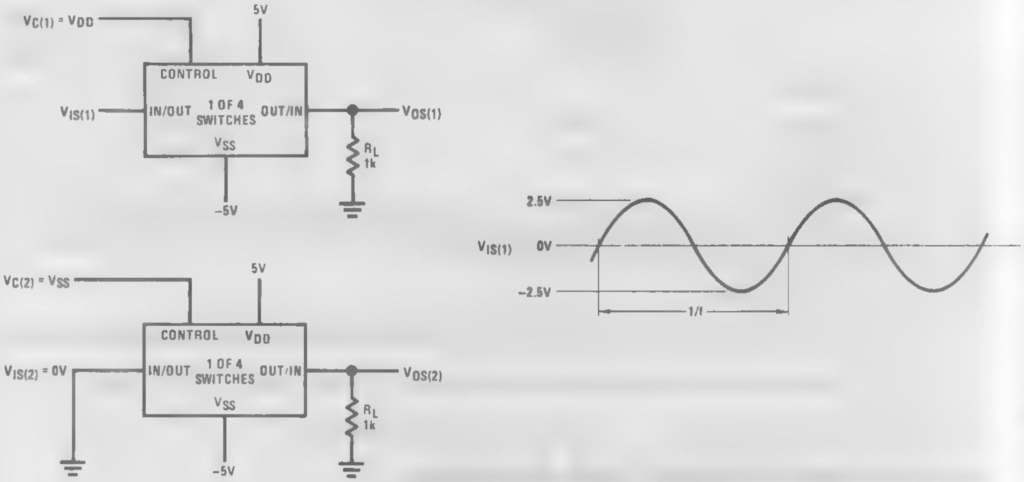


FIGURE 5. Crosstalk Between Any Two Switches

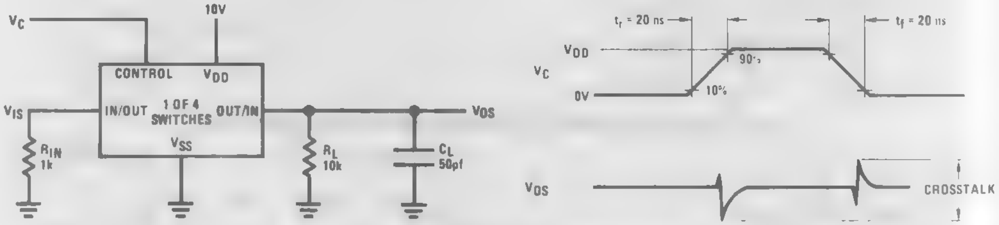


FIGURE 6. Crosstalk: Control Input to Signal Output

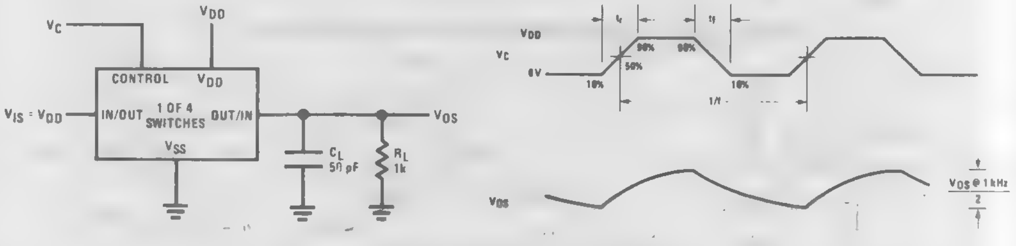
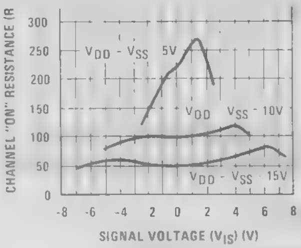
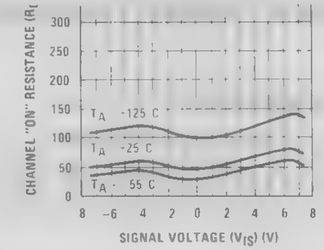
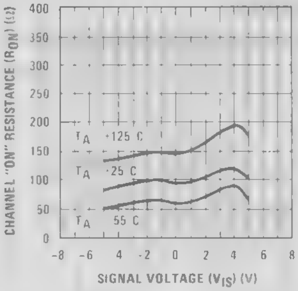


FIGURE 7. Maximum Control Input Frequency

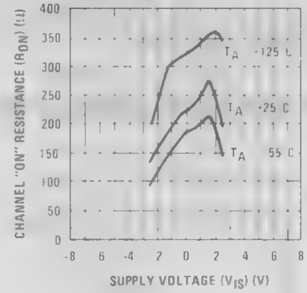




"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS}$ 5V



Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

National Semiconductor

CD4069M/CD4069C Inverter Circuits

General Description

The CD4069B consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

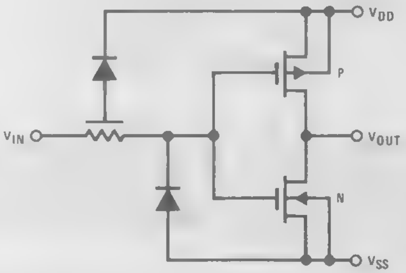
This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C903, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

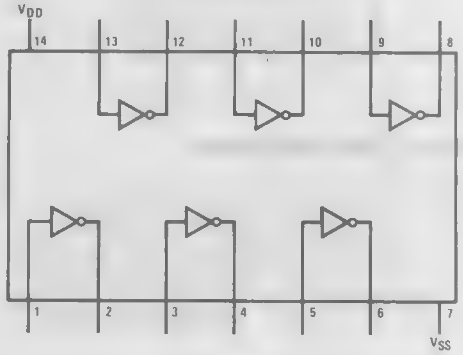
Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} typ.
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Equivalent to MM54C04/MM74C04	

Schematic and Connection Diagrams

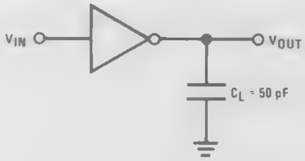


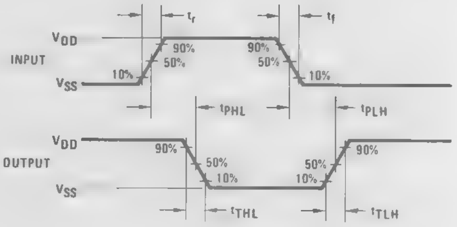
Dual-In-Line Package



TOP VIEW

AC Test Circuits and Switching Time Waveforms





$t_r = t_f = 20$ ns

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4069M	−55°C to +125°C
CD4069C	−40°C to +85°C

DC Electrical Characteristics

CD4069M (Note 2)

PARAMETER		CONDITIONS	-55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
		V_{DD} = 10V		0.5			0.5		15	μA
		V_{DD} = 15V		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4069C (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15	μA
		V_{DD} = 15V		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		8.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−8.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, t_r and $t_f \leqslant 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		50	90	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		80	150	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Gate		6	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 3)		12		pF

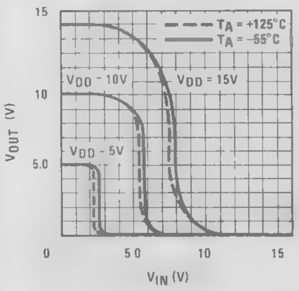
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

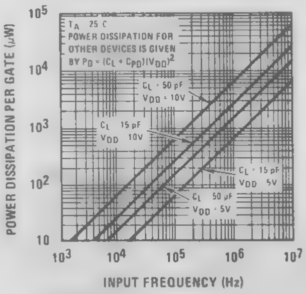
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

Typical Performance Characteristics

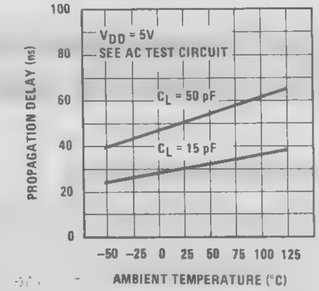
Gate Transfer Characteristics



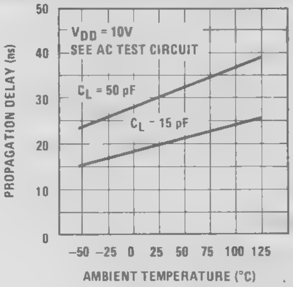
Power Dissipation vs Frequency



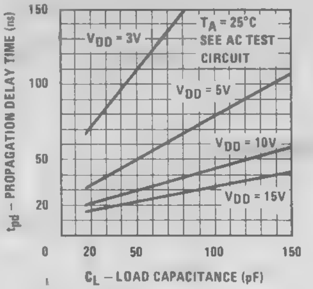
Propagation Delay vs Ambient Temperature



Propagation Delay vs Ambient Temperature



Propagation Delay Time vs Load Capacitance



National Semiconductor

CD4070BM/CD4070BC Quad 2-Input EXCLUSIVE-OR Gate

General Description

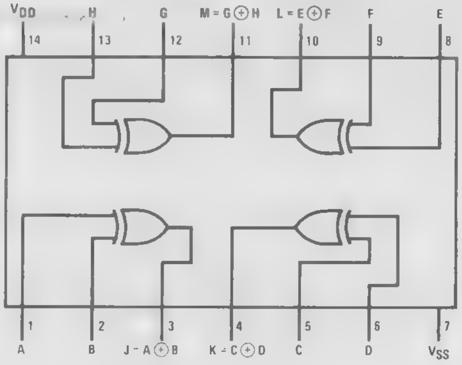
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption, and high noise margin, this gate provides basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} typ.
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Pin compatible to CD4030A
- Equivalent to MM54C86/MM74C86 and MC14507B

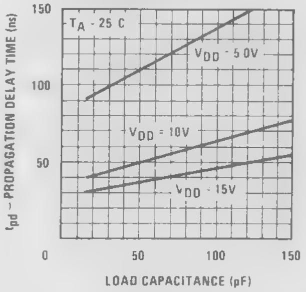
Connection Diagram

Dual-In-Line Package



Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance



Truth Table

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4070BC	−40°C to +85°C
CD4070BM	−55°C to +125°C

DC Electrical Characteristics CD4070BM (Note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		0.25			0.25		7.5	μA
	$V_{DD} = 10V$		0.5			0.5		15	μA
	$V_{DD} = 15V$		1.0			1.0		30	μA
V_{OL} Low Level Output Voltage	$\|I_O\| < 1\mu A$								
	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\|I_O\| < 1\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\mu A$								
	$V_{DD} = 5V, V_O = 4.5V$		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 9V$		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 13.5V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\mu A$								
	$V_{DD} = 5V, V_O = 0.5V$	3.5		3.5			3.5		V
	$V_{DD} = 10V, V_O = 1V$	7.0		7.0			7.0		V
	$V_{DD} = 15V, V_O = 1.5V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
	$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4070BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1.0			1.0		7.5	μA
		$V_{DD} = 10V$		2.0			2.0		15	μA
		$V_{DD} = 15V$		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	0.52		0.44	0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, t_r and $t_f \leq 20\,ns$, unless otherwise specified.

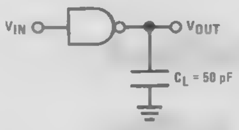
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	$V_{DD} = 5V$		110	185	ns
		$V_{DD} = 10V$		50	90	ns
		$V_{DD} = 15V$		40	75	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Input (Note 3)		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

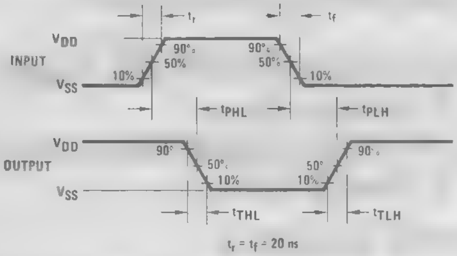
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

AC Test Circuit and Switching Time Waveforms



Note: Delays measured with input t_r, t_f = 20 ns.



National Semiconductor

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

General Description

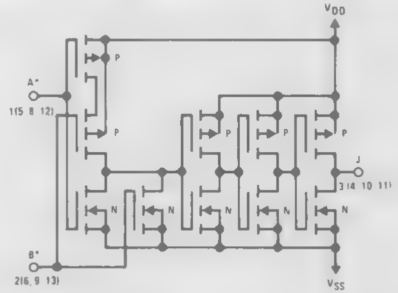
These quad gates are monolithic complementary MOS (CMOS) integrated circuits consructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

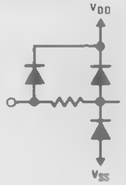
All inputs protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V–10–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Schematic and Connection Diagrams



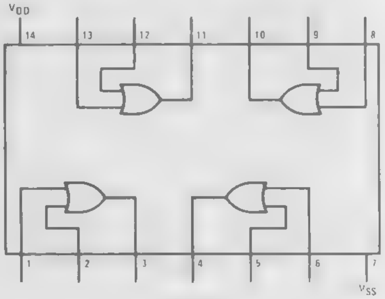


1/4 of device shown

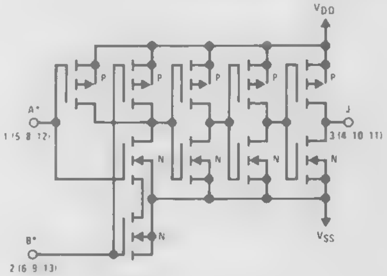
J = A + B
Logical "1" = High
Logical "0" = Low

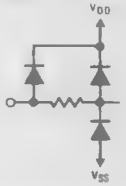
*All inputs protected by standard CMOS protection circuit

CD4071B
Dual-In-Line and Flat Package



TOP VIEW



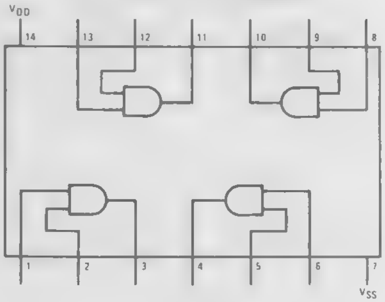


1/4 of device shown

J = A · B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4081B
Dual-In-Line and Flat Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

Voltage at Any Pin	$-0.5V$ to $V_{DD} + 0.5V$
Package Dissipation	500 mW
V_{DD} Range	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating V_{DD} Range	$3\ V_{DC}$ to $15\ V_{DC}$
Operating Temperature Range	
CD4071BM, CD4081BM	−55°C to +125°C
CD4071BC, CD4081BC	−40°C to +85°C

DC Electrical Characteristics — CD4071BM/CD4081BM (Note 2)

	PARAMETER	CONDITIONS	-55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$, $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$, $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$, $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$, $\|I_O\| < 1\mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$, $\|I_O\| < 1\mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$, $\|I_O\| < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		0.51	0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		1.3	2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	4.2		−3.4	8.8		2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		0.10		10^{5}	0.10		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.10		10^{5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics CD4071BC/CD4081BC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1		0.004	1		7.5	µA
		$V_{DD} = 10V$		2		0.005	2		15	µA
		$V_{DD} = 15V$		4		0.006	4		30	µA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	µA

AC Electrical Characteristics CD4071BC/CD4071BM

$T_A = 25°C$, Input t_r; $t_f = 20$ ns. $C_L = 50$ pF. R_L=200KΩ Typical temperature coefficient is 0.3%/°C

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	$V_{DD} = 5V$	100	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	$V_{DD} = 5V$	90	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$	90	200	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

AC Electrical Characteristics CD4081BC/CD4081BM

$T_A = 25°C$, Input t_r; t_f = 20 ns. C_L = 50 pF. R_L = 200K Typical temperature coefficient is 0.3%/°C

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

Typical Performance Characteristics

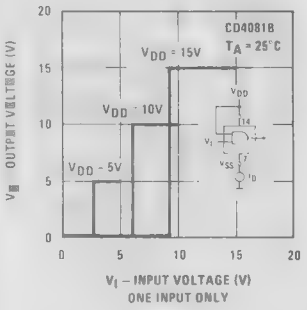


FIGURE 1. Typical Transfer Characteristics

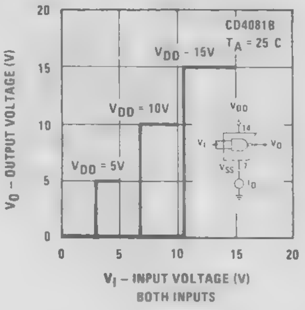


FIGURE 2. Typical Transfer Characteristics

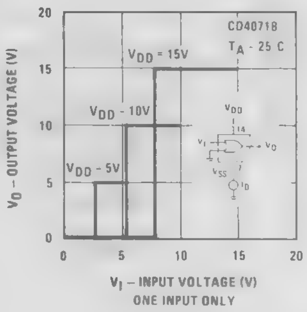


FIGURE 3. Typical Transfer Characteristics

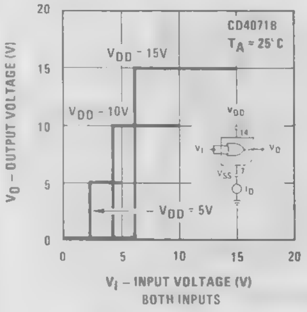


FIGURE 4. Typical Transfer Characteristics

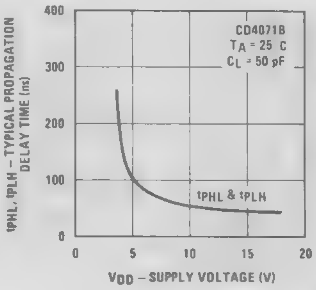


FIGURE 5

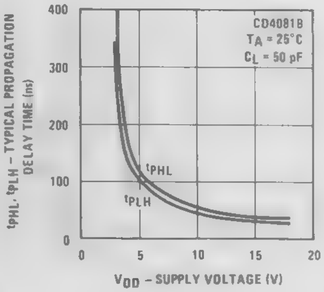


FIGURE 6

Typical Performance Characteristics (Cont'd.)

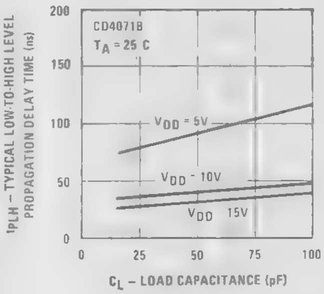


FIGURE 7

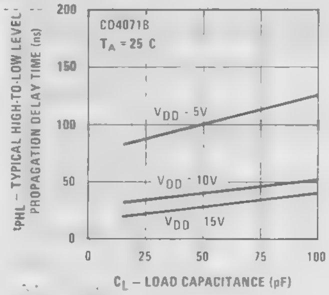


FIGURE 8

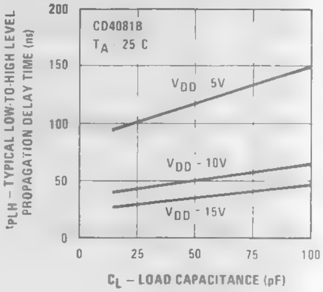


FIGURE 9

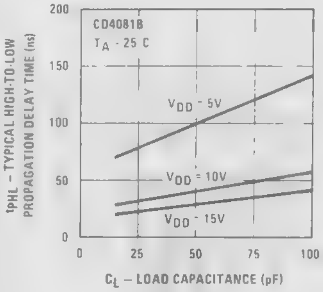


FIGURE 10

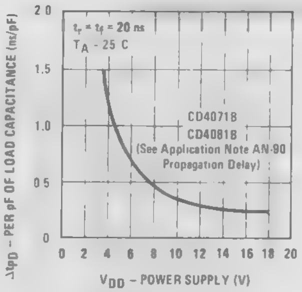


FIGURE 11

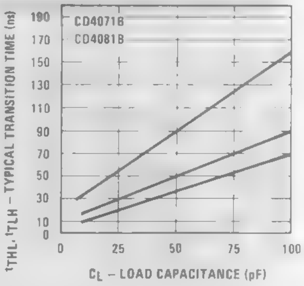


FIGURE 12

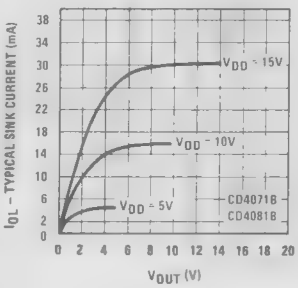


FIGURE 13

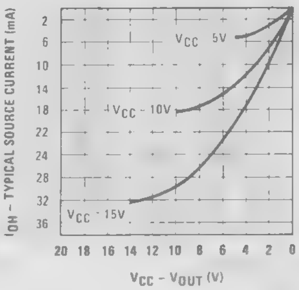


FIGURE 14

National Semiconductor

CD4072BM/CD4072BC Dual 4-Input OR Gate, CD4082BM/CD4082BC Dual 4-Input AND Gate

General Description

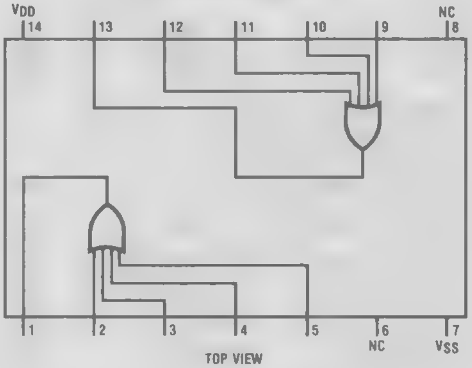
These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

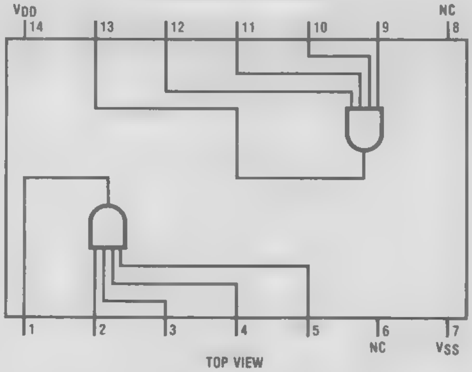
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fanout of 2 driving 74L or 1 driving 74LS
- 5V – 10V – 15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

CD4072BM/CD4072BC



CD4082BM/CD4082BC



Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 to V_{DD}0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD}	Supply Voltage	3.0 to 15 V
V_{IN}	Input Voltage	0 V to V_{DD} V
T_A	Operating Temperature Range	
	CD4072BM, CD4082BM	−55°C to +125°C
	CD4072BC, CD4082BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4072BM, CD4082BM

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD}=5.0\,V$		0.25		0.004	0.25		7.5	µA
	$V_{DD}=10\,V$		0.5		0.005	0.5		15	µA
	$V_{DD}=15\,V$		1.0		0.006	1.0		30	µA
V_{OL} Low Level Output Voltage	$V_{DD}=5.0\,V$		0.05		0	0.05		0.05	V
	$V_{DD}=10\,V$		0.05		0	0.05		0.05	V
	$V_{DD}=15\,V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD}=5.0\,V$	4.95		4.95	5.0		4.95		V
	$V_{DD}=10\,V$	9.95		9.95	10		9.95		V
	$V_{DD}=15\,V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD}=5.0\,V$, $V_O=0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
	$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$		3.0		4.50	3.0		3.0	V
	$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD}=5.0\,V$, $V_O=0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
	$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$	7.0		7.0	5.50		7.0		V
	$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	$V_{DD}=5.0\,V$, $V_O=0.4\,V$	0.64		0.51	0.88		0.36		mA
	$V_{DD}=10\,V$, $V_O=0.5\,V$	1.6		1.3	2.2		0.90		mA
	$V_{DD}=15\,V$, $V_O=1.5\,V$	4.2		3.4	8.0		2.4		mA
I_{OH} High Level Output Current	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.64		−0.51	−0.88		−0.36		mA
	$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.6		−1.3	−2.2		−0.90		mA
	$V_{DD}=15\,V$, $V_O=13.5\,V$	−4.2		−3.4	−8.0		−2.4		mA
I_{IN} Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.10		-10^{-5}	−0.10		−1.0	µA
	$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.10		10^{-5}	0.10		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0\,V$ unless otherwise specified.

DC Electrical Characteristics (Note 2) — CD4072BC, CD4082BC

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		1.0		0.004	1.0		7.5	μA
	V_{DD} = 10 V		2.0		0.005	2.0		15	μA
	V_{DD} = 15 V		4.0		0.006	4.0		30	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10		9.95		V
	V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.2		0.90		mA
	V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8.0		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.52		−0.44	−0.88		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1	−2.2		−0.90		mA
	V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0	−8.0		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.3		-10^{-5}	−0.3		−1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay, High to Low Level	V_{DD} = 5.0 V		125	250	ns
		V_{DD} = 10 V		60	100	ns
		V_{DD} = 15 V		45	70	ns
t_{PLH}	Propagation Delay, Low to High Level	V_{DD} = 5.0 V		125	250	ns
		V_{DD} = 10 V		60	100	ns
		V_{DD} = 15 V		45	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5.0 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns
C_{IN}	Average Input Capacitance (Note 3)	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 4)	Any Gate		20		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.

National Semiconductor

CD4073BM/CD4073BC Double Buffered Triple 3-Input AND Gate
CD4075BM/CD4075BC Double Buffered Triple 3-Input OR Gate

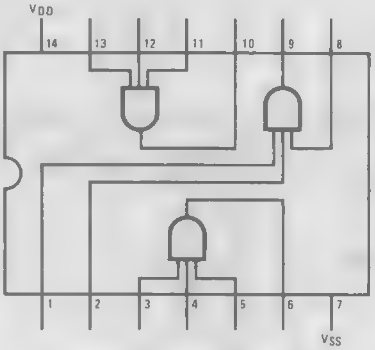
General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

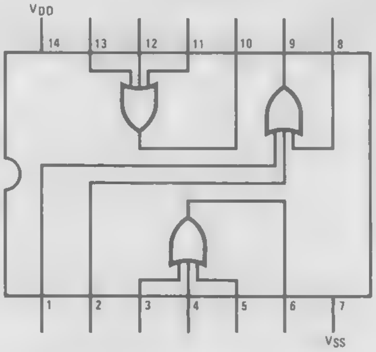
Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} typ.
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5 V - 10 V - 15 V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15 V over full temperature range

Connection Diagrams



CD4073 Triple 3-Input AND Gate
TOP VIEW



CD4075B Triple 3-Input OR Gate
TOP VIEW

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions (Note 2)

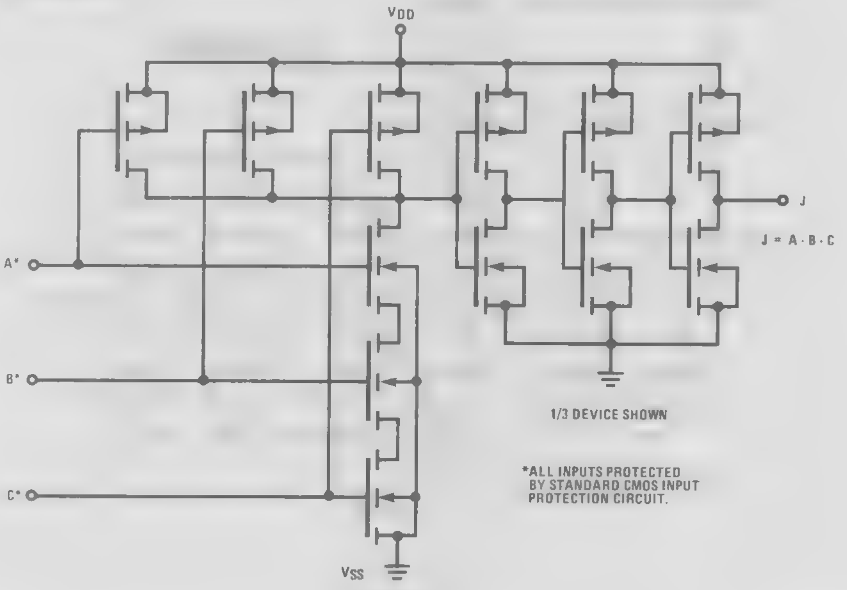
V_{DD}	DC Supply Voltage	$+5\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4073BM/CD4075BM	−55°C to +125°C
	CD4073BC/CD4075BC	−40°C to +85°C

DC Electrical Characteristics CD4073BM/CD4075BM (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5\ V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10\ V$		0.5		0.005	0.5		15	μA
		$V_{DD} = 15\ V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\ V$, $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\ V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15\ V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\ V$, $\|I_O\| < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10\ V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15\ V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$, $\|I_O\| < 1\ \mu A$		1.5		2	1.5		1.5	V
		$V_{DD} = 10\ V$, $V_O = 1.0\ V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15\ V$, $V_O = 1.5\ V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 4.5\ V$, $\|I_O\| < 1\ \mu A$	3.5		3.5	3		3.5		V
		$V_{DD} = 10\ V$, $V_O = 9.0\ V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15\ V$, $V_O = 13.5\ V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5\ V$, $V_O = 0.4\ V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\ V$, $V_O = 0.5\ V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15\ V$, $V_O = 1.5\ V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5\ V$, $V_O = 4.6\ V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10\ V$, $V_O = 9.5\ V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15\ V$, $V_O = 13.5\ V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\ V$, $V_{IN} = 0\ V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15\ V$, $V_{IN} = 15\ V$		0.10		10^{-5}	0.10		1.0	μA

Notes on following page.

Schematic Diagram



1/3 DEVICE SHOWN

*ALL INPUTS PROTECTED BY STANDARD CMOS INPUT PROTECTION CIRCUIT.

CD4073BC

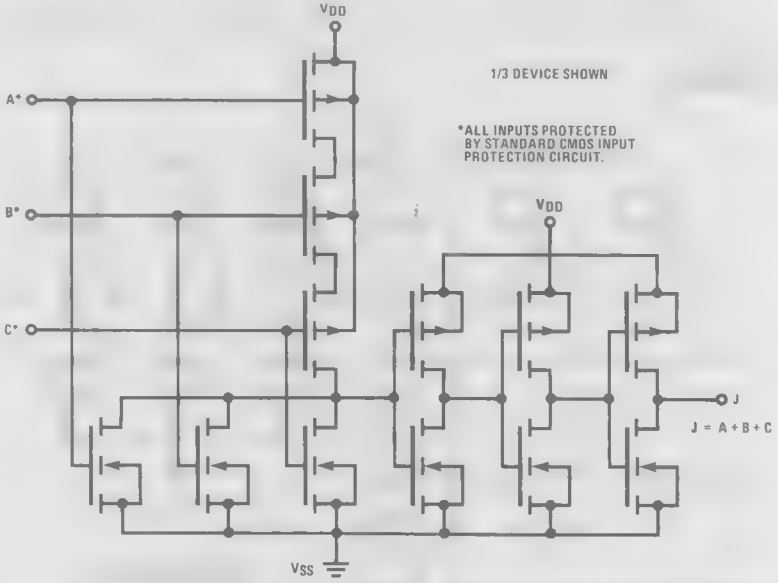
DC Electrical Characteristics CD4073BC/CD4075BC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5$ V		1		0.004	1		7.5	μA
		$V_{DD} = 10$ V		2		0.005	2		15	μA
		$V_{DD} = 15$ V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5$ V		0.05		0	0.05		0.05	V
		$V_{DD} = 10$ V, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15$ V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5$ V	4.95		4.95	5		4.95		V
		$V_{DD} = 10$ V, $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15$ V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5$ V, $V_O = 0.5$ V		1.5		2	1.5		1.5	V
		$V_{DD} = 10$ V, $V_O = 1.0$ V, $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		$V_{DD} = 15$ V, $V_O = 1.5$ V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5$ V, $V_O = 4.5$ V	3.5		3.5	3		3.5		V
		$V_{DD} = 10$ V, $V_O = 9.0$ V, $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		$V_{DD} = 15$ V, $V_O = 13.5$ V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5$ V, $V_O = 0.4$ V	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10$ V, $V_O = 0.5$ V	1.3		1.1	2.2		0.90		mA
		$V_{DD} = 15$ V, $V_O = 1.5$ V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5$ V, $V_O = 4.6$ V	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10$ V, $V_O = 9.5$ V	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD} = 15$ V, $V_O = 13.5$ V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15$ V, $V_{IN} = 0$ V		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD} = 15$ V, $V_{IN} = 15$ V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0$ V unless otherwise specified.

Schematic Diagram


VDD
A*
B*
C*
1/3 DEVICE SHOWN
*ALL INPUTS PROTECTED BY STANDARD CMOS INPUT PROTECTION CIRCUIT.
VDD
J
J = A + B + C
VSS

CD4075BC

AC Electrical Characteristics CD4073BM/CD4073BC/CD4075BM/CD4075BC

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$ unless otherwise specified.

PARAMETER		CONDITIONS	CD4073BC CD4073BM			CD4075BC CD4075BM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD} = 5\,V$		130	250		140	250	ns
		$V_{DD} = 10\,V$		60	100		70	100	ns
		$V_{DD} = 15\,V$		40	70		50	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD} = 5\,V$		140	250		130	250	ns
		$V_{DD} = 10\,V$		70	100		50	100	ns
		$V_{DD} = 15\,V$		50	70		40	70	ns
t_{THL} t_{TLH}	Transition Time	$V_{DD} = 5\,V$		90	200		90	200	ns
		$V_{DD} = 10\,V$		50	100		50	100	ns
		$V_{DD} = 15\,V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance (See Note 3)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (See Note 4)	Any Gate		17			17		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

National Semiconductor

CD4076BM/CD4076BC TRI-STATE® Quad D Flip-Flop

General Description

The CD4076BM/CD4076BC TRI-STATE quad D flip-flop is a monlithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. The four D type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disables allow the flip flops to remain in their present state without disrupting the clock. If either of the two input disables is taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

Clearing is enabled by taking the clear input to a logic "1" level. Clocking occurs on the positive-going transition.

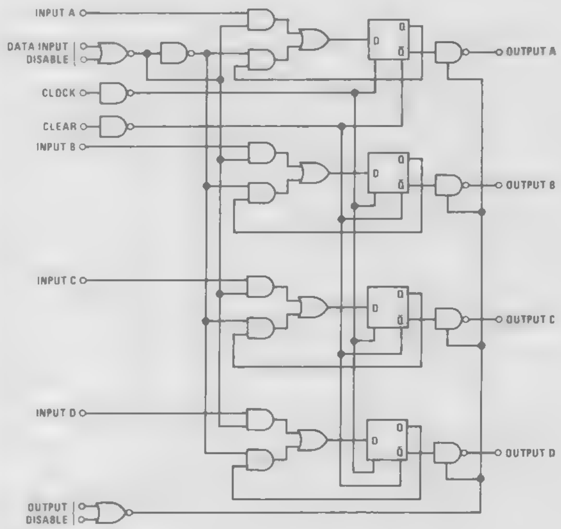
All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

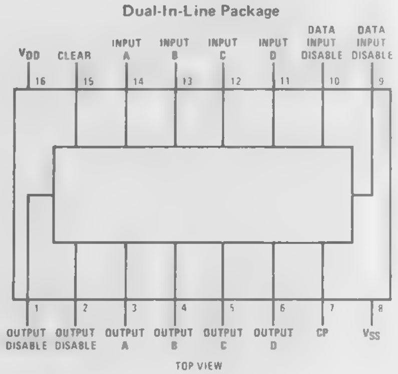
Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

- ■ High impedance TRI-STATE outputs
- ■ Inputs can be disabled without gating the clock
- ■ Equivalent to MM54C173/MM74C173

Logic and Connection Diagrams





Truth Table

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4076BM	−55°C to +125°C
CD4076BC	−40°C to +85°C

DC Electrical Characteristics CD4076BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4076BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA

DC Electrical Characteristics (Cont'd.) CD4076BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	Output Current in High Impedance State	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Output	$V_{DD} = 5V$		220	400	ns
		$V_{DD} = 10V$		80	200	ns
		$V_{DD} = 15V$		65	160	ns
t_{PHL}	Propagation Delay Time From Clear to Output	$V_{DD} = 5V$		240	490	ns
		$V_{DD} = 10V$		90	180	ns
		$V_{DD} = 15V$		70	145	ns
t_{SU}	Minimum Input Data Set-Up Time	$V_{DD} = 5V$		40	80	ns
		$V_{DD} = 10V$		15	30	ns
		$V_{DD} = 15V$		12	25	ns
t_H	Minimum Input Data Hold Time	$V_{DD} = 5V$		−40	0	ns
		$V_{DD} = 10V$		−12	0	ns
		$V_{DD} = 15V$		−10	0	ns
t_{SU}	Minimum Input Disable Set-Up Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		35	70	ns
		$V_{DD} = 15V$		28	55	ns
t_H	Minimum Input Disable Hold Time	$V_{DD} = 5V$		−75	0	ns
		$V_{DD} = 10V$		−30	0	ns
		$V_{DD} = 15V$		−25	0	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time From Output Disable to High Impedance State	$V_{DD} = 5V$, $R_L = 1.0k$		170	340	ns
		$V_{DD} = 10V$, R_L 1.0k		70	140	ns
		$V_{DD} = 15V$, R_L 1.0k		56	115	ns
t_{PZH}, t_{PZL}	Propagation Delay From Output Disable to Logical "1" Level or Logical "0" Level (From High Impedance State)	$V_{DD} = 5V$, $R_L = 1.0k$		170	340	ns
		$V_{DD} = 10V$, $R_L = 1.0k$		70	140	ns
		$V_{DD} = 15V$, $R_L = 1.0k$		56	115	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	3.0	4.0		MHz
		$V_{DD} = 10V$	7.0	12.0		MHz
		$V_{DD} = 15V$	8.75	15.0		MHz
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$		150		ns
		$V_{DD} = 10V$		70		ns
		$V_{DD} = 15V$		56		ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	10			μs
		$V_{DD} = 10V$	5			μs
		$V_{DD} = 15V$	2			μs
C_{IN}	Average Input Capacitance	Data Inputs (A, B, C, D)		3	7.5	pF
		Other Inputs		6	15	pF
C_{PD}	Power Dissipation Capacity	All Four Flip-Flops, (Note 3)		100		pF
C_{OUT}	TRI-STATE® Output Capacitance	Any Output			15	pF

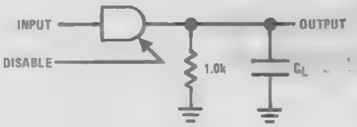
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

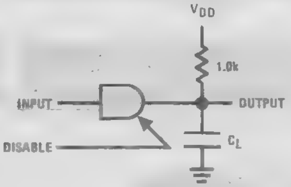
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN–90.

AC Test Circuits and Switching Time Waveforms

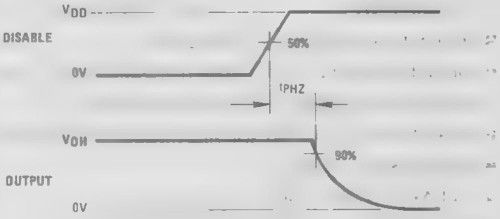
t_{PHZ} and t_{PZH}



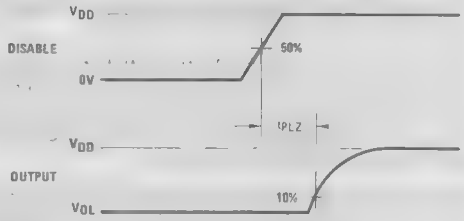
t_{PLZ} and t_{PZL}



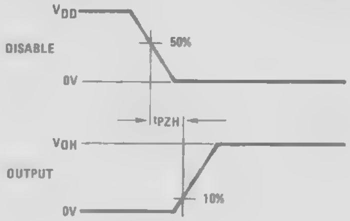
t_{PHZ}



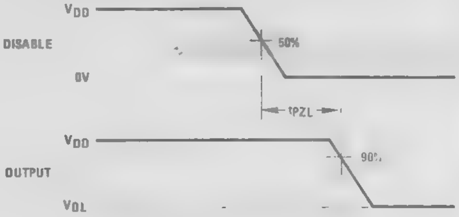
t_{PLZ}

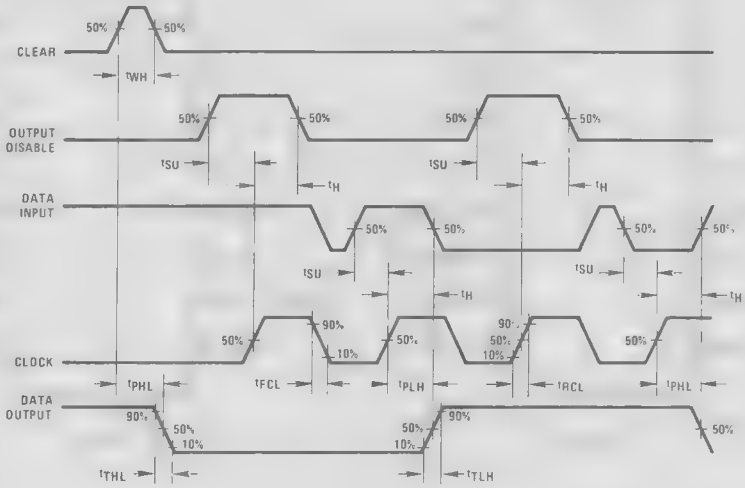


t_{PZH}



t_{PZL}





National Semiconductor

CD4089BM/CD4089BC Binary Rate Multiplier CD4527BM/CD4527BC BCD Rate Multiplier

General Description

The CD4089B is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $\frac{1}{16}$ times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

The CD4527B is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $\frac{1}{10}$ times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

These devices may be used to perform arithmetic operations including multiplication and division, A/D and D/A conversion and frequency division.

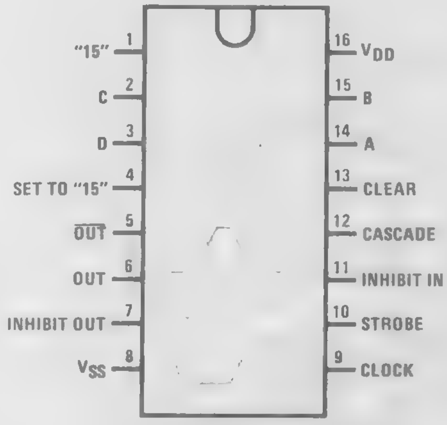
Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} typ.
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Internally synchronous 4-bit counter
- Output clocked on the negative-going edge of clock
- STROBE for inhibiting and enabling outputs
- INHIBIT IN and CASCADE inputs for cascade operation
- Complementary output
- CLEAR and SET inputs
- "9" or "15" output and INHIBIT OUT output

Connection Diagrams

CD4089B

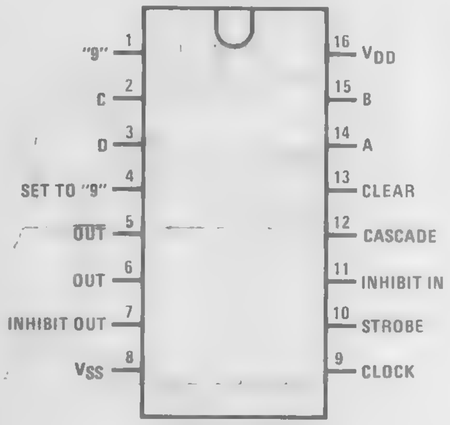
Dual-In-Line and Flat Package



TOP VIEW

CD4527B

Dual-In-Line and Flat Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15 V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4089BM, CD4527BM	−55°C to +125°C
CD4089BC, CD4527BC	−40°C to +85°C

DC Electrical Characteristics CD4089BM/CD4527BM (note 2)

PARAMETER		CONDITIONS	55 C		25 C			125 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4089BC/CD4527BC (Note 2)

PARAMETER		CONDITIONS	−40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics (Cont'd.) CD4089BC/CD4527BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to Out or $\overline{\text{Out}}$	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		60	120	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to E_{OUT}	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	240	ns
		V_{DD} = 15V		75	150	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to "9" or "15"	V_{DD} = 5V		280	560	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Set or Clear to Out or $\overline{\text{Out}}$	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Cascade to Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Strobe to Out	V_{DD} = 5V		220	440	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		65	130	ns
t_{TLH}, t_{THL}	Transition Time, All Outputs	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
$t_{W(CL)}$	Minimum Clock Pulse Width	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	2		MHz
		V_{DD} = 10V	2.5	5		MHz
		V_{DD} = 15V	3.5	7		MHz
t_r	Maximum Clock Rise Time	V_{DD} = 5V			5	μs
		V_{DD} = 10V			1.5	μs
		V_{DD} = 15V			1.0	μs
t_f	Maximum Clock Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
$t_{W(S,R)}$	Minimum Set or Clear Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		25	55	ns
t_{REM}	Set Removal Time	V_{DD} = 5V		−45	0	ns
		V_{DD} = 10V		−20	0	ns
		V_{DD} = 15V		−10	0	ns
$t_{SET\text{-}UP}$	Inhibit In Set-Up Time	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		45	90	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		80		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Truth Tables

CD4089B
Binary Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{\text{Out}}$	Pin 7 Inh Out	Pin 1 "15"
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

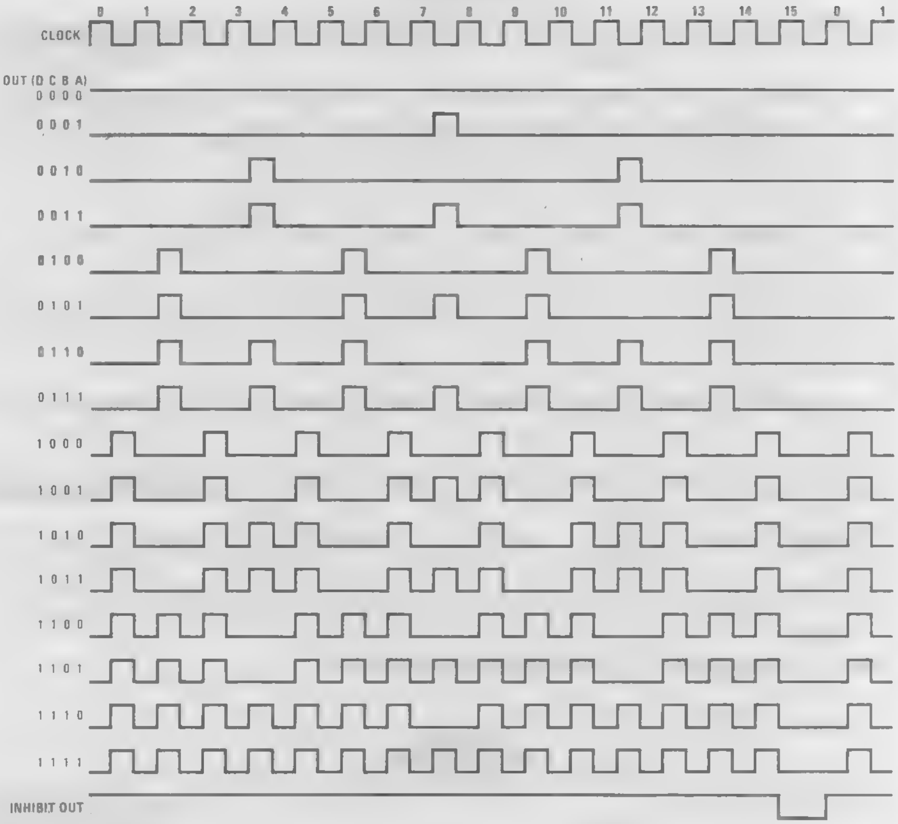
CD4527B
BCD Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{\text{Out}}$	Pin 7 Inh Out	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

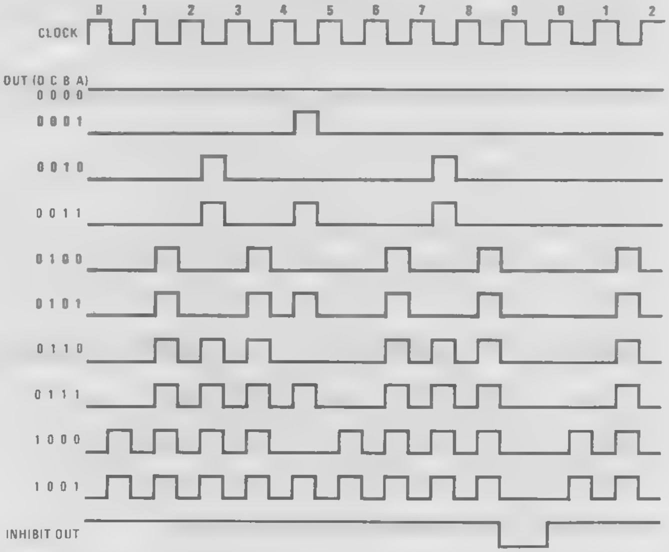
*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

Logic Waveforms

CD4089B
Binary Rate Multiplier

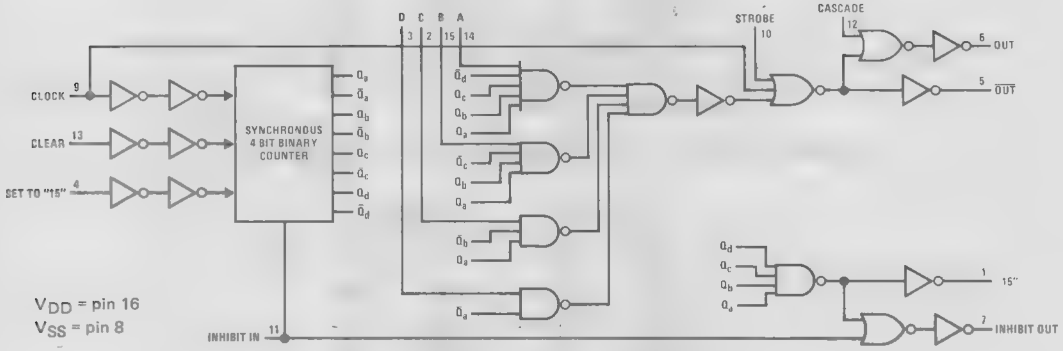


CD4527B
BCD Rate Multiplier



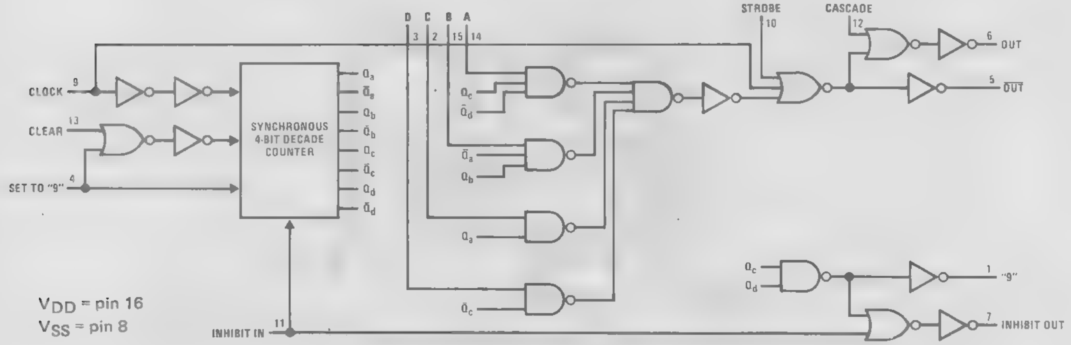
Logic Diagrams

CD4089B
Binary Rate Multiplier



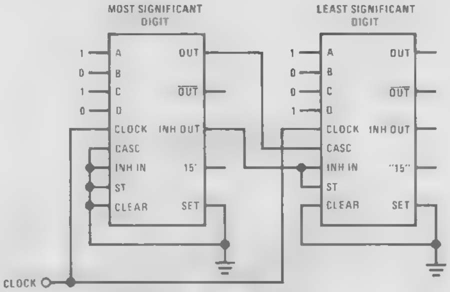
V_{DD} = pin 16
V_{SS} = pin 8

CD4527B
BCD Rate Multiplier

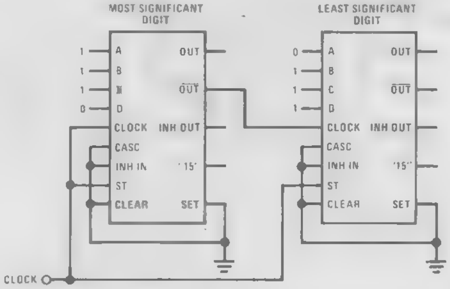


V_{DD} = pin 16
V_{SS} = pin 8

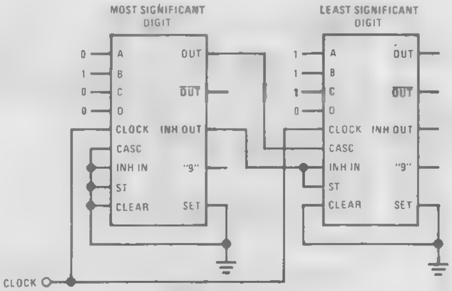
Cascading Packages



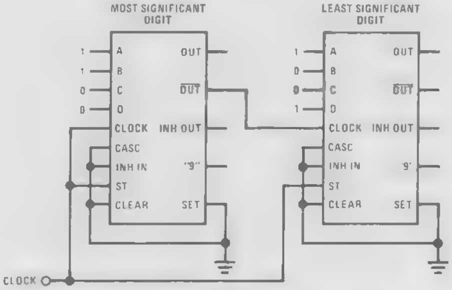
Two CD4089B's cascaded in the "add" mode with a preset number of 89 $\left(\frac{5}{16} + \frac{9}{256} = \frac{89}{256}\right)$



Two CD4089B's cascaded in the "multiply" mode with a preset number of 98 $\left(\frac{7}{16} \times \frac{14}{16} = \frac{98}{256}\right)$



Two CD4527B's cascaded in the "add" mode with a preset number of 27 $\left(\frac{2}{10} + \frac{7}{100} = \frac{27}{100}\right)$



Two CD4527B's cascaded in the "multiply" mode with a preset number of 27 $\left(\frac{3}{10} \times \frac{9}{10} = \frac{27}{100}\right)$

National Semiconductor

CD4093BM/CD4093BC Quad 2-Input NAND Schmitt Trigger

General Description

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive (V_T^+) and the negative voltage (V_T^-) is defined as hysteresis voltage (V_H).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

Features

- Wide supply voltage range 3.0 V to 15 V
- Schmitt-trigger on each input with no external components
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Standard B-series output drive
- Hysteresis voltage (any input) $T_A = 25°C$

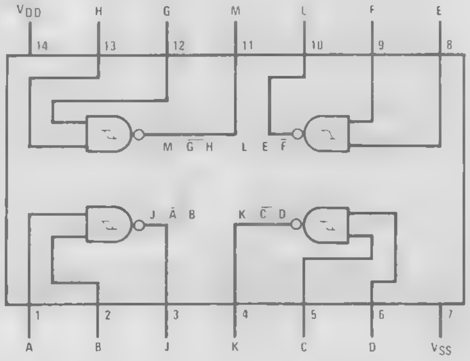
Typical	$V_{DD} = 5.0\,V$	$V_H = 1.5\,V$
	$V_{DD} = 10\,V$	$V_H = 2.2\,V$
	$V_{DD} = 15\,V$	$V_H = 2.7\,V$
Guaranteed		$V_H = 0.1\,V_{DD}$

Applications

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

Connection Diagram

Dual-In-Line Package



Absolute Maximum Ratings

(Notes 1 and 2)

DC Supply Voltage (V_{DD})	–0.5 to +18 V_{DC}
Input Voltage (V_{IN})	–0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	–65°C to +150°C
Package Dissipation (P_D)	500 mW
Lead Temperature (Soldering, 10 seconds) (T_L)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4093BM	–55°C to +125°C
CD4093BC	–40°C to +85°C

DC Electrical Characteristics CD4093BM (Note 2)

PARAMETER		CONDITIONS	–55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
		V_{DD} = 10V		0.5			0.5		15.0	μA
		V_{DD} = 15V		1.0			1.0		30.0	μA
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{DD}$, $\|I_O\| < 1 \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{SS}$, $\|I_O\| < 1 \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_T	Negative-Going Threshold Voltage	$\|I_O\| < 1 \mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage	$\|I_O\| < 1 \mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 0.5V	2.75	3.65	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	V_{DD} = 10V	1.0	4.30	1.0	2.2	4.0	0.70	4.0	V
	/	V_{DD} = 15V	1.5	6.30	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	$V_{IN} = V_{DD}$								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IN} = V_{SS}$								
		V_{DD} = 5V, V_O = 4.6V	0.64		0.51	-0.88		-0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.6		1.3	–2.25		–0.9		mA
		V_{DD} = 15V, V_O = 13.5V	–4.2		3.4	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		–0.1		10^{-5}	-0.1		1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics CD4093BC (Note 2)

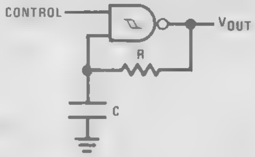
PARAMETER		CONDITIONS	40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15.0	μA
		V_{DD} = 15V		4.0			4.0		30.0	μA
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{DD}$, $\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{SS}$, $\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage (Any Input)	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.30	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage (Any Input)	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	2.75	3.6	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_{T+} - V_{T-}$) (Any Input)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
		V_{DD} = 10V	1.0	4.3	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.3	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	$V_{IN} = V_{DD}$								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IN} = V_{SS}$								
		V_{DD} = 5V, V_O = 4.6V	0.52		0.44	0.88		-0.36		mA
		V_{DD} = 10V, V_O = 9.5V	-1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 13.5V	-3.6		8.0	-8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		0.3		10^{-5}	0.3		-1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

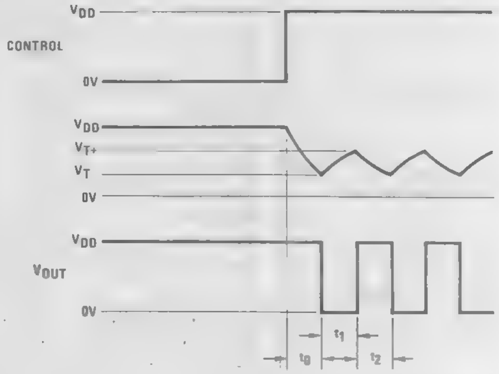
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, Input t_r, $t_f = 20\,ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	300	ns
		V_{DD} = 15V		80	240	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		90	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance			5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance			24		pF

Typical Applications

Gated Oscillator





Assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$ then:

$t_0 = RC \ln [V_{DD}/V_{T-}]$

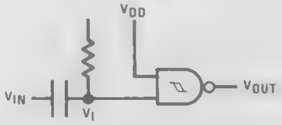
$t_1 = RC \ln [(V_{DD} - V_{T-})/(V_{DD} + V_{T+})]$

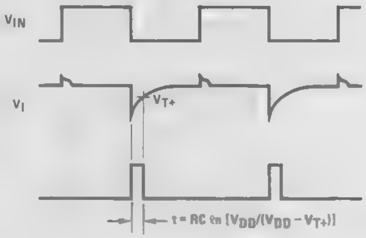
$t_2 = RC \ln [V_{T+}/V_{T-}]$

$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC \ln \dfrac{(V_{T+})(V_{DD} - V_{T-})}{(V_{T-})(V_{DD} - V_{T+})}}$$

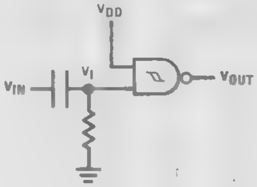
Gated One-Shot

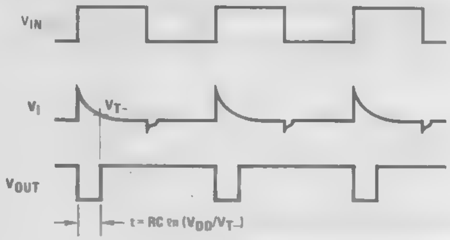
(a) Negative-Edge Triggered



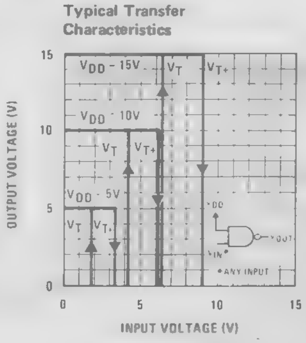


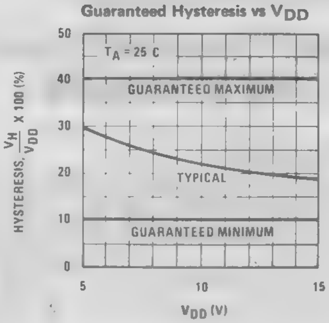
(b) Positive-Edge Triggered

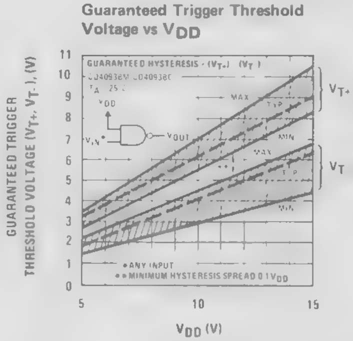


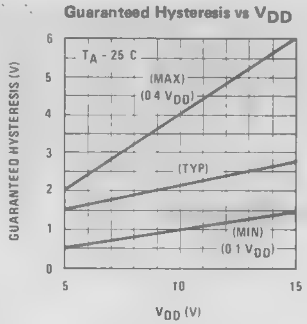


Typical Performance Characteristics

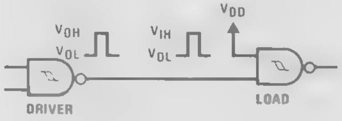

Typical Transfer Characteristics

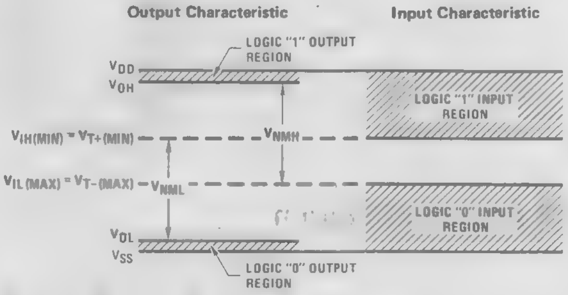

Guaranteed Hysteresis vs V_{DD}


Guaranteed Trigger Threshold Voltage vs V_{DD}


Guaranteed Hysteresis vs V_{DD}

Input and Output Characteristics



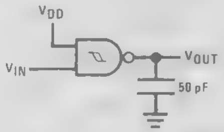

Output Characteristic

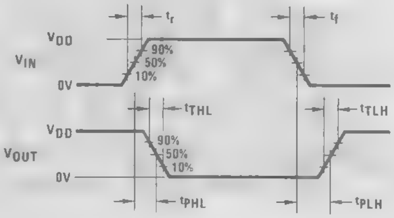
Input Characteristic

$$V_{NML} = V_{IH(MIN)} - V_{OL} \cong V_{IH(MIN)} = V_{T+(MIN)}$$

$$V_{NMH} = V_{OH} - V_{IL(MAX)} \cong V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T-(MAX)}$$

AC Test Circuits and Switching Time Waveforms





National Semiconductor

PRELIMINARY

CD4094BM/CD4094BC 8-Bit Shift Register/Latch with TRI-STATE® Outputs

General Description

The CD4094BM/CD4094BC consists of an 8-bit shift register and a TRI-STATE® 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

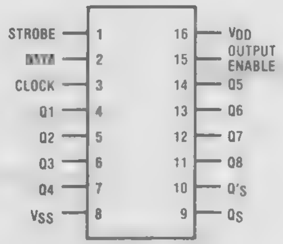
The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is high, data propagates through the latch to TRI-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken high.

TRI-STATE is a registered trademark of National Semiconductor Corp.

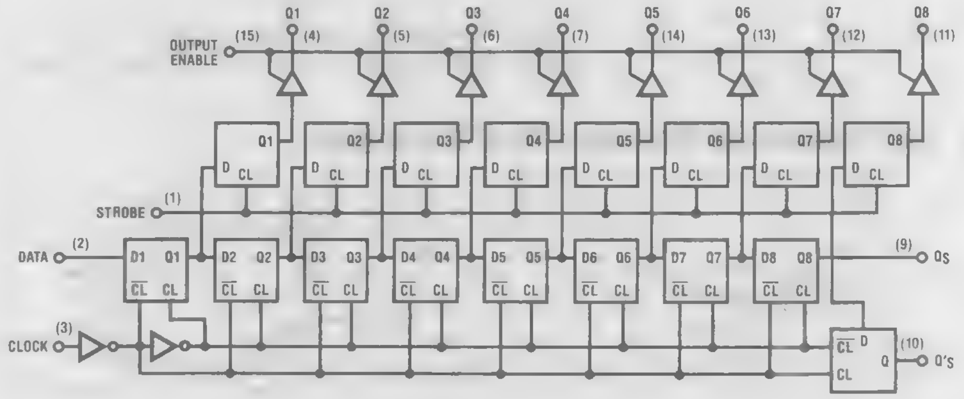
Features

■ Wide supply voltage range	3.0V to 18V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ TRI-STATE outputs	

Connection Diagram



Block or Logic Diagram



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	+3.0 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4094BM	−55°C to +125°C
CD4094BC	−40°C to +85°C

DC Electrical Characteristics CD4094BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0			5.0		150	µA
	V_{DD} = 10 V		10			10		300	µA
	V_{DD} = 15 V		20			20		600	µA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O\rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O\rvert \leq 1\,\mu A$	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	0.88		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	2.55		−0.9		mA
	V_{DD} = 15 V, V_O = 113.5 V	−4.2		−3.4	8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1			−0.1		−1.0	µA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1			0.1		1.0	µA

DC Electrical Characteristics CD4094BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20			20		150	µA
	V_{DD} = 10 V		40			40		300	µA
	V_{DD} = 15 V		80			80		600	µA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O\rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O\rvert \leq 1\,\mu A$	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.25		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics (cont'd) CD4094BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OH} High Level Output Current	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	0.88		−0.36		mA
	$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	2.55		−0.9		mA
	$V_{DD}=15\,V$, $V_O=113.5\,V$	−3.6		−3.0	8.8		−2.4		mA
I_{IN} Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.3			−0.3		−1.0	μA
	$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.3			0.3		1.0	μA

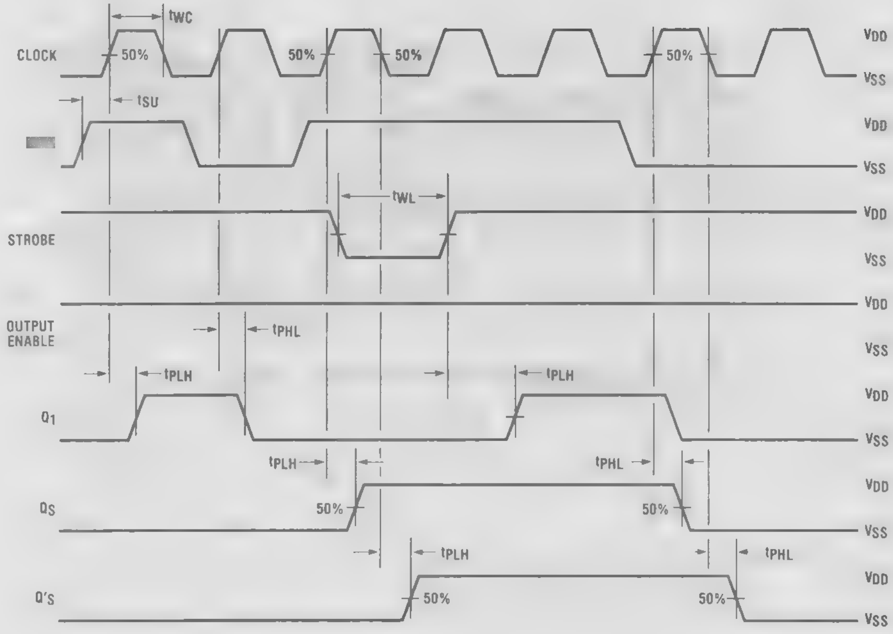
AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$

		Conditions	Min.	Typ.	Max.	Units
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q_S	$V_{DD}=5.0\,V$		300		ns
		$V_{DD}=10\,V$		125		ns
		$V_{DD}=15\,V$		95		ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q'_S	$V_{DD}=5.0\,V$		230		ns
		$V_{DD}=10\,V$		110		ns
		$V_{DD}=15\,V$		75		ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Parallel Out	$V_{DD}=5.0\,V$		420		ns
		$V_{DD}=10\,V$		195		ns
		$V_{DD}=15\,V$		135		ns
t_{PHL}, t_{PLH}	Propagation Delay Strobe to Parallel Out	$V_{DD}=5.0\,V$		290		ns
		$V_{DD}=10\,V$		145		ns
		$V_{DD}=15\,V$		100		ns
t_{PHZ}	Propagation Delay High Level to High Impedance	$V_{DD}=5.0\,V$		140		ns
		$V_{DD}=10\,V$		75		ns
		$V_{DD}=15\,V$		55		ns
t_{PLZ}	Propagation Delay Low Level to High Impedance	$V_{DD}=5.0\,V$		225		ns
		$V_{DD}=10\,V$		95		ns
		$V_{DD}=15\,V$		70		ns
t_{PZH}	Propagation Delay High Impedance to High Level	$V_{DD}=5.0\,V$		225		ns
		$V_{DD}=10\,V$		95		ns
		$V_{DD}=15\,V$		70		ns
t_{PZL}	Propagation Delay High Impedance to Low Level	$V_{DD}=5.0\,V$		140		ns
		$V_{DD}=10\,V$		75		ns
		$V_{DD}=15\,V$		55		ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0\,V$		100		ns
		$V_{DD}=10\,V$		50		ns
		$V_{DD}=15\,V$		40		ns
t_{SU}	Set-up Time Data to Clock	$V_{DD}=5.0\,V$		60		ns
		$V_{DD}=10\,V$		30		ns
		$V_{DD}=15\,V$		20		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{DD}=5.0\,V$	15			μs
		$V_{DD}=10\,V$	5.0			μs
		$V_{DD}=15\,V$	5.0			μs
t_{PC}	Minimum Clock Pulse Width	$V_{DD}=5.0\,V$		100		ns
		$V_{DD}=10\,V$		50		ns
		$V_{DD}=15\,V$		40		ns
t_{PS}	Minimum Strobe Pulse Width	$V_{DD}=5.0\,V$		100		ns
		$V_{DD}=10\,V$		40		ns
		$V_{DD}=15\,V$		35		ns
f_{MAX}	Maximum Clock Frequency	$V_{DD}=5.0\,V$		2.5		MHz
		$V_{DD}=10\,V$		5.0		MHz
		$V_{DD}=15\,V$		6.0		MHz
C_{IN}	Input Capacitance	Any Input		5.0		pF

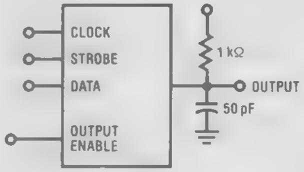
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0\,V$ unless otherwise specified.

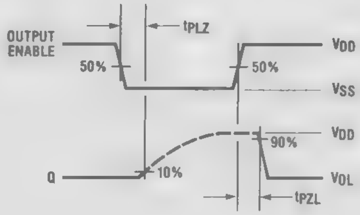
Timing Diagram

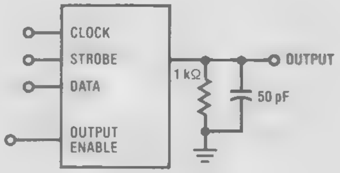


Test Circuits and Timing Diagrams for TRI-STATE®

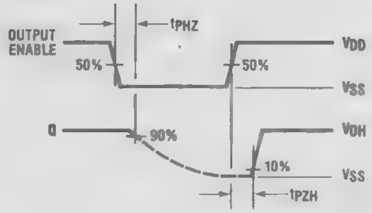


t_{PZL}, t_{PLZ}





t_{PZH}, t_{PHZ}



Logic Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q'_S
↑	0	X	X	Hi-Z	Hi-Z	Q7	No Chg.
↓	0	X	X	Hi-Z	Hi-Z	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	$Q_N - 1$	Q7	No Chg.
↑	1	1	1	1	$Q_N - 1$	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

X = Don't Care

*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

National Semiconductor

CD4099BM/CD4099BC 8-Bit Addressable Latch

General Description

The CD4099B is an 8-bit addressable latch with three address inputs (A0-A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D), and eight outputs (Q0-Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

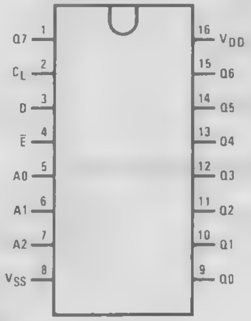
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Connection Diagram

CD4099B
Dual-In-Line and Flat Package



TOP VIEW

Truth Table

MODE SELECTION				
$\overline{E}$	CL	ADDRESSED LATCH	UNADDRESSED LATCH	MODE
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4099BM	−55°C to +125°C
CD4099BC	−40°C to +85°C

DC Electrical Characteristics CD4099BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD} = 5.0\,V$		5.0		0.02	5.0		150	μA
	$V_{DD} = 10\,V$		10		0.02	10		300	μA
	$V_{DD} = 15\,V$		20		0.02	20		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$								
	$V_{DD} = 5.0\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15\,V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$								
	$V_{DD} = 5.0\,V$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10\,V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15\,V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$	0.64		0.51	0.88		0.36		mA
	$V_{DD} = 10\,V$, $V_O = 0.5\,V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5.0\,V$, $V_O = 4.6\,V$	−0.64		−0.51	−0.88		−0.36		mA
	$V_{DD} = 10\,V$, $V_O = 9.5\,V$	−1.6		−1.3	−2.25		−0.9		mA
	$V_{DD} = 15\,V$, $V_O = 13.5\,V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$		−0.1		-10^{5}	−0.1		−1.0	μA
	$V_{DD} = 15\,V$, $V_{IN} = 15\,V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4099BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	$V_{DD} = 5.0\,V$		20		0.02	20		150	μA
	$V_{DD} = 10\,V$		40		0.02	40		300	μA
	$V_{DD} = 15\,V$		80		0.02	80		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$								
	$V_{DD} = 5.0\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10\,V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15\,V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert \leq 1\,\mu A$								
	$V_{DD} = 5.0\,V$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10\,V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15\,V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5.0\,V$, $V_O = 0.5$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (cont'd) CD4099BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OL} Low Level Output Current	$V_{DD}=5.0\,V$, $V_O=0.4\,V$	0.52		0.44	0.88		0.36		mA
	$V_{DD}=10\,V$, $V_O=0.5\,V$	1.3		1.1	2.25		0.9		mA
	$V_{DD}=15\,V$, $V_O=1.5\,V$	3.6		3.0	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	−0.88		−0.36		mA
	$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	−2.25		−0.9		mA
	$V_{DD}=15\,V$, $V_O=13.5\,V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN} Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.30		-10^{-5}	−0.30		−1.0	μA
	$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$, $R_L=200\,k$, Input $t_r=t_f=20\,ns$, unless otherwise noted.

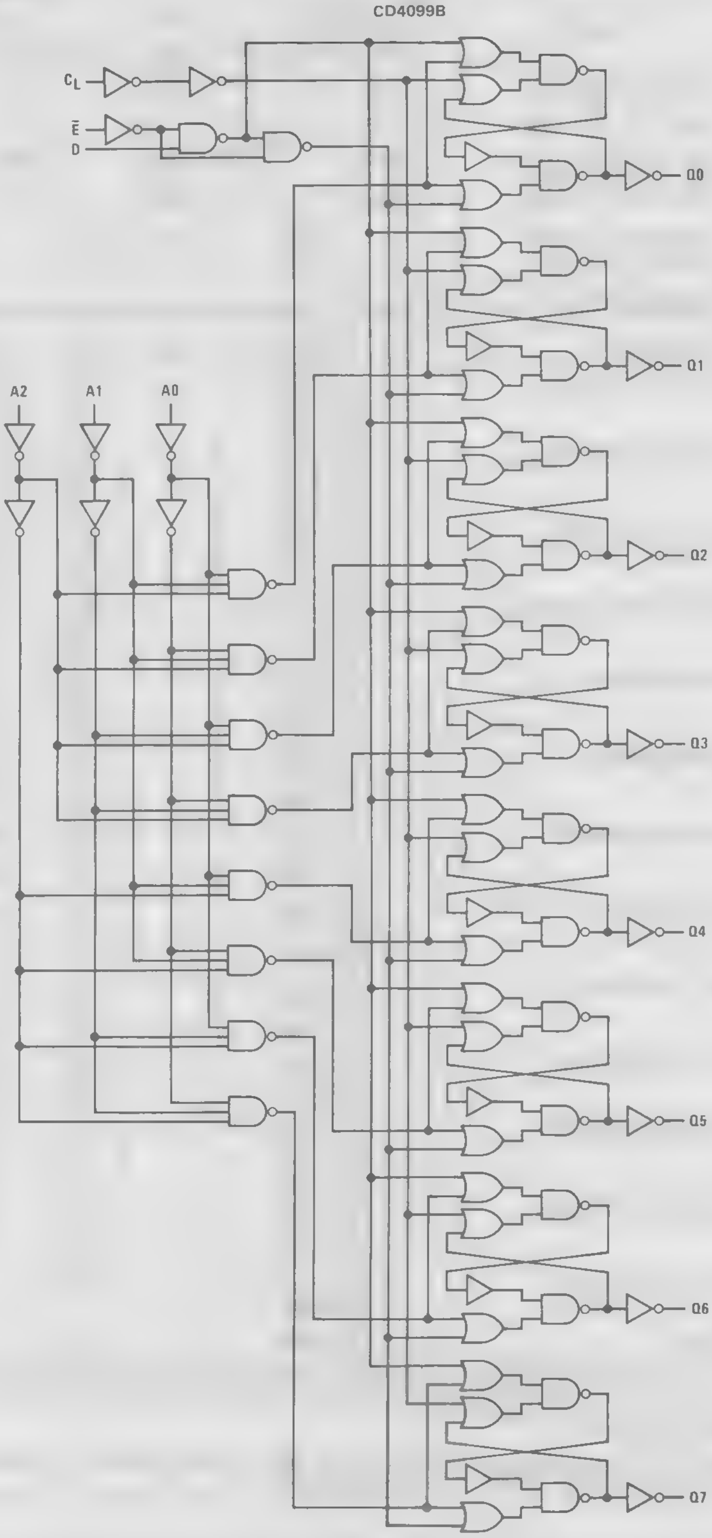
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PHL}, t_{PLH}	Propagation Delay Date to Output	$V_{DD}=5.0\,V$		200	400	ns
		$V_{DD}=10\,V$		75	150	ns
		$V_{DD}=15\,V$		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	$V_{DD}=5.0\,V$		200	400	ns
		$V_{DD}=10\,V$		80	160	ns
		$V_{DD}=15\,V$		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	$V_{DD}=5.0\,V$		175	350	ns
		$V_{DD}=10\,V$		80	160	ns
		$V_{DD}=15\,V$		65	130	ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	$V_{DD}=5.0\,V$		225	450	ns
		$V_{DD}=10\,V$		100	200	ns
		$V_{DD}=15\,V$		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		50	100	ns
		$V_{DD}=15\,V$		40	80	ns
t_{WH}, T_{WL}	Minimum Data Pulse Width	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		50	100	ns
		$V_{DD}=15\,V$		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	$V_{DD}=5.0\,V$		200	400	ns
		$V_{DD}=10\,V$		100	200	ns
		$V_{DD}=15\,V$		65	125	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD}=5.0\,V$		75	150	ns
		$V_{DD}=10\,V$		40	75	ns
		$V_{DD}=15\,V$		25	50	ns
t_{SU}	Minimum Set-Up Time Data to E	$V_{DD}=5.0\,V$		40	80	ns
		$V_{DD}=10\,V$		20	40	ns
		$V_{DD}=15\,V$		15	30	ns
t_H	Minimum Hold Time Data to E	$V_{DD}=5.0\,V$		60	120	ns
		$V_{DD}=10\,V$		30	60	ns
		$V_{DD}=15\,V$		25	50	ns
t_{SU}	Minimum Set-Up Time Address to E	$V_{DD}=5.0\,V$		−15	50	ns
		$V_{DD}=10\,V$		0	30	ns
		$V_{DD}=15\,V$		0	20	ns
t_H	Minimum Hold Time Address to E	$V_{DD}=5.0\,V$		−50	15	ns
		$V_{DD}=10\,V$		−20	10	ns
		$V_{DD}=15\,V$		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

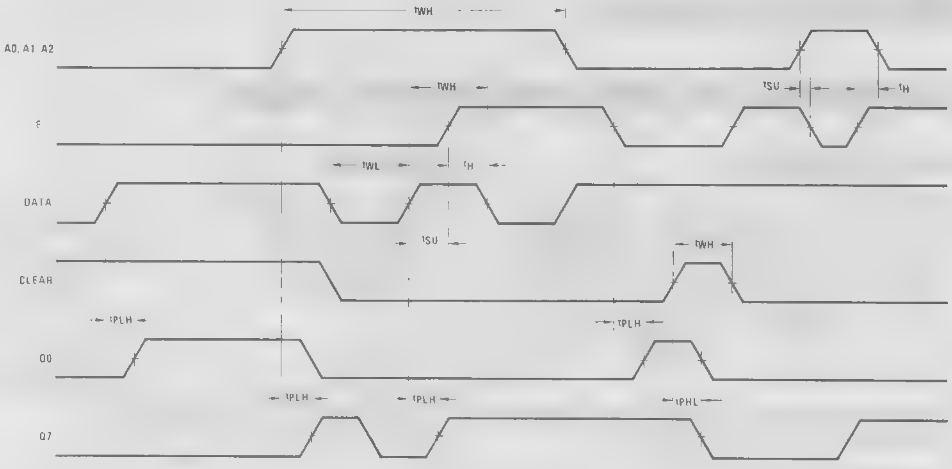
Note 2: $V_{SS}=0\,V$ unless otherwise specified.

Note 3: Dynamic power dissipation (P_D) is given by: $P_D=(C_{PD}+C_L)\,V_{CC}{}^2f+P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

Logic Diagram



Switching Time Waveforms



National Semiconductor

CD40106BM/CD40106BC Hex Schmitt Trigger

General Description

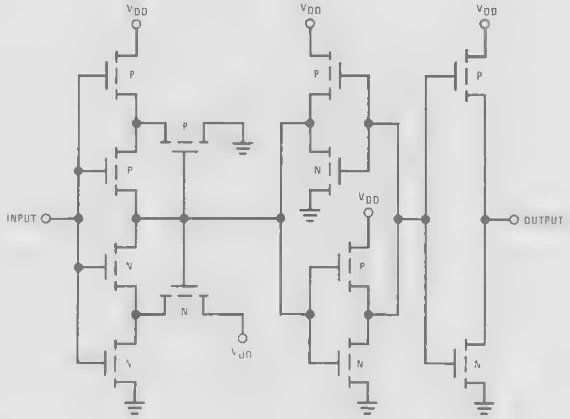
The CD40106B Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{DD} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{DD}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

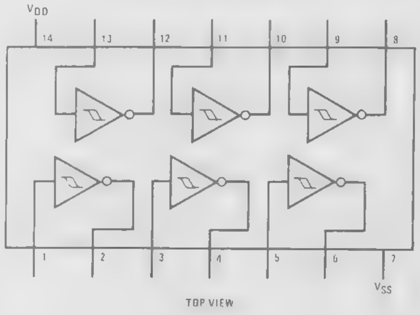
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.7 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Hysteresis	0.4 V_{DD} (typ.) 0.2 V_{DD} guaranteed
■ Equivalent to MM54C14/MM74C14	
■ Equivalent to MC14584B	

Schematic Diagram

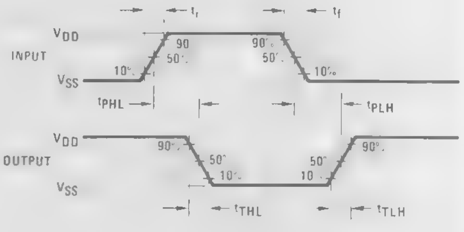


Connection Diagram

Dual-In-Line Package



Switching Time Waveforms



$t_r = t_f = 20$ ns

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40106BM	−55°C to +125°C
CD40106BC	−40°C to +85°C

DC Electrical Characteristics CD40106BM (Note 2)

	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

DC Electrical Characteristics CD40106BC (Note 2)

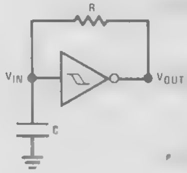
PARAMETER		CONDITIONS	−40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		4.0			4.0		30	μA
		$V_{DD} = 10V$		8.0			8.0		60	μA
		$V_{DD} = 15V$		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		$V_{DD} = 10V$, $V_O = 9V$	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	$V_{DD} = 5V$, $V_O = 0.5V$	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		$V_{DD} = 10V$, $V_O = 1V$	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		$V_{DD} = 15V$, $V_O = 1.5V$	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	$V_{DD} = 5V$	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		$V_{DD} = 10V$	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		$V_{DD} = 15V$	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	0.52		0.44	0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.30		10^{5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50 pF$, $R_L = 200k$, t_r and $t_f = 20 ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	$V_{DD} = 5V$		220	400	ns
		$V_{DD} = 10V$		80	200	ns
		$V_{DD} = 15V$		70	160	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 3)		14		pF

Typical Applications

Low Power Oscillator

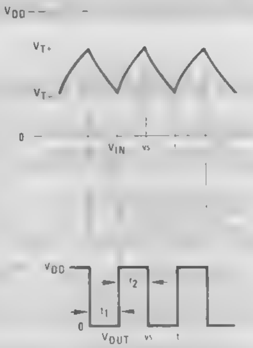


$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

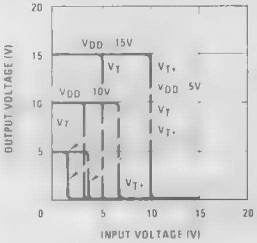
$$t_2 \approx RC \ln \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

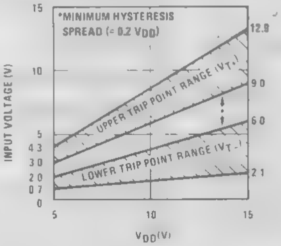
$$f \approx \frac{1}{RC \ln \frac{V_{T+} (V_{DD} - V_{T-})}{V_{T-} (V_{DD} - V_{T+})}}$$

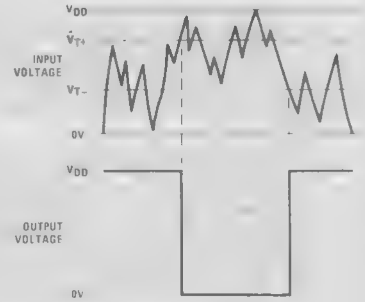
Note: The equations assume $t_1 + t_2 >> t_{pHL} + t_{pLH}$



Typical Performance Characteristics


Typical Transfer Characteristics


Guaranteed Trip Point Range



CD40160BM/CD40160BC, CD40161BM/CD40161BC,
CD40162BM/CD40162BC, CD40163BM/CD40163BC

National Semiconductor

CD40160BM/CD40160BC Decade Counter with Asynchronous Clear
CD40161BM/CD40161BC Binary Counter with Asynchronous Clear
CD40162BM/CD40162BC Decade Counter with Synchronous Clear
CD40163BM/CD40163BC Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

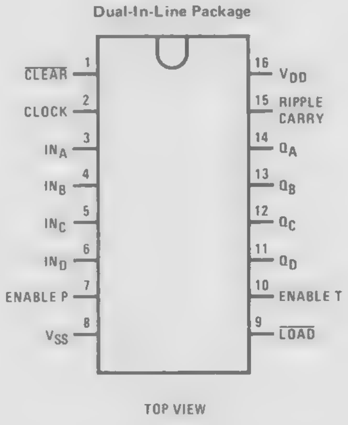
A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40162B and CD40163B is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the CD40160B and CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14160B, MC14161B, MC14162B, MC14163B
- Equivalent to MM74C160, MM74C161, MM74C162, MM74C163

Connection Diagram



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

DC Electrical Characteristics CD40160BC/CD40162BC/CD40163BC (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD40160BM/CD40162BM/CD40163BM (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O - 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

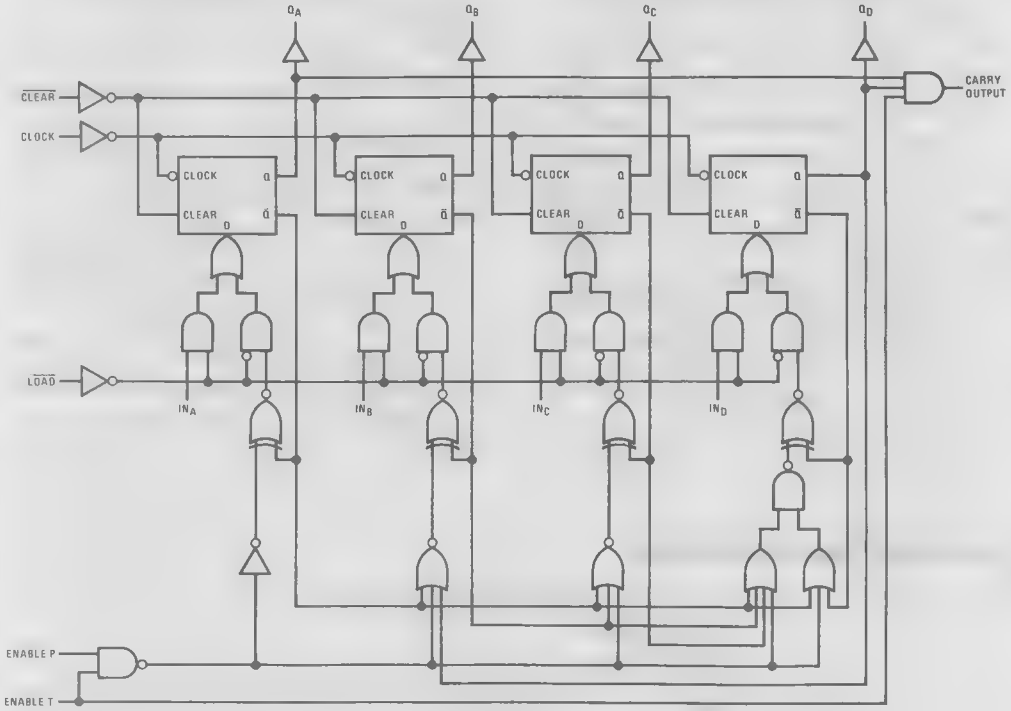
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, unless otherwise specified.

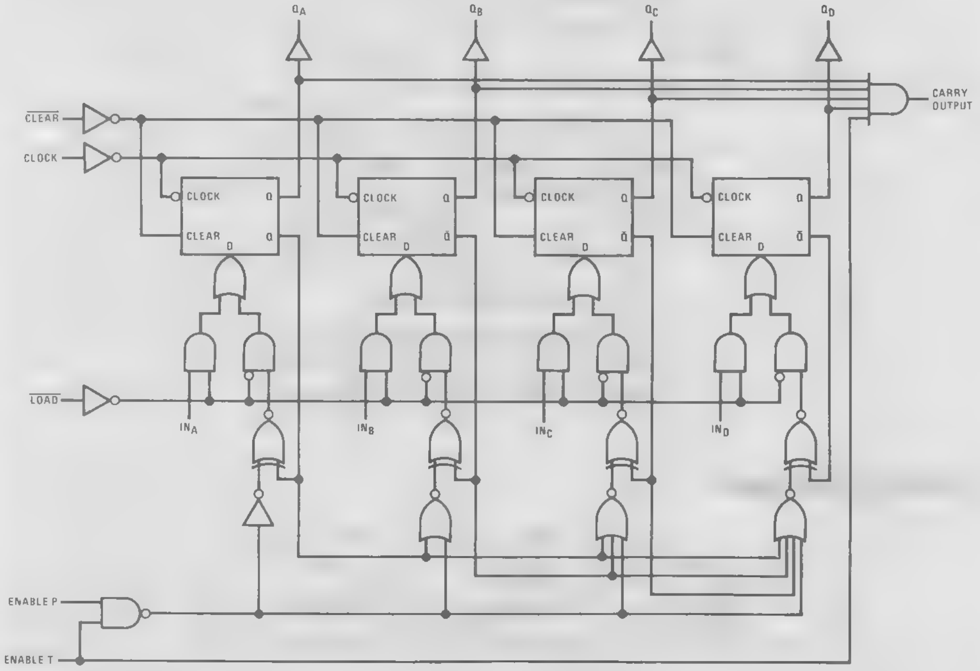
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Q	V_{DD} = 5V		250	400	ns
		V_{DD} = 10V		100	160	ns
		V_{DD} = 15V		80	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Carry Out	V_{DD} = 5V		290	450	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		100	160	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From T Enable to Carry Out	V_{DD} = 5V		180	290	ns
		V_{DD} = 10V		70	130	ns
		V_{DD} = 15V		60	110	ns
t_{PHL}	Propagation Time From Clear to Q (CD40160B, CD40161B Only)	V_{DD} = 5V		190	300	ns
		V_{DD} = 10V		80	150	ns
		V_{DD} = 15V		70	120	ns
t_{SU}	Minimum Time Prior to Clock that Data or Load must be Present	V_{DD} = 5V		120		ns
		V_{DD} = 10V		30		ns
		V_{DD} = 15V		25		ns
t_{SU}	Minimum Time Prior to Clock that Enable P or T must be Present	V_{DD} = 5V		170	280	ns
		V_{DD} = 10V		70	120	ns
		V_{DD} = 15V		60	100	ns
t_{SU}	Minimum Time Prior to Clock that Clear must be Present (CD40162B, CD40163B Only)	V_{DD} = 5V		120	190	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	70	ns
t_{WL} or t_{WH}	Maximum Clock Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise or Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5.0	μs
		V_{DD} = 15V			5.0	μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2	4		MHz
		V_{DD} = 10V	5.5	11		MHz
		V_{DD} = 15V	7	14		MHz
t_{THL} or t_{TLH}	Transition Time	All Outputs				
		V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity	(Note 3)		95		pF

Logic Diagram

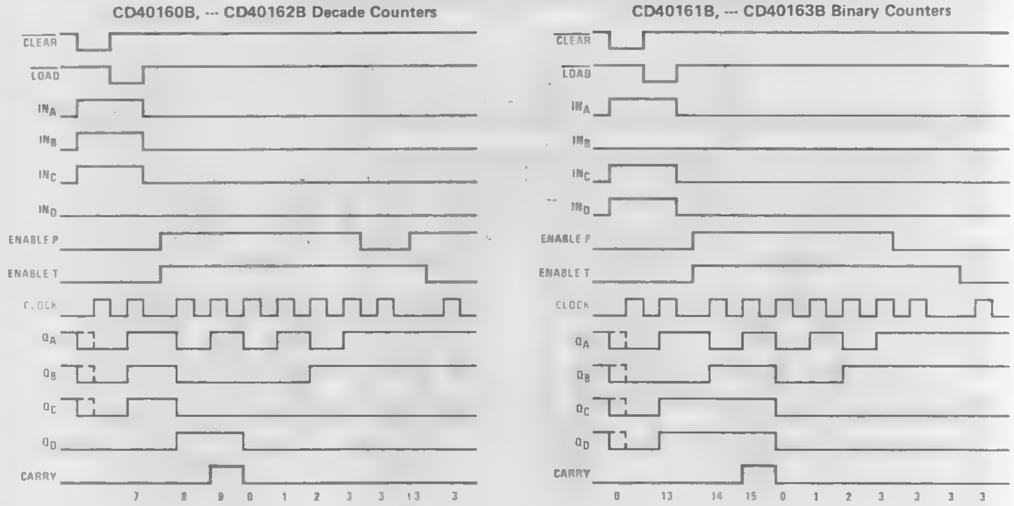
CD40160B, CD40162B Clear is Synchronous for the CD40162B



CD40161B, CD40163B Clear is Synchronous for the CD40163B



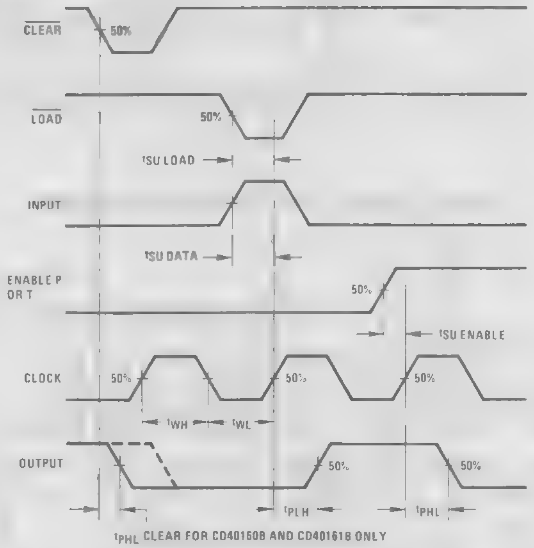
Logic Waveforms



CD40160B, — CD40162B Decade Counters

CD40161B, — CD40163B Binary Counters

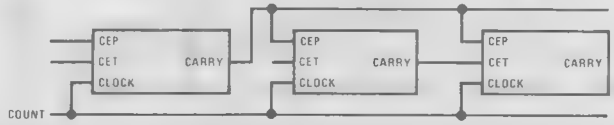
Switching Time Waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns PRR ≤ 1 MHz duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



National Semiconductor

CD40174BM/CD40174BC Hex D Flip-Flop
CD40175BM/CD40175BC Quad D Flip-Flop

General Description

The CD40174B consists of six positive-edge triggered D-type flip-flops; the true output from each flip-flop are externally available. The CD40175B consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at $\overline{\text{Clear}}$ input, clears all Q outputs to logical "0" and $\overline{Q}$'s (CD40175B only) to logical "1,"

All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

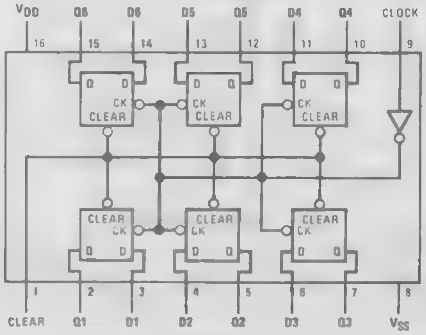
Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

- ■ Equivalent to MC14174B, MC14175B
- ■ Equivalent to MM74C174, MM74C175

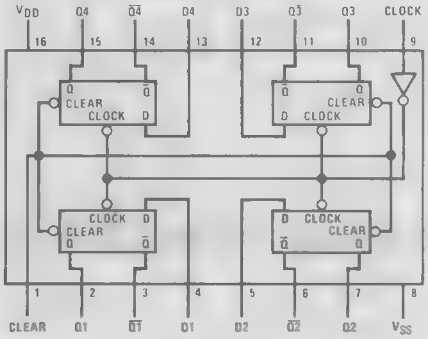
Connection Diagrams

CD40174B
Dual-In-Line Package



TOP VIEW

CD40175B
Dual-In-Line Package



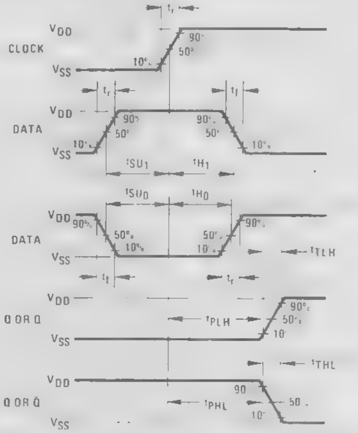
TOP VIEW

Truth Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change
* = $\overline{Q}$ for CD40175B only

Switching Time Waveforms



$t_r = t_f = 20$ ns

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

DC Electrical Characteristics CD40174BM/CD40175BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	4.2		3.4	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}			1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}			1.0	μA

DC Electrical Characteristics CD40174BC/CD40175BC/ (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4			4		30	μA
		V_{DD} = 10V		8			8		60	μA
		V_{DD} = 15V		16			16		120	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		8.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.41	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−8.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, and $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$ (CD40175 Only)	$V_{DD} = 5V$		190	300	ns
		$V_{DD} = 10V$		75	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PHL}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{DD} = 5V$		180	300	ns
		$V_{DD} = 10V$		70	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PLH}	Propagation Delay Time to a Logical "1" from Clear to $\overline{Q}$ (CD40175 Only)	$V_{DD} = 5V$		230	400	ns
		$V_{DD} = 10V$		90	150	ns
		$V_{DD} = 15V$		75	120	ns
t_{SU}	Time Prior to Clock Pulse that Data must be Present	$V_{DD} = 5V$	100	45		ns
		$V_{DD} = 10V$	40	16		ns
		$V_{DD} = 15V$	35	13		ns
t_H	Time after Clock Pulse that Data must be Held	$V_{DD} = 5V$		-11	0	ns
		$V_{DD} = 10V$		4	0	ns
		$V_{DD} = 15V$		3	0	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Clock Pulse Width	$V_{DD} = 5V$		130	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}	Minimum Clear Pulse Width	$V_{DD} = 5V$		120	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{RCL}	Maximum Clock Rise Time	$V_{DD} = 5V$	15	450		μs
		$V_{DD} = 10V$	5.0	125		μs
		$V_{DD} = 15V$	5.0	125		μs
t_{fCL}	Maximum Clock Fall Time	$V_{DD} = 5V$	15	50		μs
		$V_{DD} = 10V$	5.0	50		μs
		$V_{DD} = 15V$	5	50		μs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.0	3.5		MHz
		$V_{DD} = 10V$	5.0	10		MHz
		$V_{DD} = 15V$	6.0	12		MHz
C_{IN}	Input Capacitance	Clear Input,		10	15	pF
		Other Input		5.0	7.5	pF
C_{PD}	Power Dissipation	Per Package, (Note 3)		130		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

National Semiconductor

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BM and CD40192BC are BCD counters. While the CD40193BM and CD40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

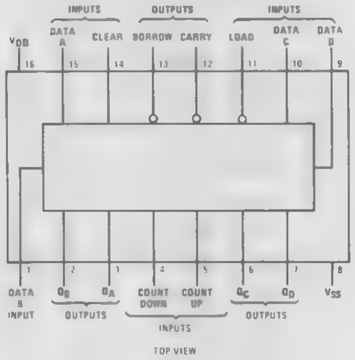
All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS}.

Features

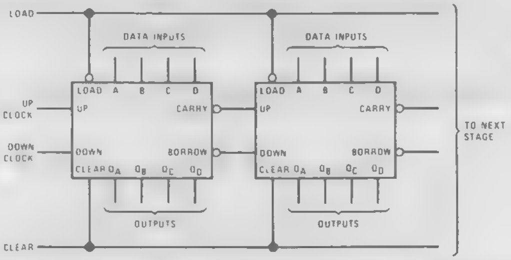
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Carry and borrow outputs for easy expansion to N-bit by cascading	
■ Asynchronous clear	
■ Equivalent to	MM54C192/MM74C192 and MM54C193/MM74C193

Connection Diagram

Dual-In-Line Package



Cascading Packages



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40192BM, CD40193BM	−55°C to +125°C
CD40192BC, CD40193BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) CD40192BM/CD40193BM

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics (Note 2) CD40192BC/CD40193BC

PARAMETER		CONDITIONS	40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, Input $t_r = t_f = 20\,ns$, unless otherwise specified.

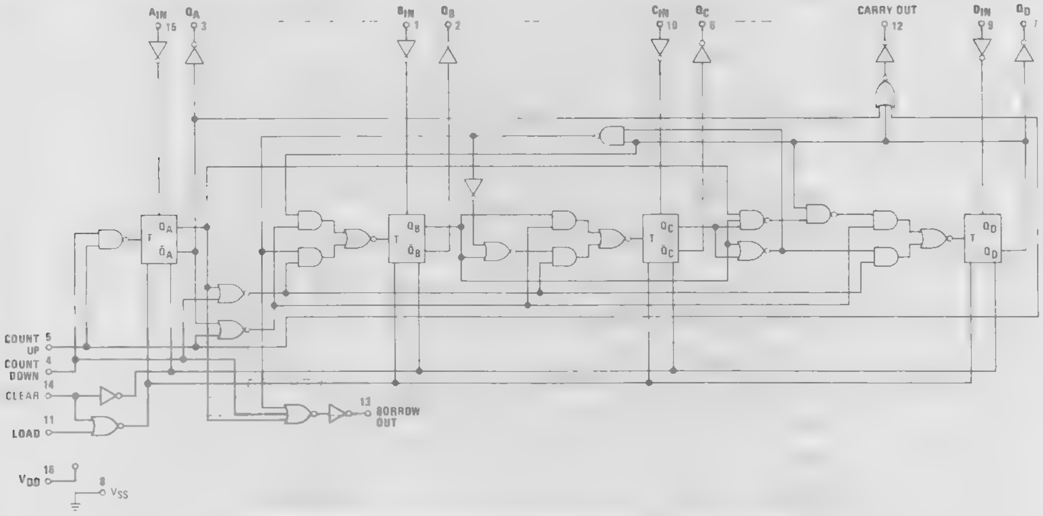
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Up Or Count Down To Q	$V_{DD} = 5V$		250	400	ns
		$V_{DD} = 10V$		100	160	ns
		$V_{DD} = 15V$		80	130	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Up To Carry	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		50	80	ns
		$V_{DD} = 15V$		40	65	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Down To Borrow	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		50	80	ns
		$V_{DD} = 15V$		40	65	ns
t_{SU}	Time Prior To Load That Data Must Be Present	$V_{DD} = 5V$		100	160	ns
		$V_{DD} = 10V$		30	50	ns
		$V_{DD} = 15V$		25	40	ns
t_{PHL}	Propagation Delay Time From Clear To Q	$V_{DD} = 5V$		130	220	ns
		$V_{DD} = 10V$		60	100	ns
		$V_{DD} = 15V$		50	80	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Load To Q	$V_{DD} = 5V$		300	480	ns
		$V_{DD} = 10V$		120	190	ns
		$V_{DD} = 15V$		95	150	ns
t_{TLH} or t_{THL}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Count Frequency	$V_{DD} = 5V$	2.5	4		MHz
		$V_{DD} = 10V$	6	10		MHz
		$V_{DD} = 15V$	7.5	12.5		MHz
t_{RCL} or t_{fCL}	Maximum Count Rise Or Fall Time	$V_{DD} = 5V$	15			µs
		$V_{DD} = 10V$	5			µs
		$V_{DD} = 15V$	1			µs
t_{WH}, t_{WL}	Minimum Count Pulse Width	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		35	80	ns
		$V_{DD} = 15V$		28	65	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$		300	480	ns
		$V_{DD} = 10V$		120	190	ns
		$V_{DD} = 15V$		95	150	ns
t_{WL}	Minimum Load Pulse Width	$V_{DD} = 5V$		100	160	ns
		$V_{DD} = 10V$		40	65	ns
		$V_{DD} = 15V$		32	55	ns
C_{IN}	Average Input Capacitance	Load and Data Inputs (A,B,C,D)		5	7.5	pF
		Count Up, Count Down and Clear		10	15	pF
C_{PD}	Power Dissipation Capacity	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

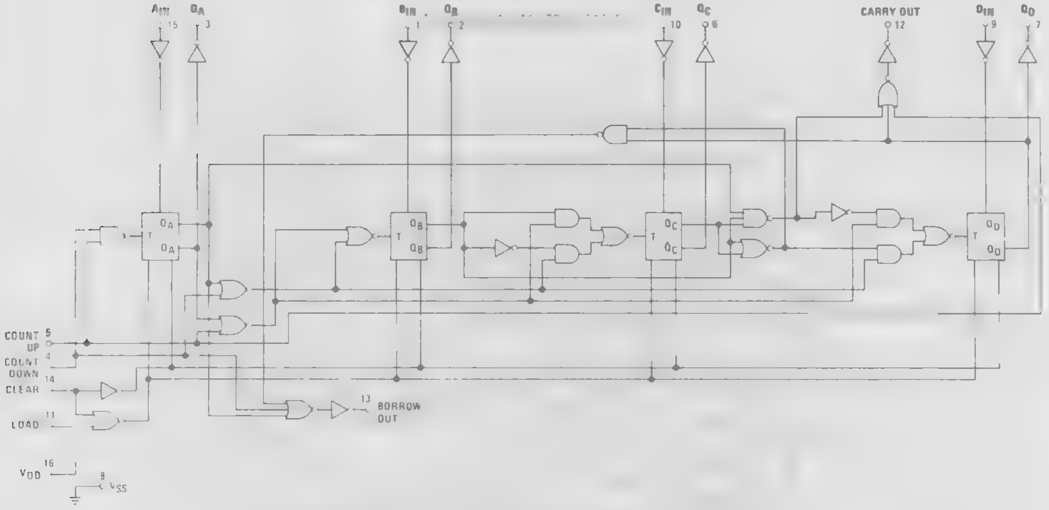
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Schematic Diagrams

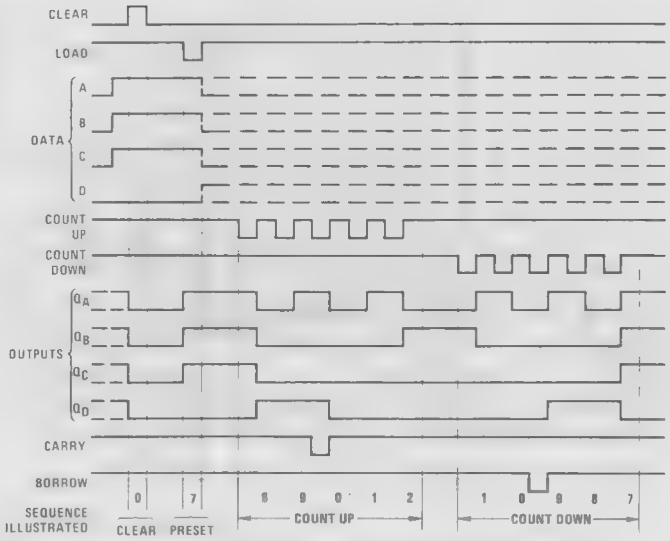


CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter



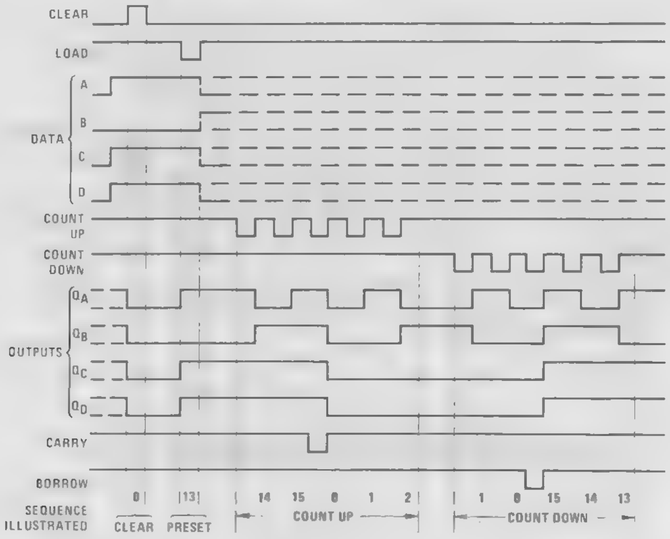
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

Timing Diagrams



Sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.

CD40192BM/CD40192BC



Sequence:
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.

CD40193BM/CD40193BC

National Semiconductor

CD4503BM/CD4503BC Hex Non-Inverting TRI-STATE® Buffer

General Description

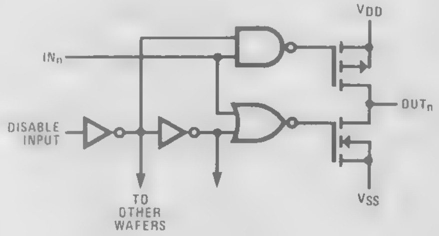
The CD4503B is a hex non-inverting TRISTATE® buffer with high output current sink and source capability. TRI-STATE outputs make it useful in bus-oriented applications. Two separate disable inputs are provided. Buffers 1 through 4 are controlled by the disable 4 input. Buffers 5 and 6 are controlled by the disable 2 input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

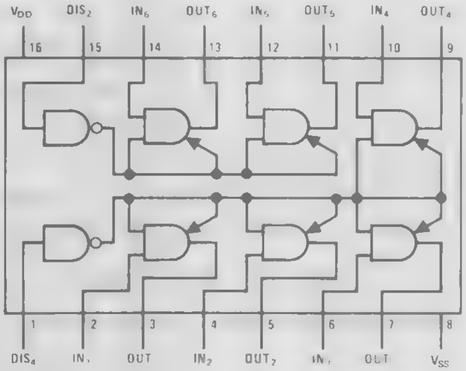
TRI-STATE is a registered trademark of National Semiconductor Corp.

Features

- Wide supply voltage range 3.0 V_{DC} to 18 V_{DC}
- TRI-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- Pin-for-pin replacement for MM80C97 and MC14503

Schematic and Connection Diagrams





TOP VIEW

Truth Table

In	Disable Input	Out
0	0	0
1	0	1
X	1	TRI-STATE

X = Don't Care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} — Supply Voltage	−0.5V to +18V
V_{IN} — Input Voltage	−0.5V to +0.5V
T_S — Storage Temperature Range	−65°C to +150°C
P_D — Power Dissipation	500 mW
T_L — Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} — Supply Voltage	3V to 15V
T_A — Operating Temperature Range	
CD4503BM	−55°C to +125°C
CD4503BC	−40°C to +85°C

DC Electrical Characteristics CD4503BM (Note 2)

Parameter	Conditions	−55°C		+25°C			+125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		1			1		30	μA
	V_{DD} = 10V		2			2		60	μA
	V_{DD} = 15V		4			4		120	μA
V_{OL} Low Level Output Voltage	V_{IN} = V_{DD} or 0								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{IN} = V_{DD} or 0								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 4.5V, V_{OL} = 0.4V	2.80		2.30	2.55		1.60		mA
	V_{DD} = 5.0V, V_{OL} = 0.4V	3.00		2.40	2.75		1.75		mA
	V_{DD} = 10V, V_{OL} = 0.5V	7.85		6.35	7.00		4.45		mA
	V_{DD} = 15V, V_{OL} = 1.5V	19.95		16.10	25.00		11.30		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_{OH} = 4.6V	−1.28		−1.02	−1.76		−0.72		mA
	V_{DD} = 10V, V_{OH} = 9.5V	−3.20		−2.60	−4.5		−1.8		mA
	V_{DD} = 15V, V_{OH} = 13.5V	−8.20		−6.80	−17.6		−4.8		mA
I_{OZ} TRI-STATE® Leakage Current	V_{DD} = 15V		±0.1		$\pm 10^{-4}$	±0.1		±1.0	μA
I_{IN} Input Current	V_{DD} = 15V		±0.1		$\pm 10^{-4}$	±0.1		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics CD4503BC (Note 2)

Parameter	Conditions	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Units
I_{DD} Quiescent Device Current	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		4 8 16		4 8 16			30 60 120	μA μA μA
V_{OL} Low Level Output Voltage	V_{IN} = V_{DD} or 0 V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V_{OH} High Level Output Voltage	V_{IN} = V_{DD} or 0 V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V V V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 4.5V, V_{OL} = 0.4V V_{DD} = 5.0V, V_{OL} = 0.4V V_{DD} = 10V, V_{OL} = 0.5V V_{DD} = 15V, V_{OL} = 1.5V	2.30 2.5 6.5 16.50		1.95 2.10 5.45 13.80	2.65 2.75 7.0 25.00		1.60 1.75 4.45 11.30		mA mA mA mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_{OH} = 4.6V V_{DD} = 10V, V_{OH} = 9.5V V_{DD} = 15V, V_{OH} = 13.5V	−1.04 −2.60 −7.2		−0.88 −2.2 −6.0	−1.76 −4.50 −17.6		−0.7 −1.8 −4.8		mA mA mA
I_{TL} TRI-STATE® Leakage Current	V_{DD} = 15V		±0.3		$\pm10^{-4}$	±0.3		±1.0	μA
I_{IN} Input Current	V_{DD} = 15V		±0.3		$\pm10^{-5}$	±0.3		±1.0	

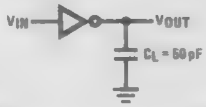
AC Electrical Characteristics CD4503B

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, Input t_r = t_f = 20 ns, unless otherwise specified.

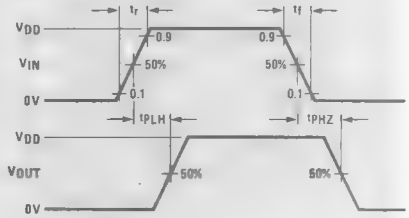
Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		75 35 25	100 40 30	ns ns ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, Logical Level to High Impedance State	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		80 40 35	125 90 70	ns ns ns
t_{PZL}, t_{PZH}	Propagation Delay Time, High Impedance State to Logical Level	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		95 40 35	175 80 70	ns ns ns
t_{TLH}	Output Rise Time	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		45 23 18	80 40 35	ns ns ns
t_{THL}	Output Fall Time	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		45 23 18	80 40 35	ns ns ns

AC Test Circuits and Switching Time Waveforms

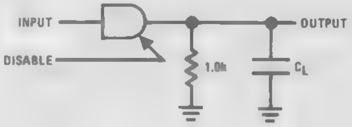
t_{PHL}, t_{PLH}



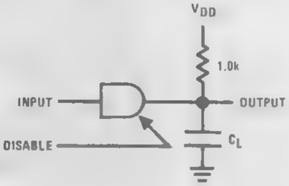
CMOS to CMOS



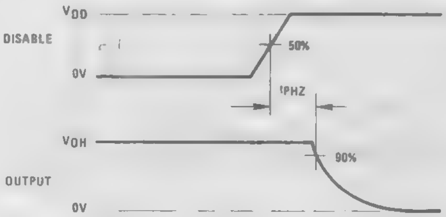
t_{PHZ} and t_{PZH}



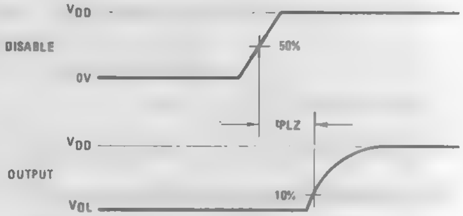
t_{PLZ} and t_{PZL}



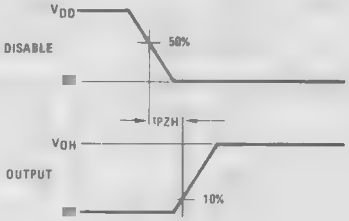
t_{PHZ}



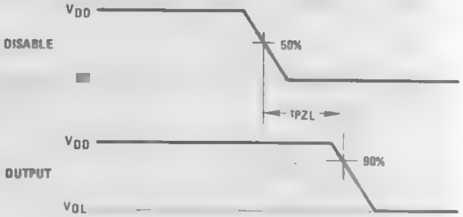
t_{PLZ}



t_{PZH}



t_{PZL}



Note: Delays measured with input t_r, $t_f \leq 20$ ns.

National Semiconductor

CD4510BM/CD4510BC BCD Up/Down Counter
CD4516BM/CD4516BC Binary Up/Down Counter

General Description

The CD4510BM/CD4510BC and CD4516BM/CD4516BC are monolithic CMOS up/down counters which count in BCD and binary, respectively.

The counters count up when the up/down input is at logical "1" and vice versa. A logical "1" preset enable signal allows information at the parallel inputs to preset the counters to any state synchronously with the clock. The counters are advanced one count at the positive-going edge ofthe clock if the carry in, preset enable, and reset inputs are at logical "0". Advancement is inhibited when any of these three inputs are at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" when the counter reaches its maximum count in the "up" mode or its minimum count in the "down" mode, provided the carry input is at logical "0" state. The counters are cleared asynchronously by applying a logical "1" voltage level at the reset input.

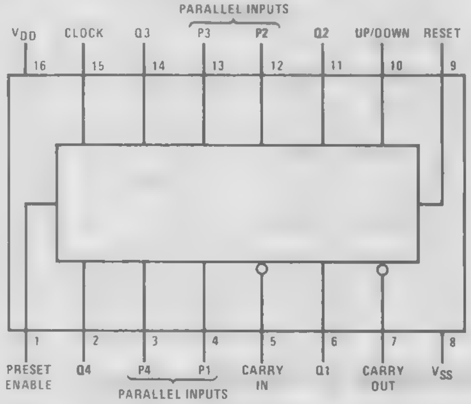
All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Parallel load "jam" inputs
- Low quiescent power dissipation 0.25 μW/package (typ.) @ V_{CC} = 5.0 V
- Motorola MC14510, MC14516 second source

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Truth Table

CLOCK	RESET	PRESET ENABLE	CARRY IN	UP/DOWN	OUTPUT FUNCTION
X	1	X	X	X	Reset to zero
X	0	1	X	X	Set to P1, P2, P3, P4
↑	0	0	0	1	Count up
↑	0	0	0	0	Count down
↓	0	0	X	X	No change
X	0	0	1	X	No change

↑ = positive transition
↓ = negative transition
X = don't care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

DC Electrical Characteristics CD4510BM/CD4516BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.05	5		150	μA
		V_{DD} = 10V		10		0.1	10		300	μA
		V_{DD} = 15V		20		0.15	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.8		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−7.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.05	20		150	μA
		V_{DD} = 10V		40		0.1	40		300	μA
		V_{DD} = 15V		80		0.15	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4510BC/CD4516BC (Note 2)

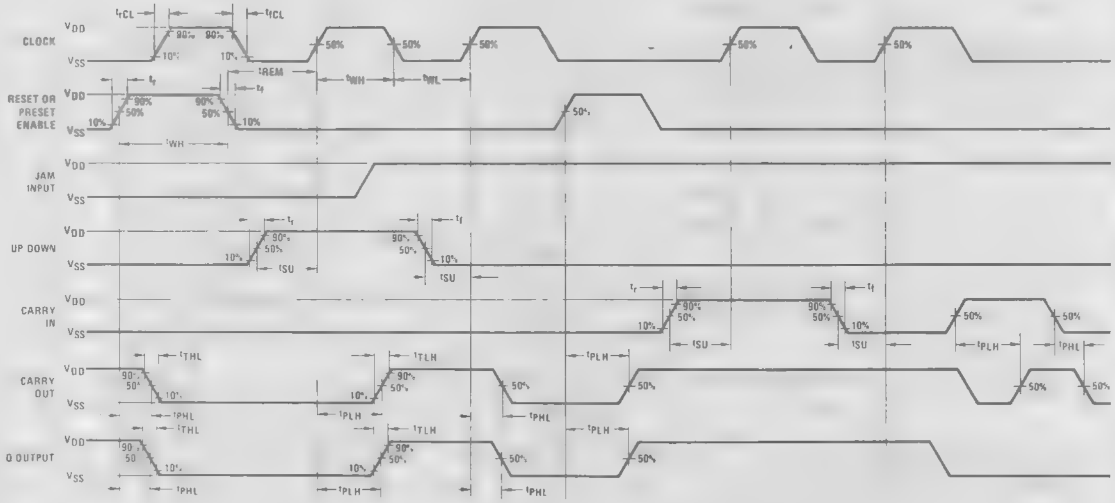
PARAMETER		CONDITIONS	40 C		25 C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.8		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.0		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	7.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	-0.52		-0.44	-0.8		0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	1.3		-1.1	2.0		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-3.6		-3.0	-7.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.3		-10^{-5}	-0.3		1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{5}	0.3		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: Devices should not be connected while power is "ON."

Switching Time Waveforms



AC Electrical Characteristics CD4510BM/CD4510BC, CD4516BM/CD4516BC

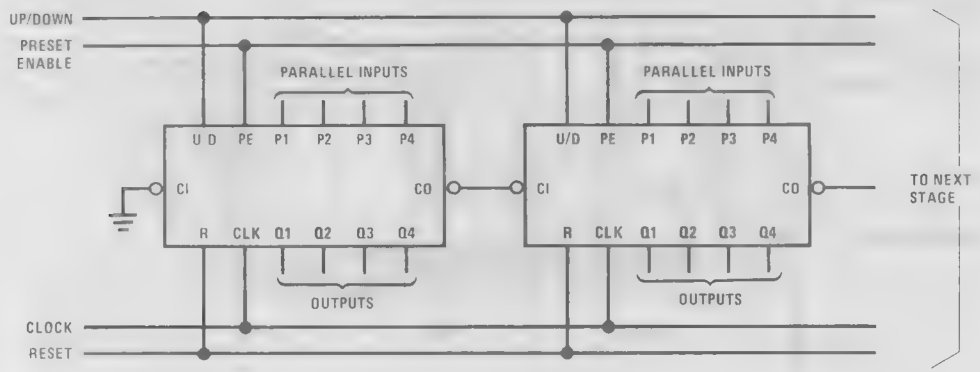
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_{rCL} = t_{fCL} = t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q Outputs	$V_{DD} = 5V$		220	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Carry Output	$V_{DD} = 5V$		315	630	ns
		$V_{DD} = 10V$		130	260	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q and Carry Outputs	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		160	315	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		50	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	15			μs
		$V_{DD} = 15V$	15			μs
t_{SU}	Minimum Carry In Set-Up Time	$V_{DD} = 5V$		100	220	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	70	ns
t_{SU}	Minimum Up/Down Set-Up Time	$V_{DD} = 5V$		200	420	ns
		$V_{DD} = 10V$		70	170	ns
		$V_{DD} = 15V$		60	150	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	3.1		MHz
		$V_{DD} = 10V$	3.8	7.6		MHz
		$V_{DD} = 15V$	5.0	10.0		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Per Package,		65		pF
RESET/PRESET ENABLE OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Q Output	$V_{DD} = 5V$		285	570	ns
		$V_{DD} = 10V$		115	230	ns
		$V_{DD} = 15V$		95	195	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Carry Output	$V_{DD} = 5V$		420	860	ns
		$V_{DD} = 10V$		170	350	ns
		$V_{DD} = 15V$		140	290	ns
t_{WH}	Minimum Reset/Preset Enable Pulse Width	$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		40	100	ns
		$V_{DD} = 15V$		35	80	ns
t_{REM}	Minimum Reset/Preset Enable Removal Time	$V_{DD} = 5V$		170	330	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		60	120	ns
CARRY INPUT OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry In to Carry Output	$V_{DD} = 5V$		260	500	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns

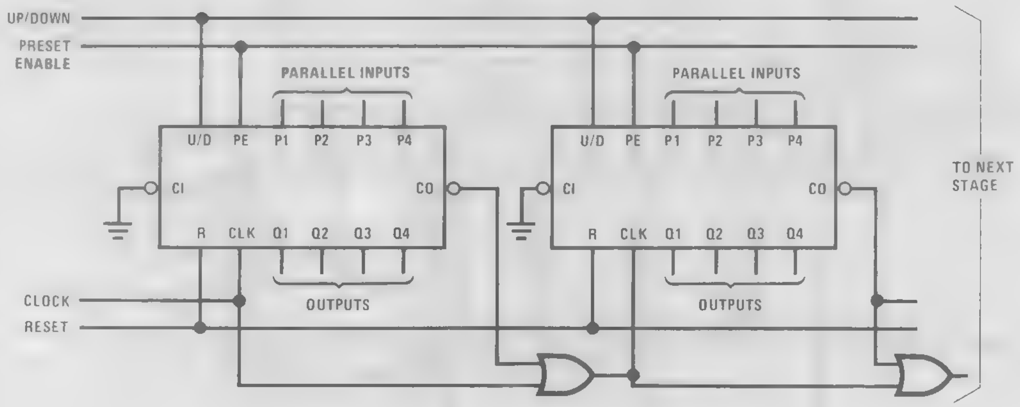
Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L)V_{DD}{}^2f + P_Q$; where C_L = load capacitance; f = frequency of operation; P_Q = Quiescent Power Dissipation. For further details, see application note AN-90, "54C/74C Family characteristics."

Cascading Packages

Parallel Clocking



Ripple Clocking



Schematic Diagrams

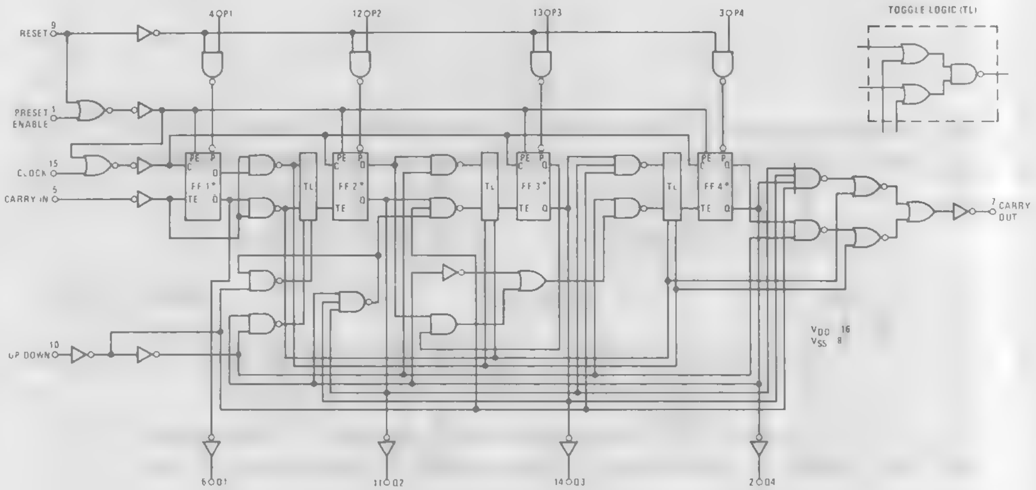
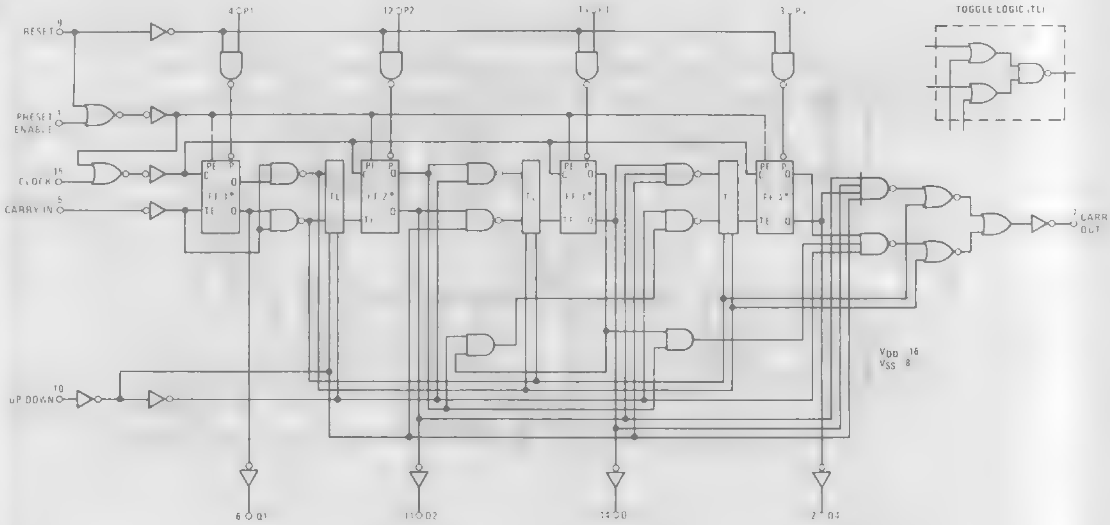


FIGURE 1. CD4510

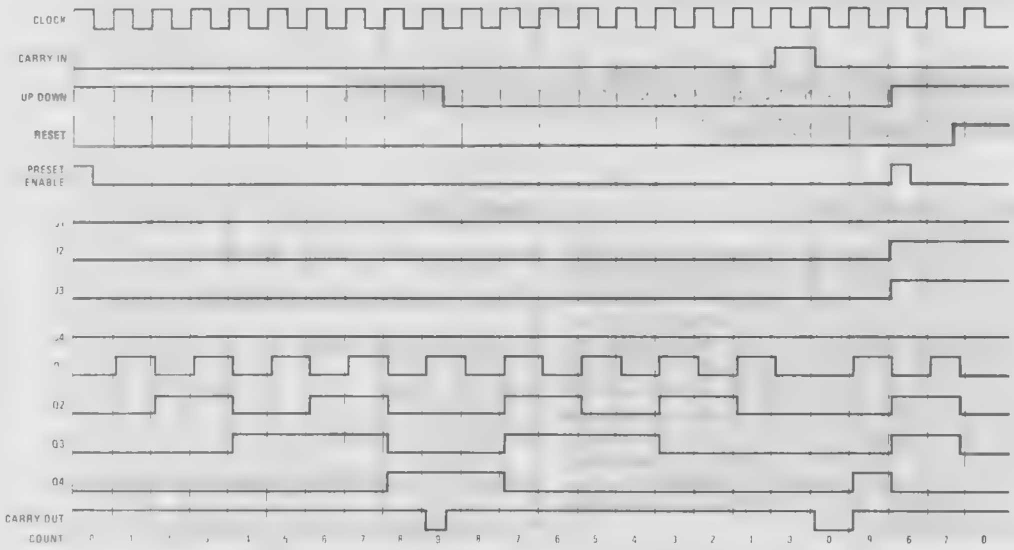


*Flip-flop toggles at the positive-going edge of clock (C) if Toggle Enable (TE) is at logical "1" and Preset Enable (PE) is at logical "0"

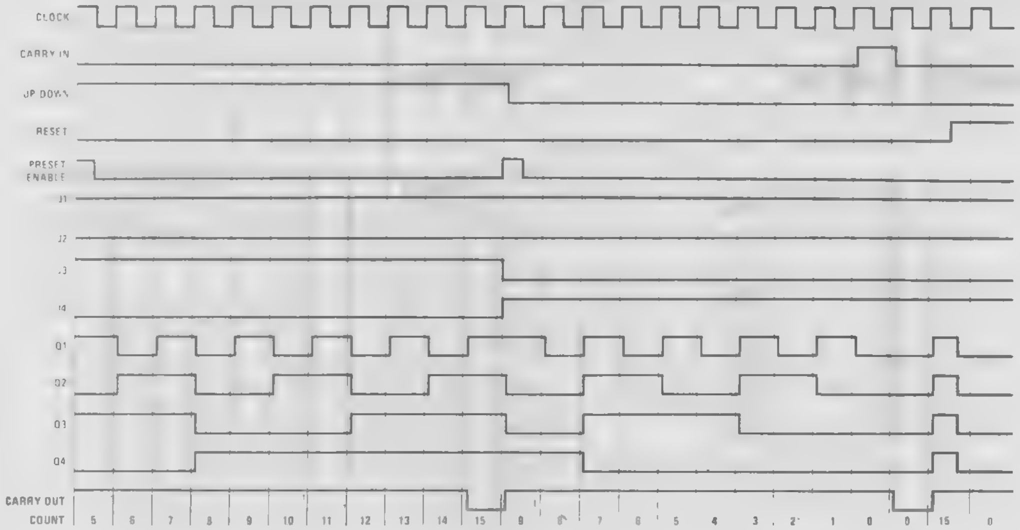
FIGURE 2. CD4516

Logic Waveforms

CD4510BM/CD4510BC



CD4516BM/CD4516BC



National Semiconductor

CD4511BM/CD4511BC BCD-to-7 Segment Latch/Decoder/Driver

General Description

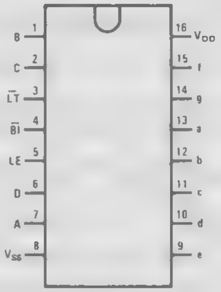
The CD4511BM/CD4511BC BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

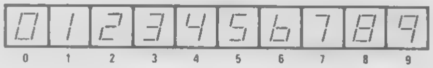
- Low logic circuit power dissipation
- High current sourcing outputs (up to 25 mA)
- Latch storage of code
- Blanking input
- Lamp test provision
- Readout blanking on all illegal input combinations
- Lamp intensity modulation capability
- Time share (multiplexing) facility
- Equivalent to Motorola MC14511

Connection Diagram

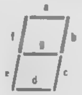


TOP VIEW

Display



Segment Identification



Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				*

X = Don't care

*Depends upon the BCD code applied during the 0 to 1 transition of LE

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	–0.5V to +18V
V_{IN} Input Voltage	–0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	–65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4510BM, CD4516BM	–55°C to +125°C
CD4510BC, CD4516BC	–40°C to +85°C

DC Electrical Characteristics CD4511BM

PARAMETER	CONDITIONS	–55°C MIN	–55°C TYP	–55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C TYP	+125°C MAX	UNITS
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V	14.1			14.1	14.59		14.1			V
Low Level Input Voltage (V_{IL})	V_{DD} = 5V, V_{OUT} = 3.8V or 0.5V			1.5		2	1.5			1.5	V
	V_{DD} = 10V, V_{OUT} = 8.8V or 1.0V			3.0		4	3.0			3.0	V
	V_{DD} = 15V, V_{OUT} = 13.8V or 1.5V			4.0		6	4.0			4.0	V
High Level Input Voltage (V_{IH})	V_{DD} = 5V, V_{OUT} = 0.5V or 3.8V	3.5			3.5	3		3.5			V
	V_{DD} = 10V, V_{OUT} = 1.0V or 8.8V	7.0			7.0	6		7.0			V
	V_{DD} = 15V, V_{OUT} = 1.5V or 13.8V	11.0			11.0	9		11.0			V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA	4.1			4.1	4.57		4.1			V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA	3.9			3.9	4.12		3.5			V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA	3.4			3.4	3.75		3.0			V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA	9.1			9.1	9.58		9.1			V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA	9.0			9.0	9.17		8.6			V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA	8.6			8.6	8.9		8.2			V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA	14.1			14.1	14.59		14.1			V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA	14.0			14.0	14.18		13.6			V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA	13.6			13.6	13.95		13.2			V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Low Level Output Current (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.64			0.51	0.88		0.36			mA
	V_{DD} = 10V, V_{OL} = 0.5V	1.6			1.3	2.25		0.9			mA
	V_{DD} = 15V, V_{OL} = 1.5V	4.2			3.4	8.8		2.4			mA
Input Current (I_{IN})	V_{DD} = 15V, V_{IN} = 0V			–0.10		-10^{-5}	–0.10			–1.0	μA
	V_{DD} = 15V, V_{IN} = 15V			0.10		10^{-5}	0.10			1.0	μA

Note 1: Devices should not be connected with power on.

DC Electrical Characteristics CD4511BC

PARAMETER	CONDITIONS	−40°C			+25°C			+85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V	14.1			14.1	14.59		14.1			V
Low Level Input Voltage (V_{IL})	V_{DD} = 5V, V_{OUT} = 3.8V or 0.5V			1.5		2	1.5			1.5	V
	V_{DD} = 10V, V_{OUT} = 8.8V or 1.0V			3.0		4	3.0			3.0	V
	V_{DD} = 15V, V_{OUT} = 13.8V or 1.5V			4.0		6	4.0			4.0	V
High Level Input Voltage (V_{IH})	V_{DD} = 5V, V_{OUT} = 0.5V or 3.8V	3.5			3.5	3		3.5			V
	V_{DD} = 10V, V_{OUT} = 1.0V or 8.8V	7.0			7.0	6		7.0			V
	V_{DD} = 15V, V_{OUT} = 1.5V or 13.8V	11.0			11.0	9		11.0			V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA	4.1			4.1	4.57		4.1			V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA	3.6			3.6	4.12		3.3			V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA	2.8			2.8	3.75		2.5			V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA	9.1			9.1	9.58		9.1			V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA	8.75			8.75	9.17		8.45			V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA	8.1			8.1	8.9		7.8			V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA	14.1			14.1	14.59		14.1			V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA	13.75			13.75	14.18		13.45			V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA	13.1			13.1	13.95		12.8			V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Low Level Output Current (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.52			0.44	0.88		0.36			mA
	V_{DD} = 10V, V_{OL} = 0.5V	1.3			1.1	2.25		0.9			mA
	V_{DD} = 15V, V_{OL} = 1.5V	3.6			3.0	8.8		2.4			mA
Input Current (I_{IN})	V_{DD} = 15V, V_{IN} = 0V			−0.30		-10^{-5}	−0.30			−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V			0.30		10^{-5}	0.30			1.0	μA

AC Electrical Characteristics

$T_A = 25°C$ and $C_L = 50\,pF$, typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	CD4511BX			UNITS
		MIN	TYP	MAX	
Input Capacitance (C_{IN})	$V_{IN} = 0$		5.0	7.5	pF
Output Rise Time (t_r) *(Figure 1a)*	$V_{DD} = 5V$		40	80	ns
	$V_{DD} = 10V$		30	60	ns
	$V_{DD} = 15V$		25	50	ns
Output Fall Time (t_f) *(Figure 1a)*	$V_{DD} = 5V$		125	250	ns
	$V_{DD} = 10V$		75	150	ns
	$V_{DD} = 15V$		65	130	ns
Turn-Off Delay Time (Data) (t_{PLH}) *(Figure 1a)*	$V_{DD} = 5V$		640	1280	ns
	$V_{DD} = 10V$		250	500	ns
	$V_{DD} = 15V$		175	350	ns
Turn-On Delay Time (Data) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		720	1440	ns
	$V_{DD} = 10V$		290	580	ns
	$V_{DD} = 15V$		195	400	ns
Turn-Off Delay Time (Blank) (t_{PLH}) *(Figure 1a)*	$V_{DD} = 5V$		320	640	ns
	$V_{DD} = 10V$		130	260	ns
	$V_{DD} = 15V$		100	200	ns
Turn-On Delay Time (Blank) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		485	970	ns
	$V_{DD} = 10V$		200	400	ns
	$V_{DD} = 15V$		160	320	ns
Turn-Off Delay Time (Lamp Test) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		313	625	ns
	$V_{DD} = 10V$		125	250	ns
	$V_{DD} = 15V$		90	180	
Turn-On Delay Time (Lamp Test) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		313	625	ns
	$V_{DD} = 10V$		125	250	ns
	$V_{DD} = 15V$		90	180	ns
Setup Time (t_{SETUP}) *(Figure 1b)*	$V_{DD} = 5V$	180	90		ns
	$V_{DD} = 10V$	76	38		ns
	$V_{DD} = 15V$	40	20		ns
Hold Time (t_{HOLD}) *(Figure 1b)*	$V_{DD} = 5V$	0	–90		ns
	$V_{DD} = 10V$	0	–38		ns
	$V_{DD} = 15V$	0	–20		ns
Minimum Latch Enable Pulse Width (PW_{LE}) *(Figure 1c)*	$V_{DD} = 5V$	520	260		ns
	$V_{DD} = 10V$	220	110		ns
	$V_{DD} = 15V$	130	65		ns

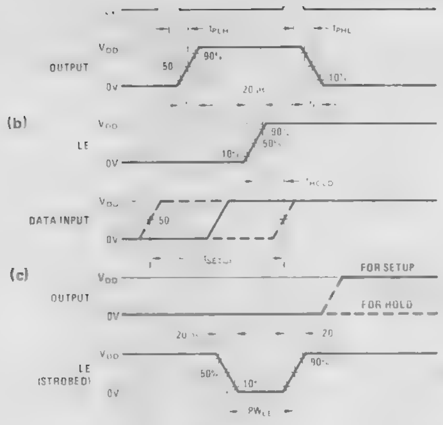
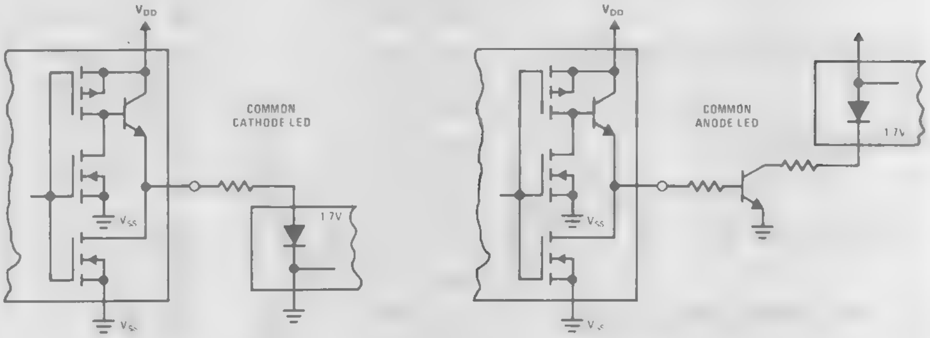


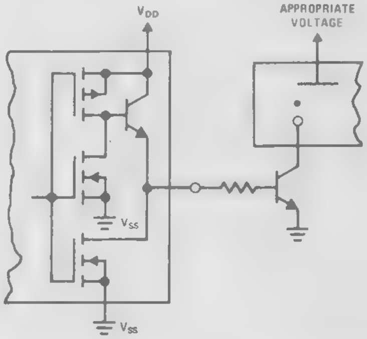
FIGURE 1.

Typical Applications

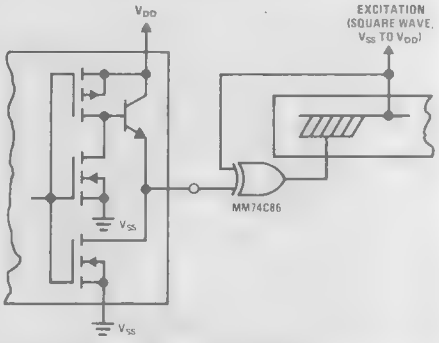
Light Emitting Diode (LED) Readout



Gas Discharge Readout



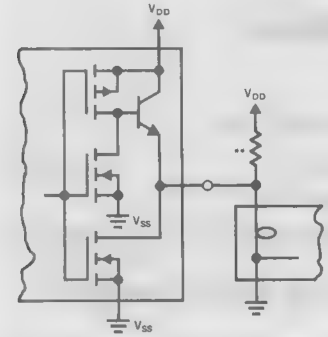
Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts

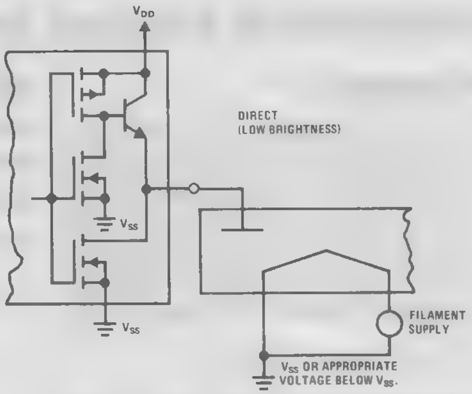
Typical Applications (Cont'd.)

Incandescent Readout



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament

Fluorescent Readout



National Semiconductor

CD4512M/CD4512C 8-Channel Data Selector

General Description

The CD4512M/CD4512C 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ($\overline{OE}$) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ($\overline{OE}$) inputs allow normal operation.

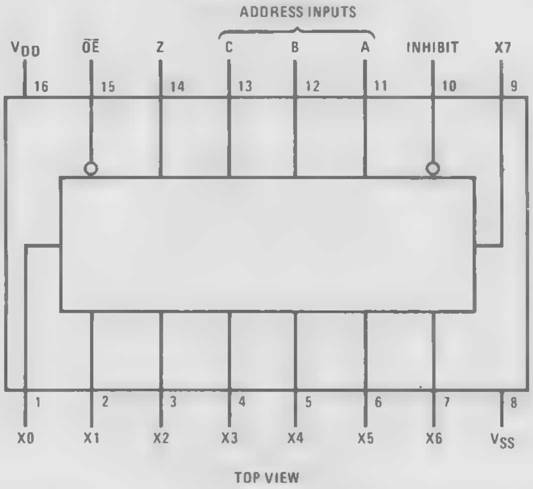
TRI-STATE is a trademark of National Semiconductor Corp

Features

- Wide supply voltage range 3.0V-15V
- High noise immunity 0.45 V_{DD} (typ.)
- TRI-STATE output
- Low quiescent power dissipation 0.25 μW/package (typ.) @ $V_{CC} = 5.0V$
- Plug-in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package



ADDRESS INPUTS			CONTROL INPUTS		OUTPUT
C	B	A	INHIBIT	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
Ø	Ø	Ø	1	0	0
Ø	Ø	Ø	Ø	1	Hi-Z

Ø = Don't care
Hi-Z = TRI-STATE® condition
Xn = Data at input n

Absolute Maximum Ratings

(Notes 1 & 2)

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4512M	−55°C to +125°C
CD4512C	−40°C to +85°C

DC Electrical Characteristics CD4512M (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0		0.005	5.0		150	μA
	V_{DD} = 10 V		10		0.010	10		300	μA
	V_{DD} = 15 V		20		0.015	20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.50		0.40	0.78		0.38		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.1		0.90	2.0		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	7.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.62		−0.50	−1.7		−0.35		mA
	V_{DD} = 10 V, V_O = 9.5 V	−0.62		−0.50	−1.9		−0.35		mA
	V_{DD} = 15 V, V_O = 13.5 V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ} TRI-STATE® Output Current	V_{DD} = 15V, V_O = 0 V		±0.1		-10^{-5}	±0.1		±3.0	μA
	V_{DD} = 15 V, V_O = 15 V				10^{-5}				μA

DC Electrical Characteristics CD4512C (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20		0.005	20		150	μA
	V_{DD} = 10 V		40		0.010	40		300	μA
	V_{DD} = 15 V		80		0.015	80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (cont'd) CD4512C (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OL} Low Level Output Current	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$	0.23		0.20	0.78		0.16		mA
	$V_{DD} = 10\,V$, $V_O = 0.5\,V$	0.60		0.50	2.0		0.09		mA
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$	1.8		1.5	7.8		1.2		mA
I_{OH} High Level Output Current	$V_{DD} = 5.0\,V$, $V_O = 2.5\,V$	−0.23		−0.20	−1.7		−0.16		mA
	$V_{DD} = 10\,V$, $V_O = 9.5\,V$	−0.23		−0.20	−0.9		−0.16		mA
	$V_{DD} = 15\,V$, $V_O = 113.5\,V$	−0.69		−0.60	−3.5		−0.48		mA
I_{IN} Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$		−0.3		-10^{-5}	−0.3		−1.0	μA
	$V_{DD} = 15\,V$, $V_{IN} = 15\,V$		0.3		10^{-5}	0.3		1.0	μA
I_{OZ} TRI-STATE® Output Current	$V_{DD} = 15\,V$, $V_O = 0\,V$ or $15\,V$		±1.0		$\pm 10^{-5}$	±1.0		±7.5	μA

AC Electrical Characteristics $T_A = 25°C$, $t_r = t_f = 20\,ns$, $C_L = 15\,pF$

Parameter		Conditions	CD4512M			CD4512C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHL}	Propagation Delay High-to-Low Level	$V_{DD} = 5.0\,V$		225	500		225	750	ns
		$V_{DD} = 10\,V$		75	175		75	200	ns
		$V_{DD} = 15\,V$		57	130		57	150	ns
t_{PLH}	Propagation Delay Low-to-High Level	$V_{DD} = 5.0\,V$		225	500		225	750	ns
		$V_{DD} = 10\,V$		75	175		75	200	ns
		$V_{DD} = 15\,V$		57	130		57	150	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5.0\,V$		70	175		70	175	ns
		$V_{DD} = 10\,V$		35	75		35	75	ns
		$V_{DD} = 15\,V$		25	55		25	55	ns
t_{PHZ}, t_{PLZ}	Propagation Delay into TRI-STATE from Logic Level	$V_{DD} = 5.0\,V$		50	125		50	125	ns
		$V_{DD} = 10\,V$		25	75		25	75	ns
		$V_{DD} = 15\,V$		19	60		19	60	ns
t_{PZH}, t_{PZL}	Propagation Delay to Logic Level from TRI-STATE	$V_{DD} = 5.0\,V$		50	125		50	125	ns
		$V_{DD} = 10\,V$		25	75		25	75	ns
		$V_{DD} = 15\,V$		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		150			150		pF

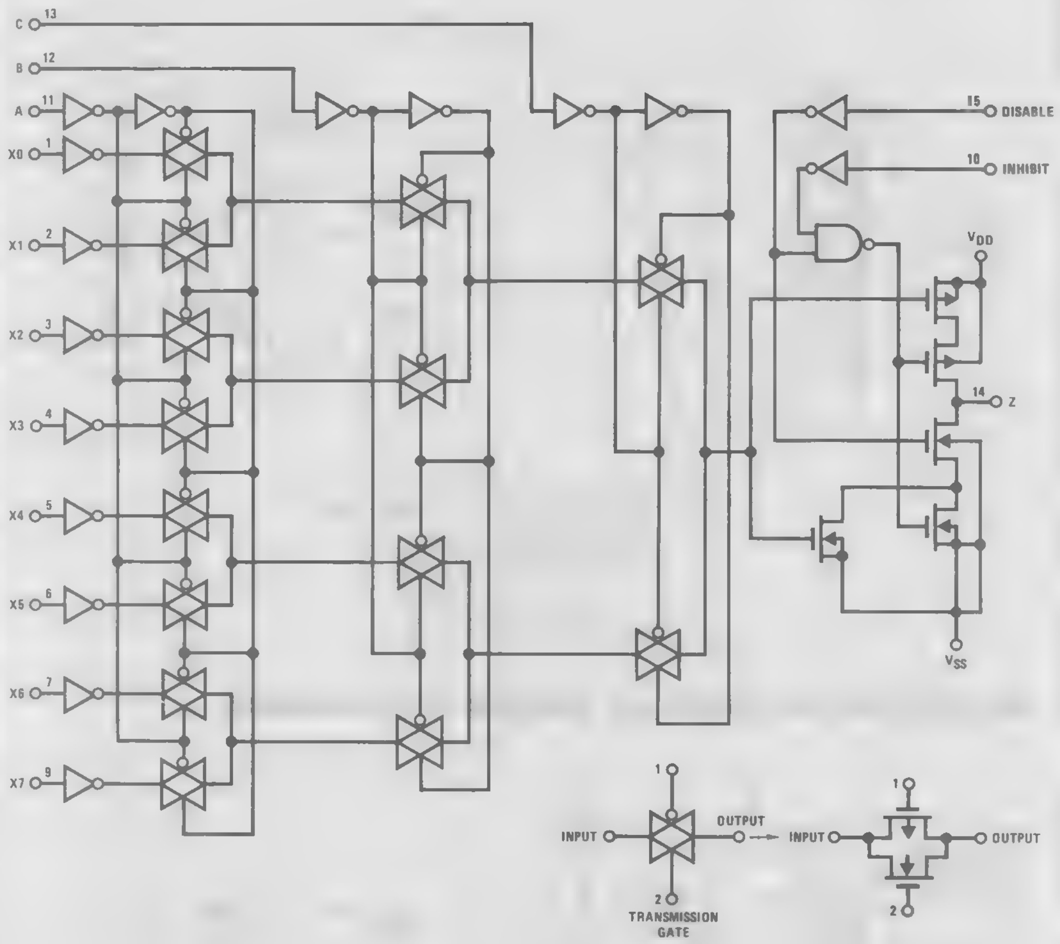
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\,V$ unless otherwise specified.

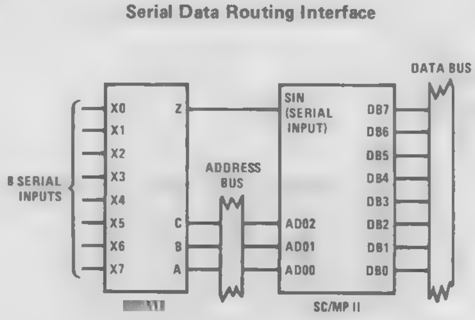
Note 3: Capacitance guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

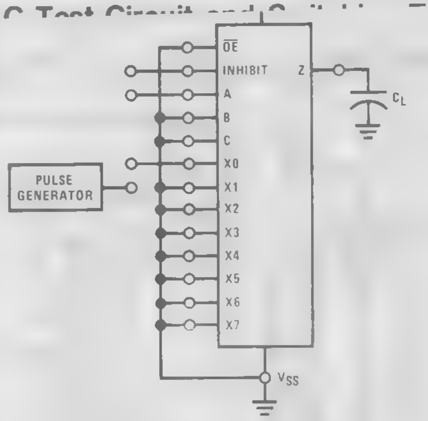
Logic Diagram

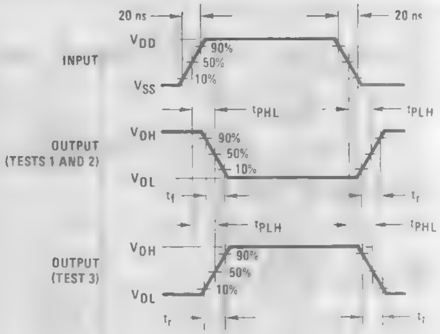


Typical Application


Serial Data Routing Interface

AC Test Circuit and Switching Time Waveforms

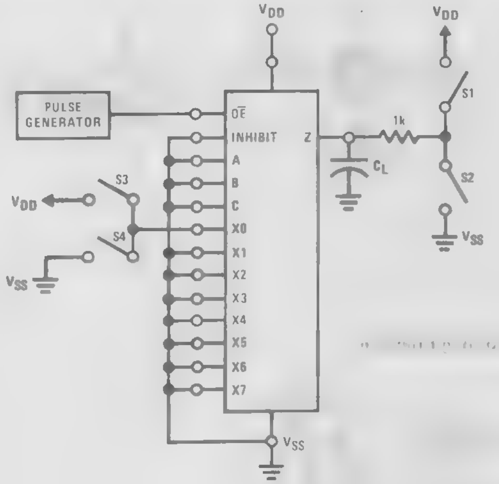


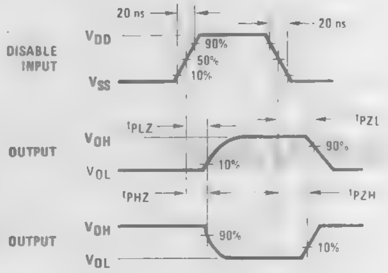


INPUT CONNECTIONS FOR t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms





SWITCH POSITIONS FOR TRI-STATE TEST

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

National Semiconductor

CD4512BM/CD4512BC 8-Channel Buffered Data Selector

General Description

The CD4512BM/CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ($\overline{OE}$) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ($\overline{OE}$) inputs allow normal operation.

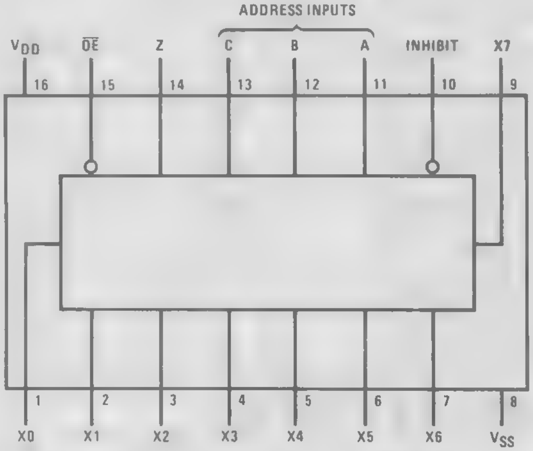
TRI-STATE is a trademark of National Semiconductor Corp

Features

- Wide supply voltage range 3.0 V-15 V
- High noise immunity 0.45 V_{DD} (typ.)
- TRI-STATE output
- Low quiescent power dissipation 0.25 μW/package (typ.) @ $V_{CC} = 5.0$ V
- Plug-in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

ADDRESS INPUTS			CONTROL INPUTS		OUTPUT
C	B	A	INHIBIT	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
Ø	Ø	Ø	1	0	0
Ø	Ø	Ø	[illegible]	1	Hi-Z

Ø = Don't care
Hi-Z = TRI-STATE® condition
Xn = Data at input n

3.0 to 15 VDC
V_{DD} Supply Voltage
V_{IN} Input Voltage
V_{DD} DC Supply Voltage
V_{DD} DC Supply Voltage −0.5 to +18 VDC
V_{IN} Input Voltage −0.5 to V_{DD} + 0.5 VDC

Absolute Maximum Ratings

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4512BM	55°C to +125°C
CD4512BC	40°C to +85°C

DC Electrical Characteristics CD4512BM (Note 2)

Parameter	Conditions	−55°C Min.	−55°C Max	25°C Min.	25°C Typ	25°C Max.	125°C Min	125°C Max	Units
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0		0.005	5.0		150	μA
	V_{DD} = 10 V		10		0.010	10		300	μA
	V_{DD} = 15 V		20		0.015	20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.78		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.0		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	7.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	0.64		0.51	1.7		0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	1.6		1.3	1.9		−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	4.2		3.4	3.5		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		0.1		10^{-5}	0.1		1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1		10	0.1		1.0	μA
I_{OZ} TRI-STATE* Output Current	V_{DD} = 15V, V_O = 0 V		±0.1		10^{-5}	±0.1		±3.0	μA
	V_{DD} = 15 V, V_O = 15 V				10^{-5}				μA

DC Electrical Characteristics CD4512BC (Note 2)

Parameter	Conditions	−40°C Min.	−40°C Max.	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20		0.005	20		150	μA
	V_{DD} = 10 V		40		0.010	40		300	μA
	V_{DD} = 15 V		80		0.015	80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (cont'd) CD4512BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OL} Low Level Output Current	$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.78		0.36		mA
	$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.0		0.9		mA
	$V_{DD}=15V$, $V_O=1.5V$	3.6		3.4	7.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD}=5.0V$, $V_O=2.5V$	−0.52		−0.44	−1.7		−0.36		mA
	$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−0.9		−0.9		mA
	$V_{DD}=15V$, $V_O=113.5V$	−3.6		−3.4	−3.5		−2.4		mA
I_{IN} Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
	$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA
I_{OZ} TRI-STATE® Output Current	$V_{DD}=15V$, $V_O=0V$ or $15V$		±1.0		$\pm 10^{-5}$	±1.0		±7.5	μA

AC Electrical Characteristics $T_A=25°C$, $t_r=t_f=20ns$, $C_L=15pF$

Parameter		Conditions	CD4512BM			CD4512BC			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHL}	Propagation Delay High-to-Low Level	$V_{DD}=5.0V$		225	500		225	750	ns
		$V_{DD}=10V$		75	175		75	200	ns
		$V_{DD}=15V$		57	130		57	150	ns
t_{PLH}	Propagation Delay Low-to-High Level	$V_{DD}=5.0V$		225	500		225	750	ns
		$V_{DD}=10V$		75	175		75	200	ns
		$V_{DD}=15V$		57	130		57	150	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0V$		70	175		70	175	ns
		$V_{DD}=10V$		35	75		35	75	ns
		$V_{DD}=15V$		25	55		25	55	ns
t_{PHZ}, t_{PLZ}	Propagation Delay into TRI-STATE from Logic Level	$V_{DD}=5.0V$		50	125		50	125	ns
		$V_{DD}=10V$		25	75		25	75	ns
		$V_{DD}=15V$		19	60		19	60	ns
t_{PZH}, t_{PZL}	Propagation Delay to Logic Level from TRI-STATE	$V_{DD}=5.0V$		50	125		50	125	ns
		$V_{DD}=10V$		25	75		25	75	ns
		$V_{DD}=15V$		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		150			150		pF

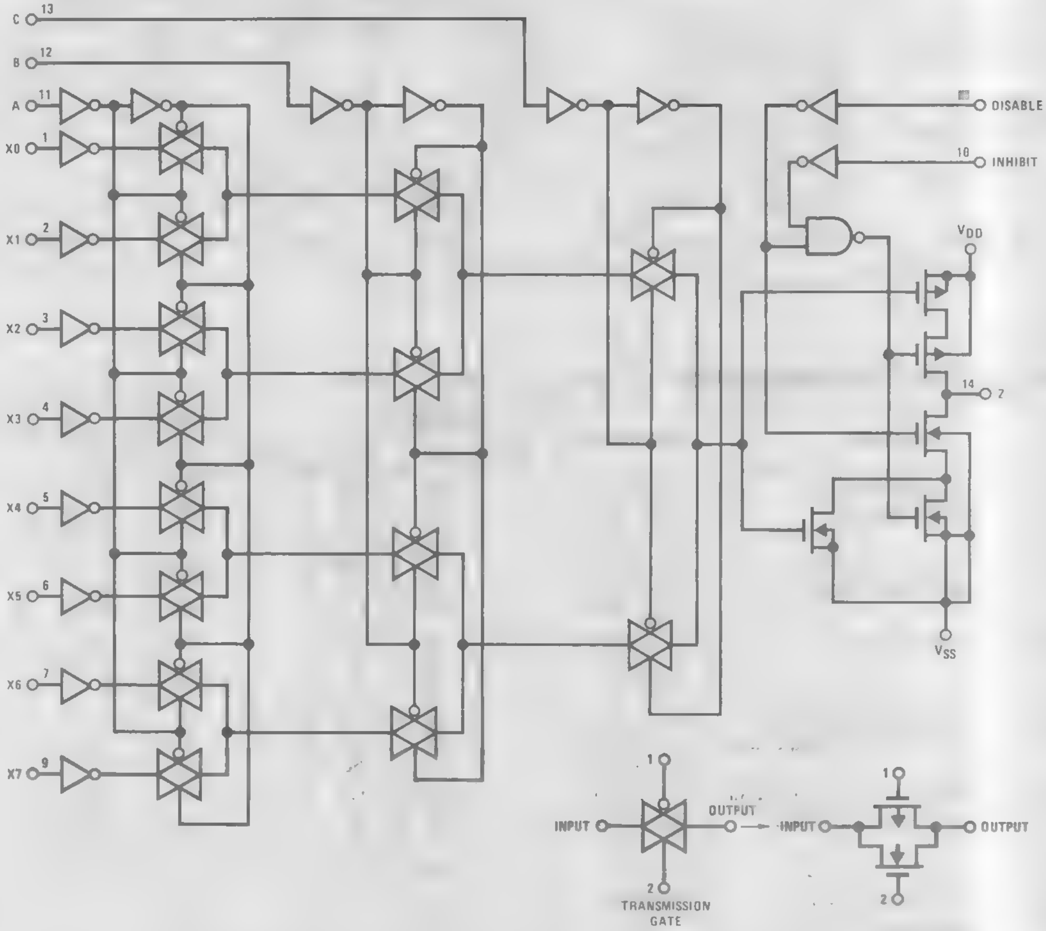
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: Capacitance guaranteed by periodic testing.

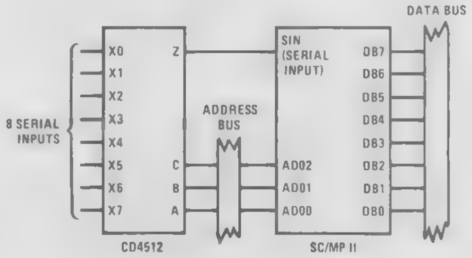
Note 4: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

Logic Diagram

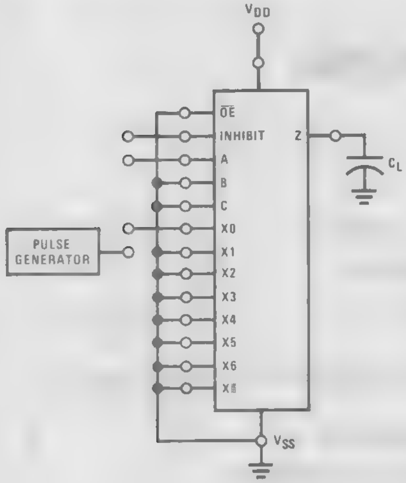


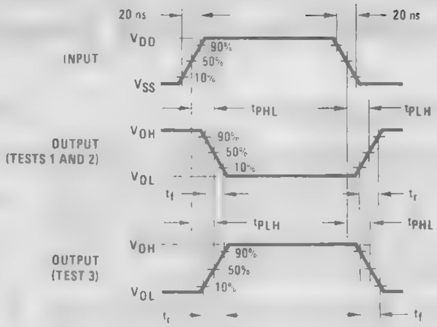
Typical Application

Serial Data Routing Interface



AC Test Circuit and Switching Time Waveforms

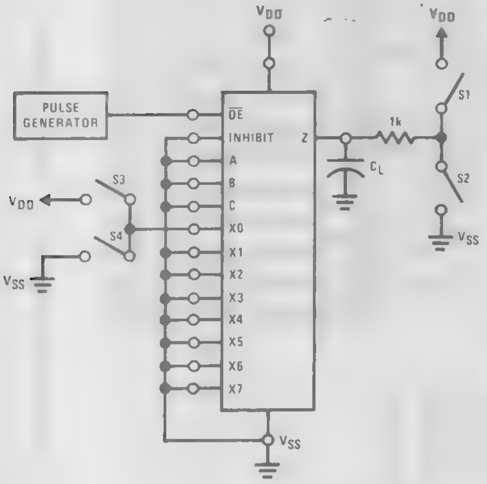


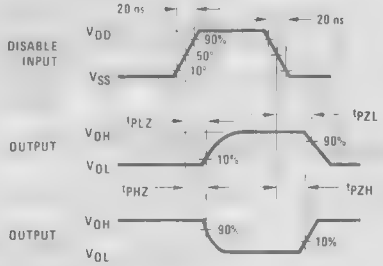


INPUT CONNECTIONS FOR t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms





SWITCH POSITIONS FOR TRI-STATE TEST

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

National Semiconductor

CD4514BM/CD4514BC, CD4515BM/CD4515BC 4-Bit Latched/4-to-16 Line Decoders

General Description

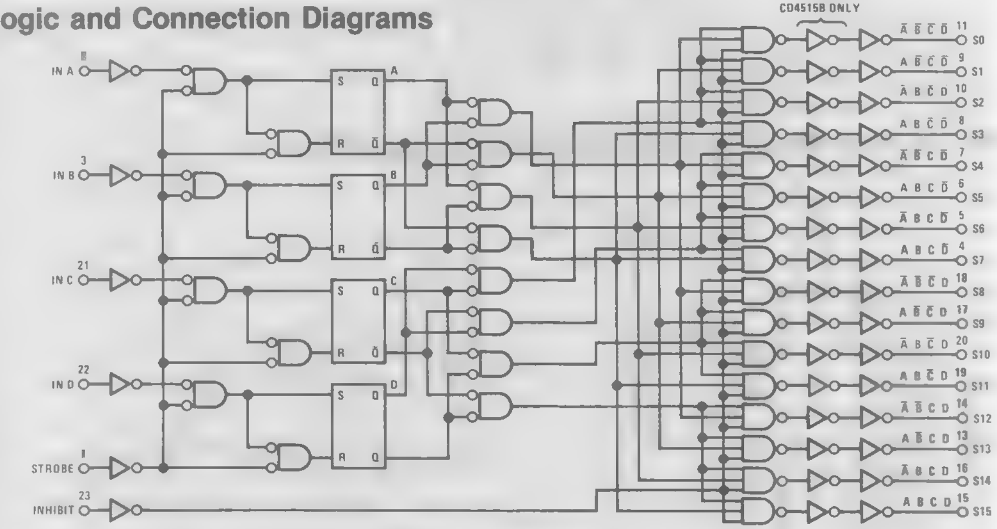
The CD4514B and CD4515B are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514B (output active high option) presents a logical "1" at the selected output, whereas the CD4515B presents a logical "0" at the selected output. The input latches are R–S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

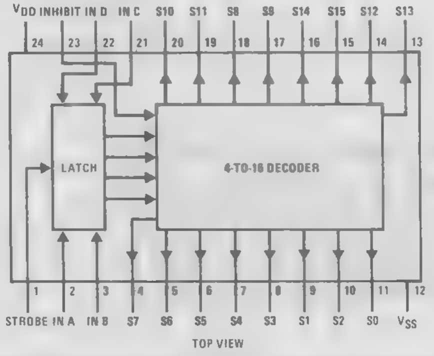
Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low quiescent power dissipation	0.025 μW/package (typ.) @ 5.0 V_{DC}
■ Single supply operation	
■ Input impedance = $10^{12}\Omega$ typically	
■ Plug-in replacement for MC14514, MC14515	

Logic and Connection Diagrams



Dual-In-Line Package



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4514BM, CD4515BM	−55°C to +125°C
CD4514BC, CD4515BC	−40°C to +85°C

DC Electrical Characteristics CD4514BM, CD4515BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.005	5.0		150	µA
		V_{DD} = 10V		10.0		0.010	10.0		300	µA
		V_{DD} = 15V		20.0		0.015	20.0		600	µA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_{IL} = 0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_{IL} = 0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\| < 1\ \mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\| < 1\ \mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.80		2.40		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.80		−2.40		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	µA

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DC Electrical Characteristics CD4514BC, CD4515BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	µA
		V_{DD} = 10V		40		0.010	40		300	µA
		V_{DD} = 15V		80		0.015	80		600	µA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V

DC Electrical Characteristics (Continued) CD4514BC, CD4515BC (Note 2)

PARAMETER		CONDITIONS	40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1,1	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

AC Electrical Characteristics All types C_L = 50 pF, T_A = 25°C, $t_r = t_f$ = 20 ns unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{THL}, t_{TLH}	Transition Times	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Times	V_{DD} = 5V		550	1100	ns
		V_{DD} = 10V		225	450	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Inhibit Propagation Delay Times	V_{DD} = 5V		400	800	ns
		V_{DD} = 10V		150	300	ns
		V_{DD} = 15V		100	200	ns
t_{SU}	Set Up Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
t_{WH}	Strobe Pulse Width	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 4)		150		pF
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and 'Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3. Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C&74C Family Characteristics application note, AN-90.

Truth Table

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS				SELECTED OUTPUT CD4514 = LOGIC "1" CD4515 = LOGIC "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't care

AC Test Circuit and Switching Time Waveforms

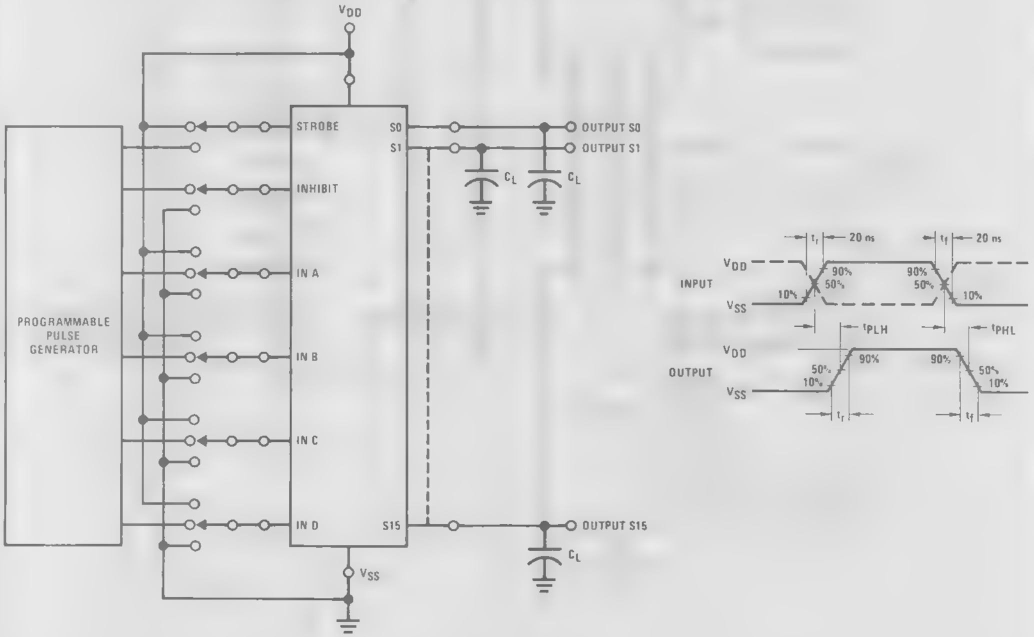


FIGURE 1

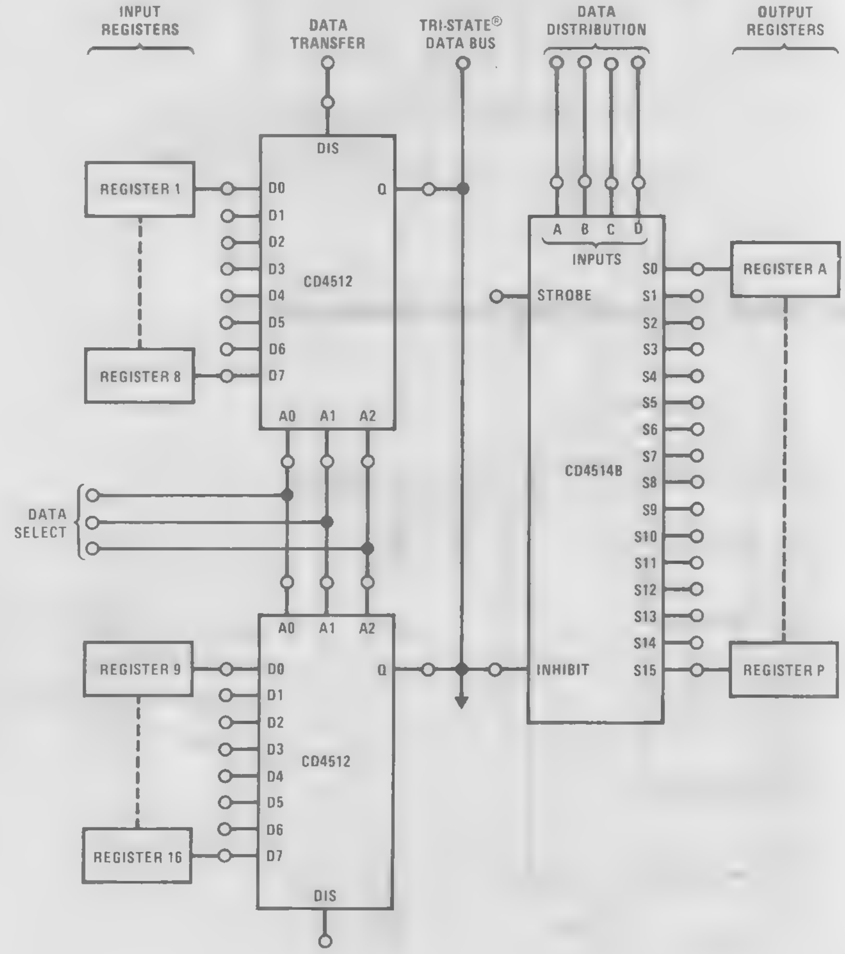
Applications

Two CD4512 8-channel data selectors are used here with the CD4514B 4-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a TRI-STATE® data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the 8 inputs on both CD4512 data selectors. One register is assigned to each input. The signals on A0, A1 and A2 choose 1-of-8 inputs for transfer out to the TRI-STATE data bus. A fourth signal, labelled Dis, disables one of the CD4512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1–16, the rate of transfer of the sequential information can also be varied. That is, if the CD4512 were addressed at a rate that is 8 times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the TRI-STATE bus is redistributed by the CD4514B 4-bit latch/decoder. Using the 4-bit address, INA–IND, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A–P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.



National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC Dual Synchronous Up Counters

General Description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 6 MHz counting rate (typ.) at V_{DD} = 10 V

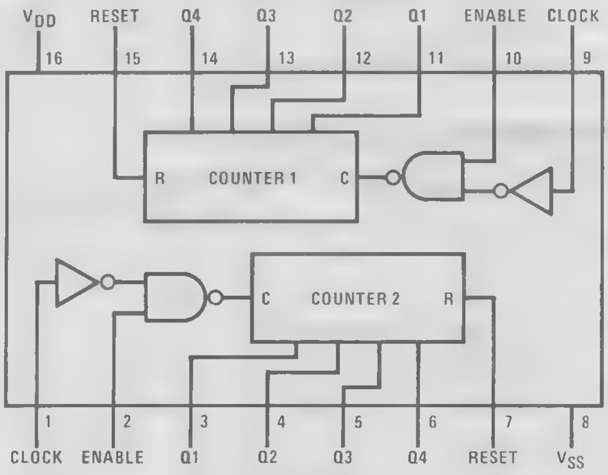
Truth Table

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment counter
0	↓	0	Increment counter
↓	X	0	No change
X	↑	0	No change
↑	0	0	No change
1	↓	0	No change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4518BM, CD4520BM	−55°C to +125°C
CD4518BC, CD4520BC	−40°C to +85°C

DC Electrical Characteristics CD4518BM/CD4520BM (Note 2)

PARAMETER		CONDITIONS	-55 C		25 C			125 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{5}	0.1		1.0	μA

DC Electrical Characteristics CD4518BC/CD4520BC (Note 2)

PARAMETER		CONDITIONS	40 C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0 01	20		150	μA
		V_{DD} = 10V		40		0 01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} − 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4518BC/CD4520BC (Note 2)

PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\,\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\,\mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
	$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
	$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
	$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN} Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
	$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, $t_r = t_f = 20\,ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock → Q	$V_{DD} = 5V$		325	650	ns
		$V_{DD} = 10V$		110	225	ns
		$V_{DD} = 15V$		85	170	ns
t_{PHL}	Propagation Delay Time Reset → Q	$V_{DD} = 5V$		220	560	ns
		$V_{DD} = 10V$		90	230	ns
		$V_{DD} = 15V$		65	160	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	1.5	3		MHz
		$V_{DD} = 10V$	3.0	6		MHz
		$V_{DD} = 15V$	4.0	8		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		35	70	ns
t_{RCL}, t_{FC}	Maximum Clock or Enable Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	10			μs
		$V_{DD} = 15V$	5			μs
t_{WH}, t_{WL}	Minimum Enable Pulse Width	$V_{DD} = 5V$		125	250	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}	Minimum Reset Pulse Width	$V_{DD} = 5V$		180	375	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Either Counter, (Note 3)		50		pF

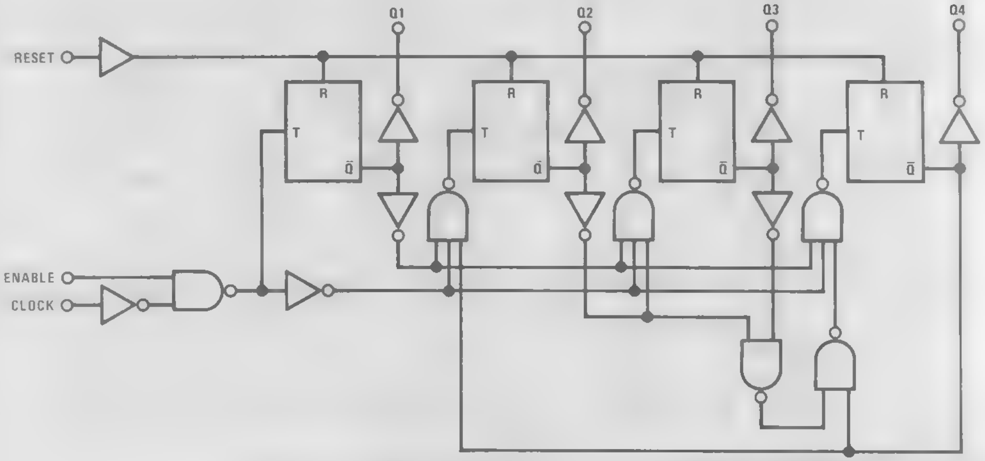
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

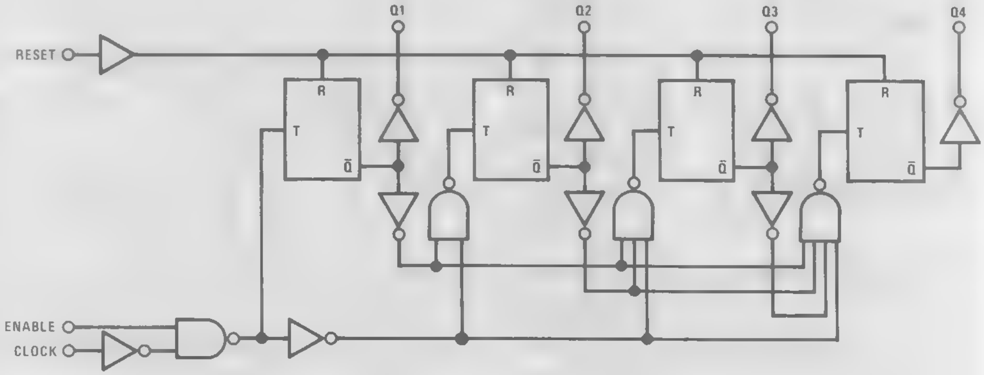
Note 3: C_{PD} determines the no load ac power consumption of a CMOS device. For a complete explanation, see "54C/74C Family Characteristics," application note AN-90.

Logic Diagrams

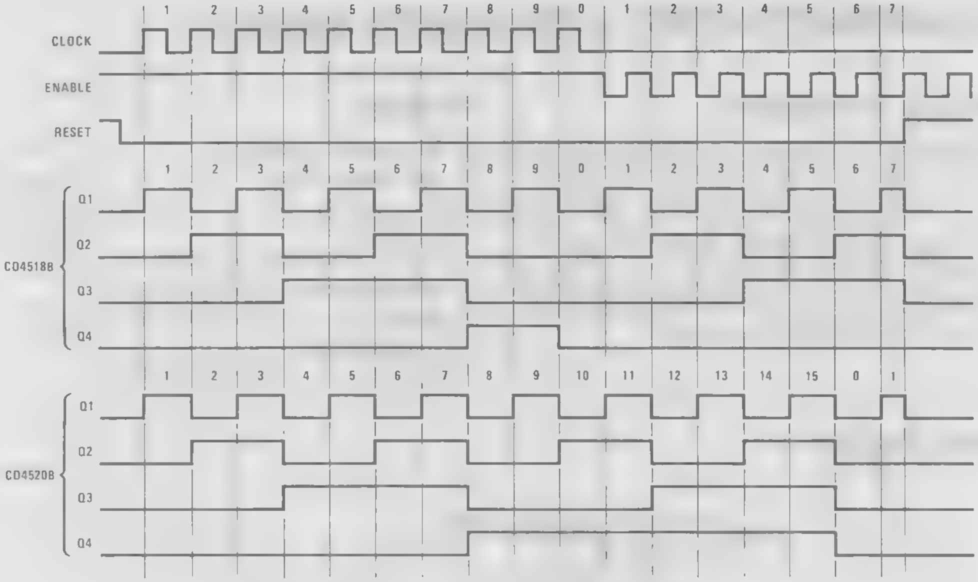
Decade Counter (CD4518B) 1/2 Device Shown



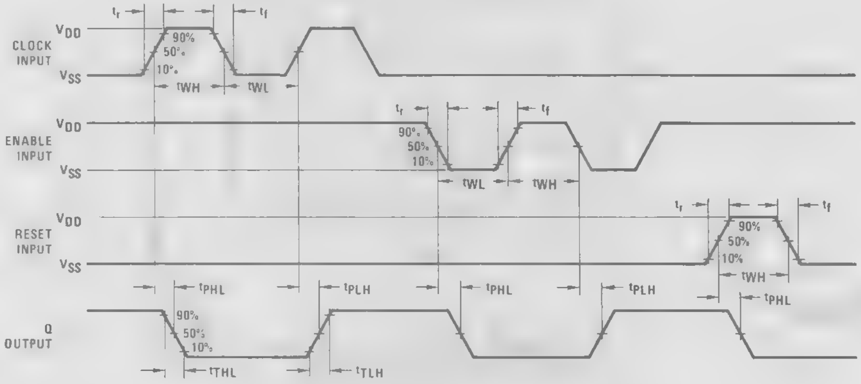
Binary Counter (CD4520B) 1/2 Device Shown



Timing Diagrams



Switching Time Waveforms



CD4519BM/CD4519BC 4-Bit AND/OR Selector

General Description

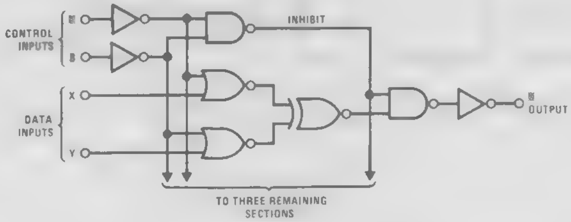
The CD4519B is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Depending on the condition of the control inputs, this part provides three functions in one package: a 4-bit AND/OR selector, a quad 2-channel Data Selector, or a Quad Exclusive-NOR Gate. The device outputs have equal source and sink current capabilities and conform to the standard B series output drive and supply voltage ratings.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

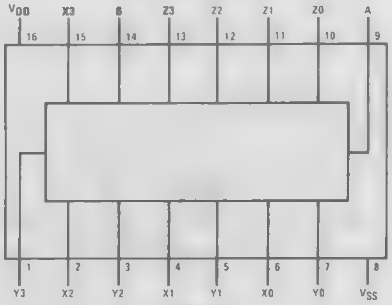
- ■ 5V–10V–15V parametric ratings
- ■ Symmetrical output characteristics
- ■ Maximum input leakage 1μA at 15V over full temperature range
- ■ Second source of Motorola MC14519

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \odot Y_n$

Note: $X_I \bigcirc Y_n = \overline{X_n \odot}\,\overline{Y_n} = X_nY_n + \overline{X}_n\overline{Y}_n$

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4519BM	−55°C to +125°C
CD4519BC	−40°C to +85°C

DC Electrical Characteristics CD4519BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.005	1		30	μA
		V_{DD} = 10V		2		0.006	2		60	μA
		V_{DD} = 15V		4		0.007	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4519BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4			4		30	μA
		V_{DD} = 10V		8			8		60	μA
		V_{DD} = 15V		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4519BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, $t_r = t_f = 20\,ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay High-to-Low Level or Low-to-High Level	*(Figure 1)*				
		$V_{DD} = 5V$		180	360	ns
		$V_{DD} = 10V$		75	150	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	*(Figure 1)*				
		$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input (Note 3)		5	7.5	pF
C_{pd}	Power Dissipation Capacity	Any Gate (Note 4)		25		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family characteristics application note AN-90.

AC Test Circuit and Switching Time Waveforms

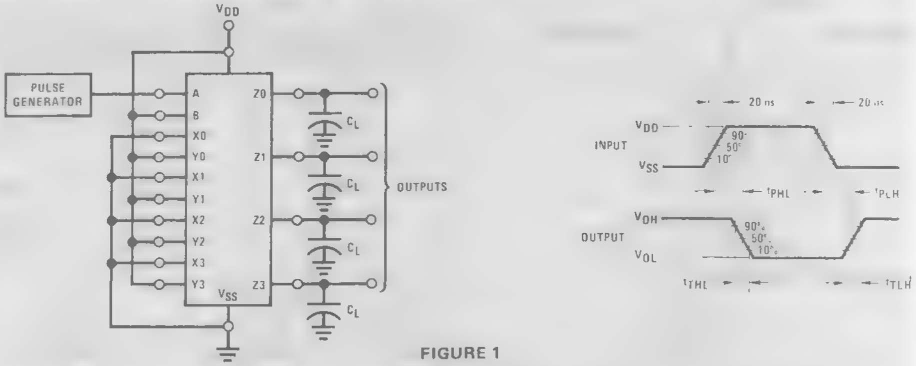
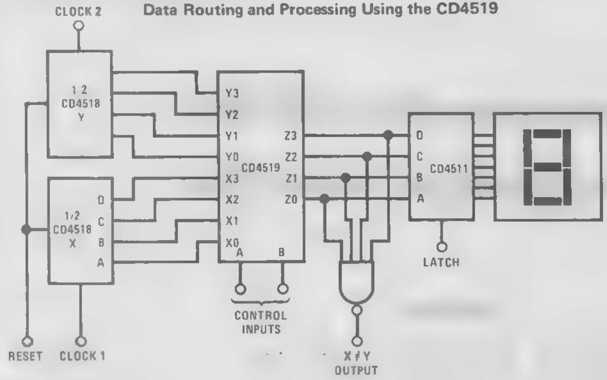


FIGURE 1

Typical Application

Data Routing and Processing Using the CD4519



CONTROL INPUTS		FUNCTION
A	B	
0	0	Display Zero
0	1	Display Counter Y
1	0	Display Counter X
1	1	Compare Counters

CD4522BM/CD4522BC Programmable Divide-By-N 4-Bit BCD Counter

CD4526BM/CD4526BC Programmable Divide-By-N 4-Bit Binary Counter

General Description

The CD4522BM/CD4522BC, CD4526BM/CD4526BC are CMOS programmable cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications, the "0" output is applied to the Preset Enable input. For multi-stage applications, the "0" output is used in conjunction with the CF (Cascade Feedback) input to perform the divide-by-N function. The "0" output is normally at logical "0" level; it will go to a logical "1" state only when the counter is at its terminal count (0000) and if CF is at logical "1" level. Thus, CF acts as an active low inhibit for the "0" output. This feature allows cascade divide-by-N operations with no additional gate required (see Applications section). The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

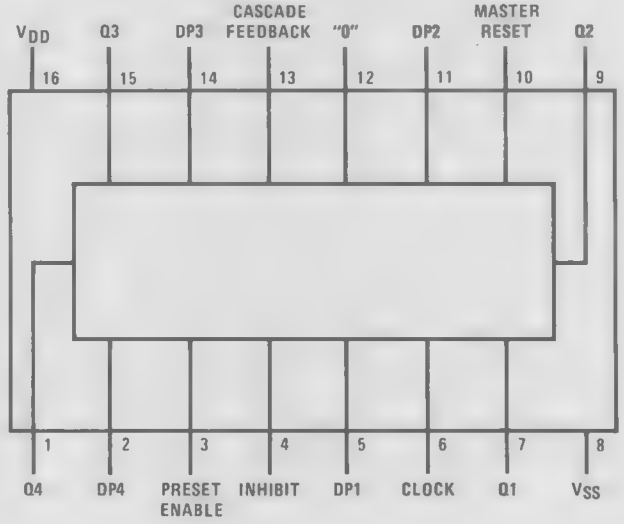
- Wide supply voltage range 3.0 V to 18 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Quiescent current = 5 nA/package (typ.) @ V_{DD} = 5.0 V
- Internally synchronous for high internal and external speed
- Logic edge-clocked design—incremented on positive transition of Clock or negative transition of Clock Inhibit
- Medium speed 7.7 MHz (typ.) @ V_{DD} = 10 V
- Asynchronous Preset Enable

Applications

- Programmable down counter
- Programmable frequency divider
- Frequency synthesizers
- Phase-locked loops

Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4522BM, CD4526BM	−55°C to +125°C
CD4522BC, CD4526BC	−40°C to +85°C

DC Electrical Characteristics CD4522BM, CD4526BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.010	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Continued) CD4522BC, CD4526BC (Note 2)

PARAMETER		CONDITIONS	40 C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		1.1	−2.25		0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		0.3		10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PHL} & t_{PLH}	Propagation Delay Time From Clock to Q Outputs	V_{DD} = 5V		350	825	ns
		V_{DD} = 10V		130	345	ns
		V_{DD} = 15V		90	240	ns
t_{PHL} & t_{PLH}	Propagation Delay Time From Clock to "0" Output	V_{DD} = 5V		200	500	ns
		V_{DD} = 10V		80	250	ns
		V_{DD} = 15V		60	190	ns
PW_C	Minimum Clock Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
f_{CL}	Maximum Clock Pulse Frequency	V_{DD} = 5V	1.5	2.9		MHz
		V_{DD} = 10V	3.0	7.7		MHz
		V_{DD} = 15V	4.0	11		MHz
t_{rCL} & t_{fCL}	Maximum Clock or Inhibit Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{HOLD}	Hold Time	V_{DD} = 5V		40	125	ns
		V_{DD} = 10V		25	50	ns
		V_{DD} = 15V		20	40	ns
PW_{PE}	Minimum Preset Enable Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
PW_{MR}	Minimum Master Reset Pulse Width	V_{DD} = 5V		160	350	ns
		V_{DD} = 10V		75	180	ns
		V_{DD} = 15V		50	120	ns
C_{IN}	Input Capacitance	(Note 3)		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

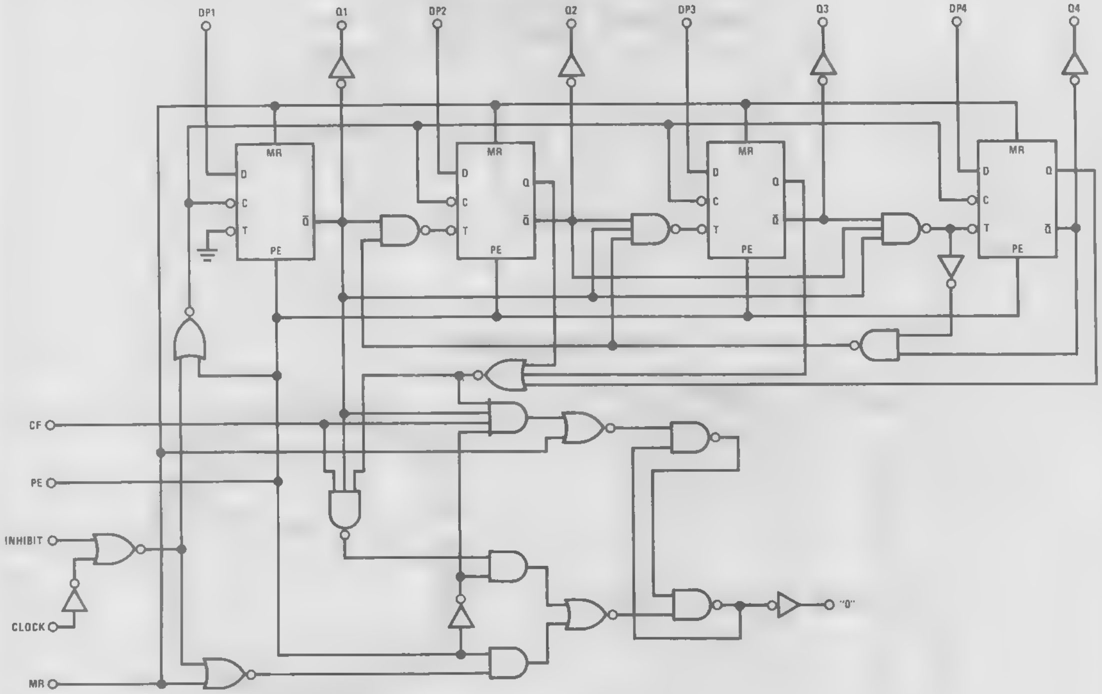
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

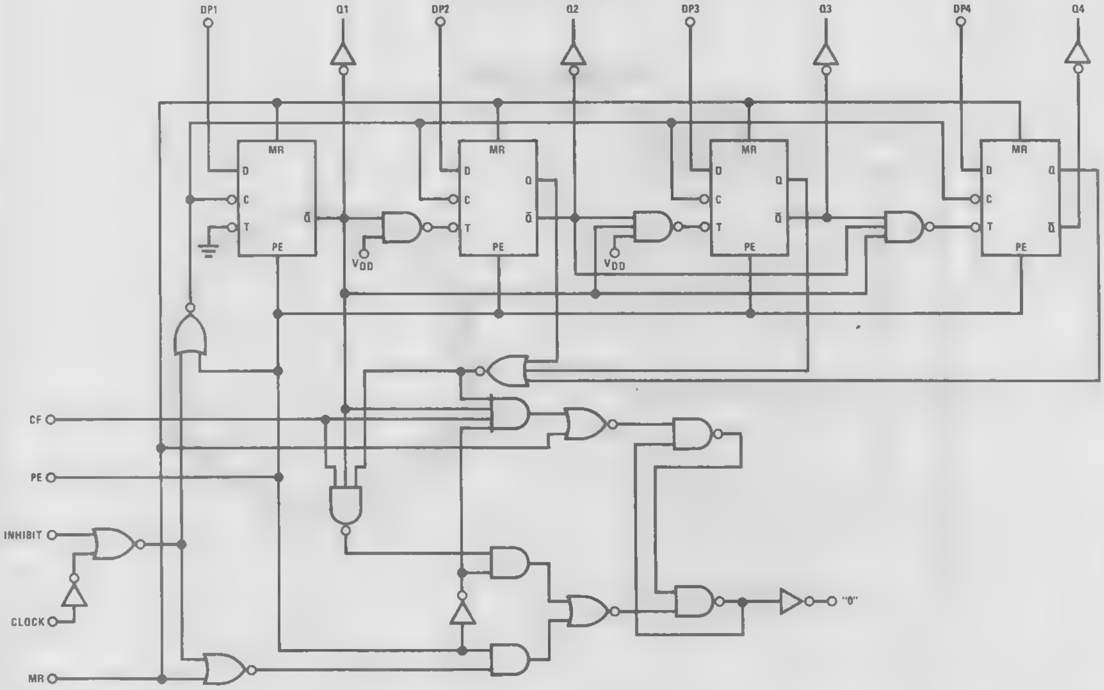
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Logic Diagrams

CD4522BM/CD4522BC



CD4526BM/CD4526BC



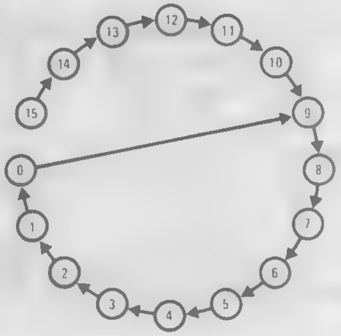
Truth Tables and Count Sequences

Both Types

CLOCK	INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
0	0	0	0	No count
↑	0	0	0	Count 1
X	1	0	0	No count
1	↓	0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

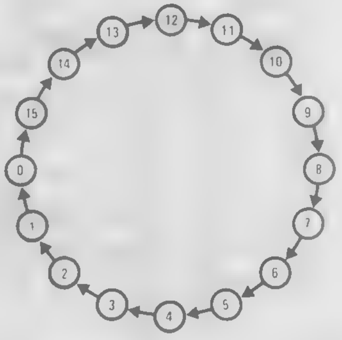
CD4522BM/CD4522BC

COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



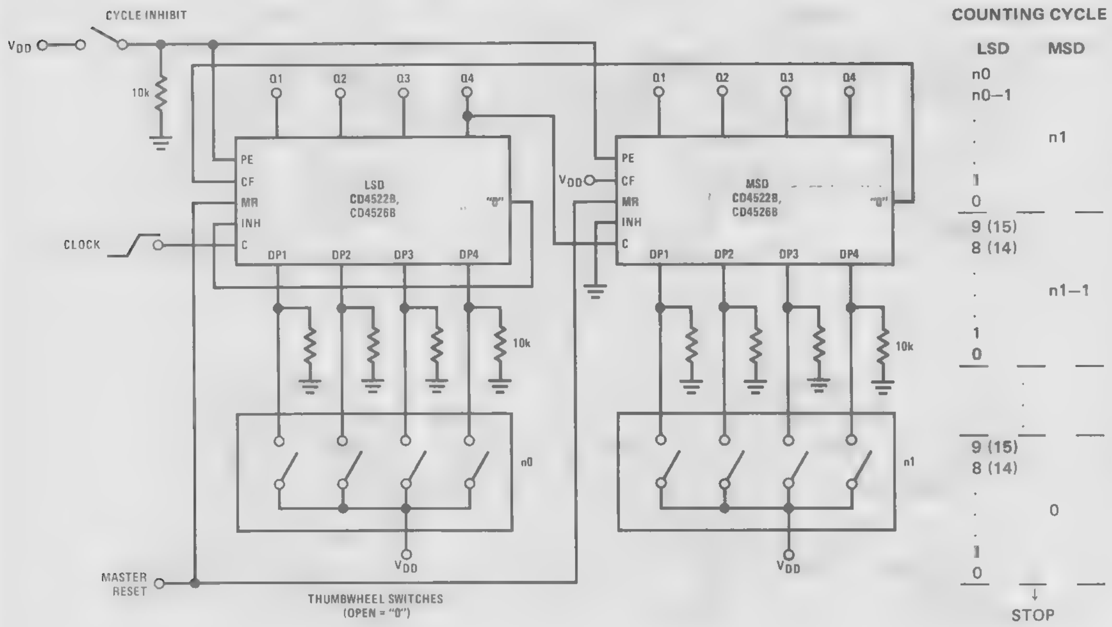
CD4526BM/CD4526BC

COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

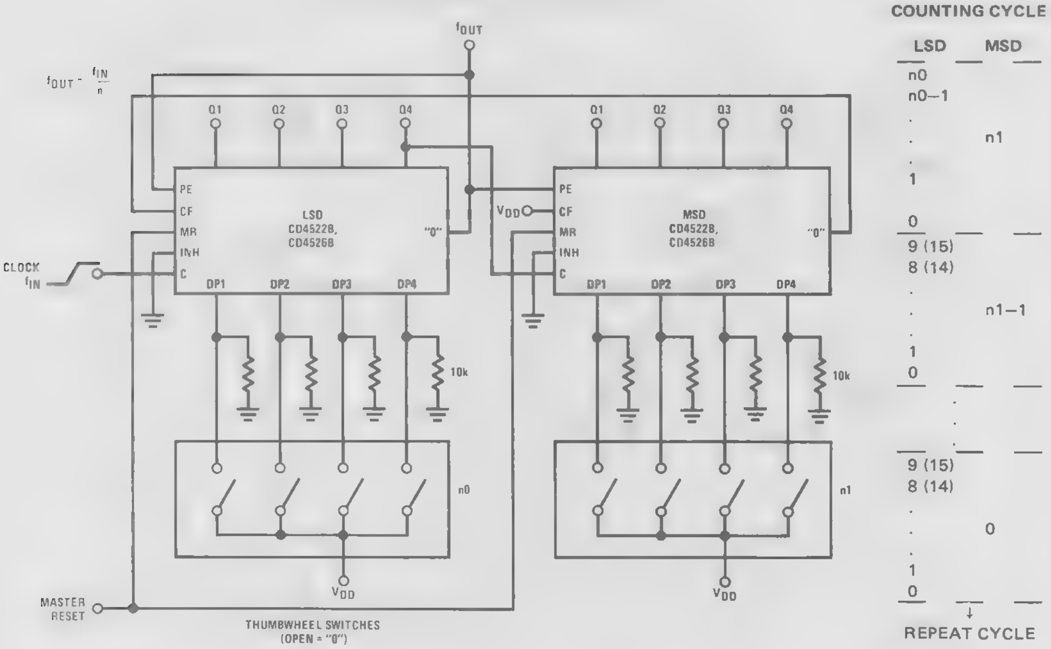


Typical Applications

2-Stage Programmable Down Counter



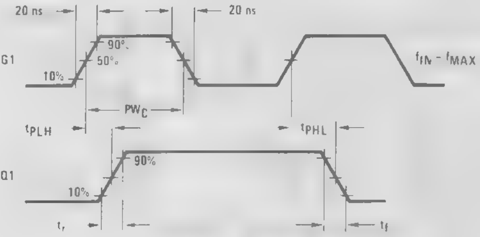
2-Stage Programmable Frequency Divider



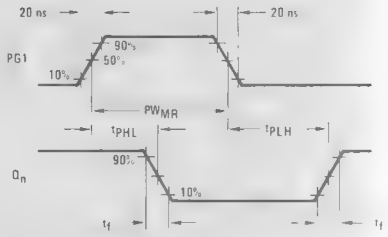
Note. When cascading more than 2 packages, tie "0" output of the nth package to CF input of the (n–1)th package for all n = 2, 3.

Switching Time Waveforms

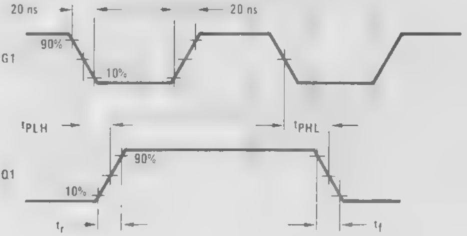
Test No. 1



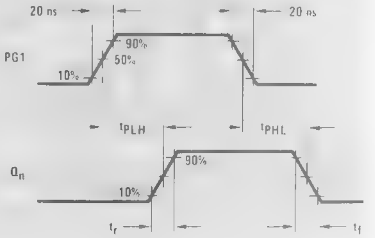
Test No. 4



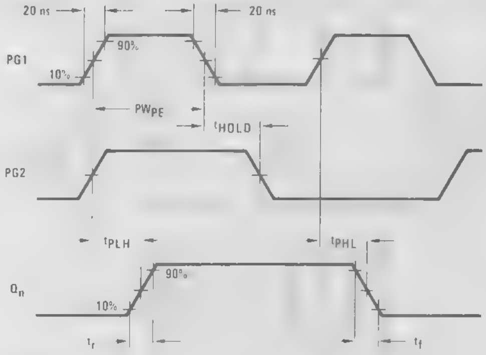
Test No. 2



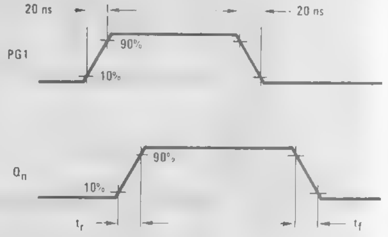
Tests No. 5 and 7



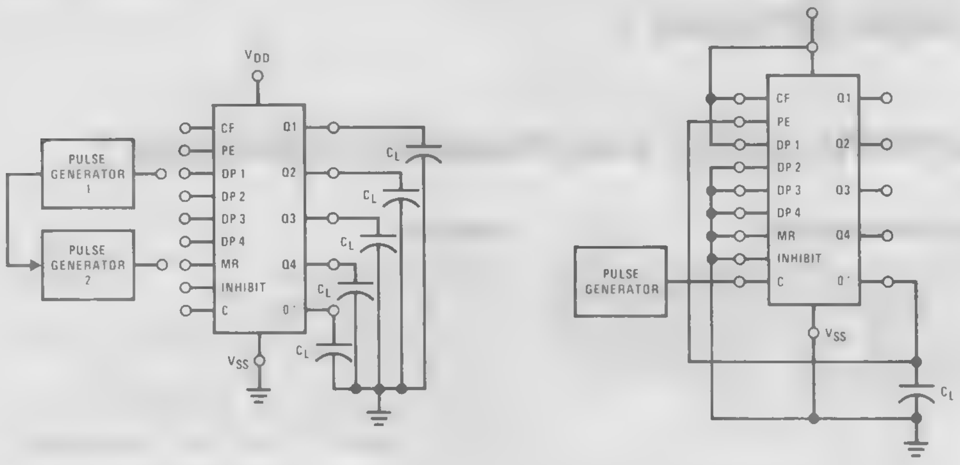
Test No. 3



Test No. 6



AC Test Circuits



a) Tests No. 1–6

b) Test No. 7

FIGURE 1. Test Circuit

Test Conditions

TABLE I

CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	DP_n	CF	OUTPUT
t_r, t_f, t_{PLH}, t_{PHL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{MAX}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{HOLD}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	*Fig. 1b*	V_{SS}	*Fig. 1b*	V_{DD}	"0"

CD4528BM/CD4528BC Dual Monostable Multivibrator

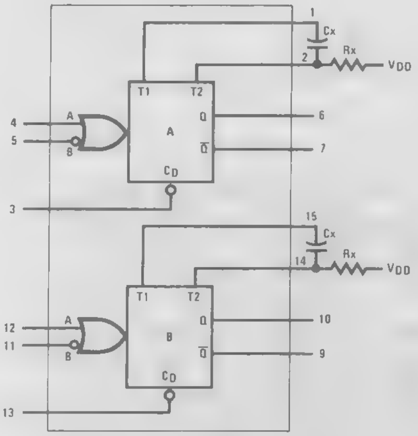
General Description

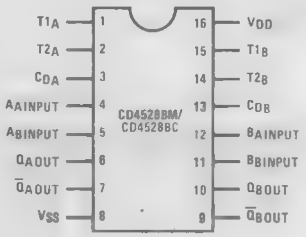
The CD4528B is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or falling edge of an input pulse, resulting in an output pulse over a wide range of widths. Pulse duration and accuracy are determined by external timing components R_X and C_X.

Features

- Wide supply voltage range 3.0 V to 18 V
- Separate reset available
- Quiescent current = 5.0 nA/package (typ.) at 5.0 V_{DC}
- Diode protection on all inputs
- Triggerable from leading or trailing edge pulse
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range

Connection Diagrams





Truth Tables

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⊔
H	↑	H	⎍	⊔

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}, DC Supply Voltage	−0.5 VDC to +18 VDC
V_{IN}, Input Voltage, All Inputs	−0.5 VDC to V_{DD} +0.5 V_{DC}
T_S, Storage Temperature Range	−65°C to +150°C
P_D, Package Dissipation	500 mW
T_L, Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD}, DC Supply Voltage	3V to 15V
V_{IN}, Input Voltage	0V to V_{DD} V_{DC}
T_A, Operating Temperature Range	
CD4528BM	−55°C to +125°C
CD4528BC	−40°C to +85°C

DC Electrical Characteristics CD4528BM (Note 2)

Parameter	Conditions	−55°C		+25°C			+125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		5	0.005		5		150	μA
	V_{DD} = 10V		10	0.010		10		300	μA
	V_{DD} = 15V		20	0.015		20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
	V_{DD} = 10V		0.05			0.05		0.05	V
	V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.36		−0.14		mA
	V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.9		−0.35		mA
	V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4528BC (Note 2)

Parameter		Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.005	20		150	μA
		$V_{DD} = 10V$		40		0.010	40		300	μA
		$V_{DD} = 15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 0.5V$ or $4.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.2		−0.16	−0.36		−0.12		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.5		−0.4	−0.9		−0.3		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

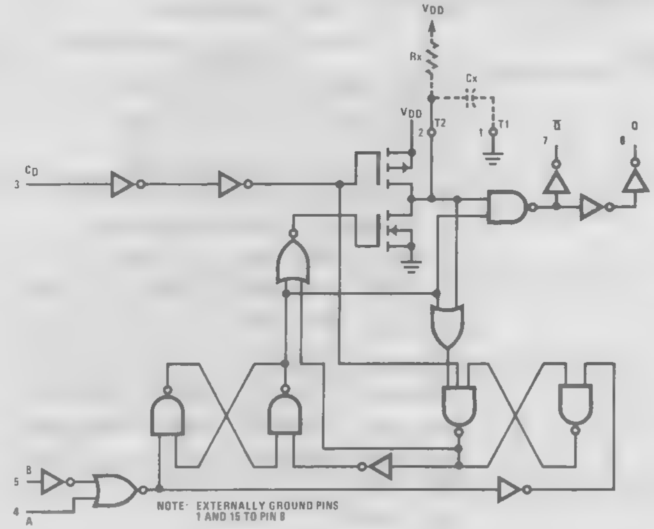
Note 2: $V_{SS} = 0V$ unless otherwise specified.

AC Electrical Characteristics CD4528BM

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, Input $t_r = t_f = 20\,ns$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output Rise Time	$t_r = (3.0\,ns/pF)C_L + 30\,ns$, $V_{DD} = 5.0V$		180	400	ns
	$t_r = (1.5\,ns/pF)C_L + 15\,ns$, $V_{DD} = 10.0V$		90	200	ns
	$t_r = (1.1\,ns/pF)C_L + 10\,ns$, $V_{DD} = 15.0V$		65	160	ns
Output Fall Time	$t_f = (1.5\,ns/pF)C_L + 25\,ns$, $V_{DD} = 5.0V$		100	200	ns
	$t_f = (0.75\,ns/pF)C_L + 12.5\,ns$, $V_{DD} = 10.0V$		50	100	ns
	$t_f = (0.55\,ns/pF)C_L + 9.5\,ns$, $V_{DD} = 15.0V$		35	80	ns
Turn-Off, Turn-On Delay A or B to Q or $\bar{Q}$ $Cx = 15\,pF$, $Rx = 5.0\,k\Omega$	$t_{PLH}, t_{PHL} = (1.7\,ns/pF)C_L + 240\,ns$, $V_{DD} = 5.0V$		230	500	ns
	$t_{PLH}, t_{PHL} = (0.66\,ns/pF)C_L + 8\,ns$, $V_{DD} = 10.0V$		100	250	ns
	$t_{PLH}, t_{PHL} = (0.5\,ns/pF)C_L + 65\,ns$, $V_{DD} = 15.0V$		65	150	ns
Turn-Off, Turn-On Delay A or B to Q or $\bar{Q}$ $Cx = 100\,pF$, $Rx = 10\,k\Omega$	$t_{PLH}, t_{PHL} = 1.7\,ns/pF)C_L + 620\,ns$, $V_{DD} = 5.0V$		230	500	ns
	$t_{PLH}, t_{PHL} = 0.66\,ns/pF)C_L + 257\,ns$, $V_{DD} = 10.0V$		100	250	ns
	$t_{PLH}, t_{PHL} = (0.5\,ns/pF)C_L + 185\,ns$, $V_{DD} = 15.0V$		65	150	ns
Minimum Input Pulse Width A or B $Cx = 15\,pF$, $Rx = 5.0\,k\Omega$	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
$Cx = 1000\,pF$, $Rx = 10\,k\Omega$	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
Output Pulse Width Q or Q For $Cx < 0.01\,\mu F$ (see graph for appropriate V_{DD} level) $Cx = 15\,pF$, $Rx = 5.0\,k\Omega$	$V_{DD} = 5.0V$		550		ns
	$V_{DD} = 10.0V$		350		ns
	$V_{DD} = 15.0V$		300		ns
For $Cx > 0.01\,\mu F$ use $PW_{out} = 0.2\,Rx\,Cx\,\ln[V_{DD} - V_{SS}]$ $Cx = 10{,}000\,pF$, $Rx = 10\,k\Omega$	$V_{DD} = 5.0V$	15	29	45	μs
	$V_{DD} = 10.0V$	10	37	90	μs
	$V_{DD} = 15.0V$	15	42	95	μs
Pulse Width Match Between Circuits in the Same Package $Cx = 10{,}000\,pF$, $Rx = 10\,k\Omega$	$V_{DD} = 5.0V$		6	25	%
	$V_{DD} = 10.0V$		8	35	%
	$V_{DD} = 15.0V$		8	35	%
Reset Propagation Delay, t_{PLH}, t_{PHL} $Cx = 15\,pF$, $Rx = 5.0\,k\Omega$	$V_{DD} = 5.0V$		325	600	ns
	$V_{DD} = 10.0V$		90	225	ns
	$V_{DD} = 15.0V$		60	170	ns
$Cx = 1000\,pF$, $Rx = 10\,k\Omega$	$V_{DD} = 5.0V$		7.0		μs
	$V_{DD} = 10.0V$		6.7		μs
	$V_{DD} = 15.0V$		6.7		μs
Minimum Retrigger Time $Cx = 15\,pF$, $Rx = 5.0\,k\Omega$	$V_{DD} = 5.0V$		0		
	$V_{DD} = 10.0V$		0		
	$V_{DD} = 15.0V$		0		
$Cx = 1000\,pF$, $Rx = 10\,k\Omega$	$V_{DD} = 5.0V$		0		
	$V_{DD} = 10.0V$		0		
	$V_{DD} = 15.0V$		0		

Logic Diagram (½ of Device Shown)



NOTE: EXTERNALLY GROUND PINS 1 AND 15 TO PIN 8

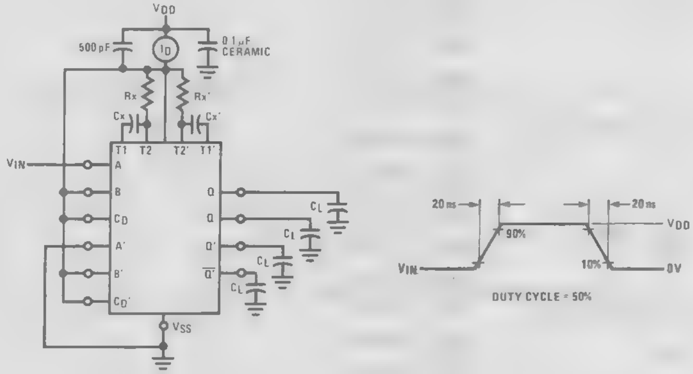
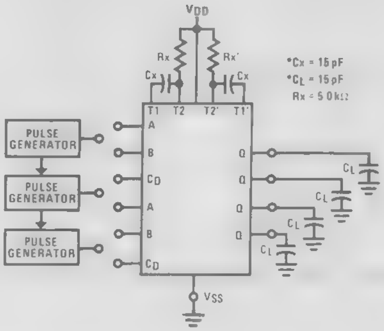


Figure 1. Power Dissipation Test Circuit and Waveforms



*Cx = 15 pF
*CL = 15 pF
Rx = 5.0 kΩ

Input Connections

Characteristics	C_D	A	B
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, PW_{in}	PG3	PG1	PG2

*INCLUDES CAPACITANCE OF PROBES, WIRING, AND FIXTURE PARASITIC

NOTE: AC TEST WAVEFORMS FOR PG1, PG2, AND PG3 ON NEXT PAGE.

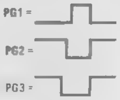


Figure 2. AC Test Circuit

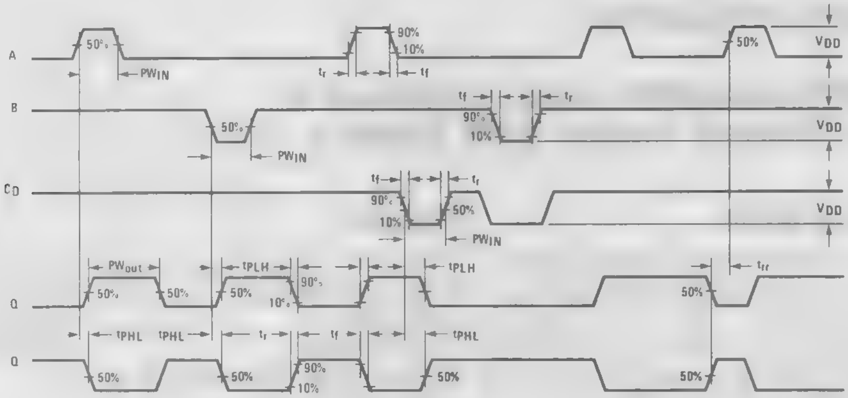


Figure 3. AC Test Waveforms

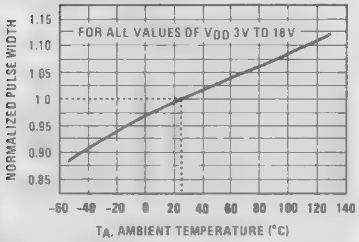


Figure 4. Normalized Pulse Width vs Temperature

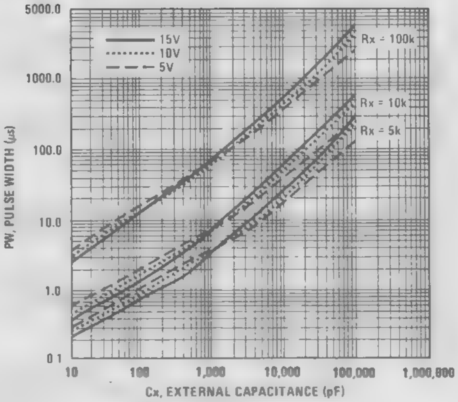


Figure 5. Pulse Width vs Cx

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single binary to 1-of-8 decoder applications.

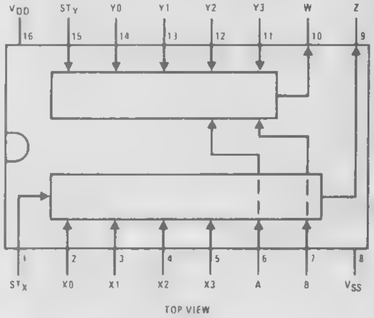
Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low quiescent power dissipation 0.005 μW/package (typ.) @ 5.0 V_{DC}
- 10 MHz frequency operation (typ.)
- Data paths are bidirectional
- Linear ON resistance [120 Ω (typ.) @ 15 V]
- TRI-STATE® outputs (high impedance disable strobe)
- Plug-in replacement for MC14529B

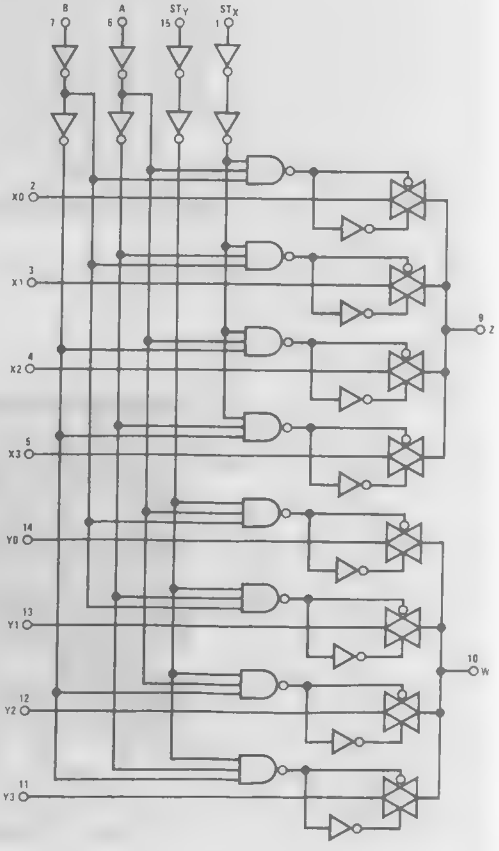
TRI-STATE is a registered trademark of National Semiconductor Corp.

Connection Diagram

Dual-In-Line Package



Logic Diagram



Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE®)		

X = Don't care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4529BM	−55°C to +125°C
CD4529BC	−40°C to +85°C

DC Electrical Characteristics CD4529BM (Note 2)

PARAMETER		CONDITIONS	−55 C		25 C			125 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.001	1.0		60	µA
		V_{DD} = 10V		1.0		0.002	1.0		60	µA
		V_{DD} = 15V		2.0		0.003	2.0		120	µA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.1		-10^{-5}	−0.1		1.0	µA
		V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	µA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		400		165	480		640	Ω
		V_{IN} = −5V		400		100	480		640	Ω
		V_{IN} = ±0.25V		400		155	480		640	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		240		135	270		400	Ω
		V_{IN} = −7.5V		240		75	270		400	Ω
		V_{IN} = ±0.25V		240		100	270		400	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		400		165	480		640	Ω
		V_{IN} = 0.25V		400		100	480		640	Ω
		V_{IN} = 5.6V		400		160	480		640	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		400	Ω
		V_{IN} = 0.25V		250		75	270		400	Ω
		V_{IN} = 9.3V		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −5V, V_{DD} = 5V, V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±2500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2)

PARAMETER		CONDITIONS	-40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.001	5.0		70	μA
		V_{DD} = 10V		5.0		0.002	5.0		70	μA
		V_{DD} = 15V		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.00		4.95		V
		V_{DD} = 10V	9.95		9.95	10.00		9.95		V
		V_{DD} = 15V	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		410		165	480		560	Ω
		V_{IN} = −5V		410		100	480		560	Ω
		V_{IN} = ±0.25V		410		155	480		560	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		250		135	270		350	Ω
		V_{IN} = −7.5V		250		75	270		350	Ω
		V_{IN} = ±0.25V		250		100	270		350	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		410		165	480		560	Ω
		V_{IN} = 0.25V		410		100	480		560	Ω
		V_{IN} = 5.6V		410		160	480		560	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		350	Ω
		V_{IN} = 0.25V		250		75	270		350	Ω
		V_{IN} = 9.3V		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V								
		V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±500	nA
		V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V								
		V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±1000	nA
		V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

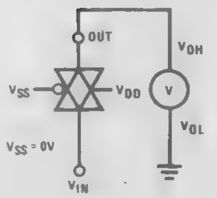
Note 3: Switch OFF is defined as $\lvert I_O \rvert \leq 10\ \mu A$, switch ON as defined by R_{ON} specification.

AC Electrical Characteristics CD4529BM/CD4529BC

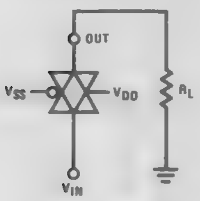
$T_A = 25°C$, $R_L = 1\ k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		10	20	ns
		$V_{DD} = 15V$		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	$V_{IN} = V_{DD}$ or V_{SS}, $C_L = 50$ pF				
		$V_{IN} \leq 10V$				
		$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		5		MHz
		$V_{DD} = 10V$		10		MHz
		$V_{DD} = 15V$		12		MHz
	Crosstalk, Control to Output	$R_{OUT} = 10\ k\Omega$, $C_L = 50$ pF, $V_{SS} = 0$				
		$V_{DD} = 5V$		5.0		mV
		$V_{DD} = 10V$		5.0		mV
		$V_{DD} = 15V$		5.0		mV
	Noise Voltage	f = 100 Hz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		24		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		25		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		30		$nV/\sqrt{cycle}$
		f = 100 kHz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		15		$nV/\sqrt{cycle}$
	Sine Wave (Distortion)	$V_{IN} = 1.77$Vrms Centered at 0V, $R_L = 10\ k\Omega$, f = 1 kHz, $V_{SS} = -5V$, $V_{DD} = 5V$		0.36		%
I_{LOSS}	Insertion Loss, $I_{LOSS} = 20\ \text{Log}_{10}\ \frac{V_{OUT}}{V_{IN}}$	$V_{IN} = 1.77$Vrms Centered at 0V, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$		2.0		dB
		$R_L = 10\ k\Omega$		0.8		dB
		$R_L = 100\ k\Omega$		0.25		dB
		$R_L = 1\ M\Omega$		0.01		dB
BW	Bandwidth, −3 dB	$V_{IN} = 1.77$Vrms Centered at 0 Vdc, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	35			MHz
		$R_L = 10\ k\Omega$	28			MHz
		$R_L = 100\ k\Omega$	27			MHz
		$R_L = 1\ M\Omega$	26			MHz
	Feedthrough and Crosstalk, $20\ \text{Log}_{10}\ \frac{V_{OUT}}{V_{IN}} = -50$ dB	$V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	850			kHz
		$R_L = 10\ k\Omega$	100			kHz
		$R_L = 100\ k\Omega$	12			kHz
		$R_L = 1\ M\Omega$	1.5			kHz

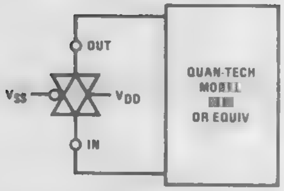
Output Voltage



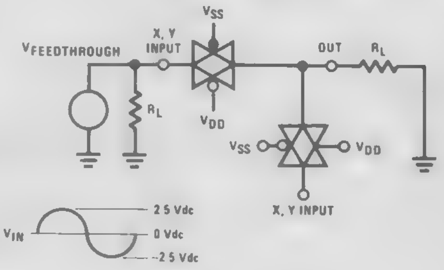
R_{ON} Characteristics



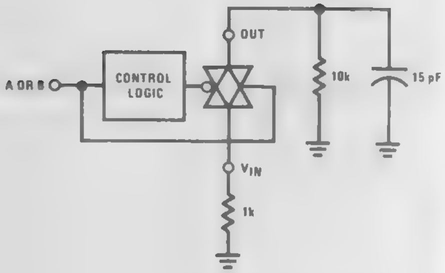
Noise Voltage



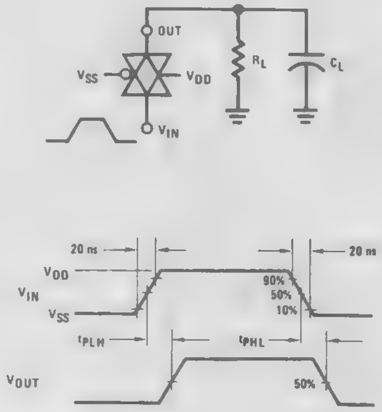
Frequency Response



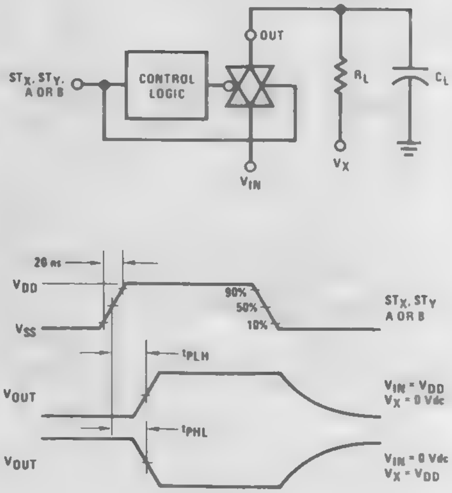
Crosstalk



Propagation Delay

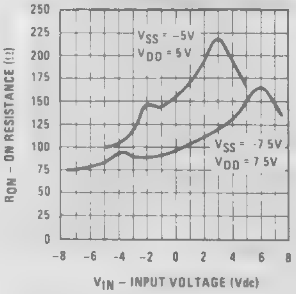


Turn-ON Delay Time

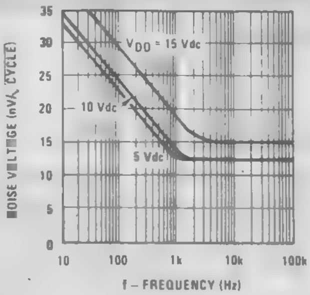


Typical Performance Characteristics

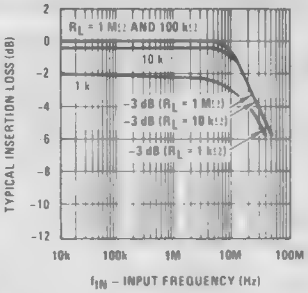
Typical R_{ON} vs V_{IN}



Typical Noise Characteristics



Typical Insertion Loss/ Bandwidth Characteristics



National Semiconductor

CD4538BM/CD4538BC Dual Precision Monostable Multivibrator

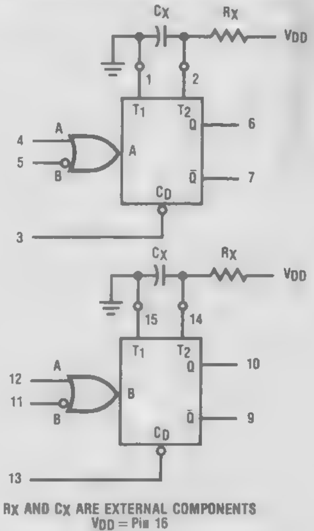
General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

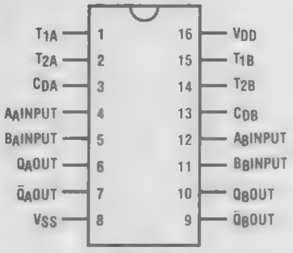
Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- New Formula: $PW_{OUT} = RC$ (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range 1 μs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current 5 nA (typ.) @ 5 V_{DC}
- Pin Compatible to CD4528B

Block & Connection Diagrams



R_X AND C_X ARE EXTERNAL COMPONENTS
V_{DD} = Pin 16
V_{SS} = Pin 8



CD4538BC

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⊓	⊔
H	↑	H	⊓	⊔

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⊓ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} DC Supply Voltage	$-0.5V$ to $+18V_{DC}$
V_{IN} Input Voltage	-0.5 to $V_{DD}+0.5V_{DC}$
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD} DC Supply Voltage	$+3$ to $+15V_{DC}$
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4538BM,	−55°C to +125°C
CD4538BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4538BM

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IH}=V_{DD}$		5		0.005	5		150	μA
		$V_{DD}=10V$, $V_{IL}=V_{SS}$		10		0.010	10		300	μA
		$V_{DD}=15V$, All outputs open		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$, $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$, $\|I_O\| < 1\mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$, $V_{IH}=V_{DD}$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_{IL}=V_{SS}$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$, $V_{IH}=V_{DD}$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_{IL}=V_{SS}$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current, pin 2 or 14	$V_{DD}=15V$, $V_{IN}=0V$ or $15V$		±0.02		$\pm10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current, other inputs	$V_{DD}=15V$, $V_{IN}=0V$ or $15V$		±0.1		$\pm10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics (Note 2) — CD4538BC

	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$; $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$, All outputs open		20		0.005	20		150	μA
		$V_{DD}=10V$		40		0.010	40		300	μA
		$V_{DD}=15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$; $\|I_O\| < 1\mu A$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$; $\|I_O\| < 1\mu A$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$; $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$; $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current, pin 2 or 14	$V_{DD}=15V$, $V_{IN}=0V$ or $15V$		±0.02		$\pm10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current, other inputs	$V_{DD}=15V$, $V_{IN}=0V$ or $15V$		±0.3		$\pm10^{-5}$	±0.3		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

		$V_{DD} = 15V$			40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation — A or B to Q or $\overline{Q}$					
		$V_{DD} = 5V$			300	600	ns
		$V_{DD} = 10V$			150	300	ns
		$V_{DD} = 15V$			100	220	ns
		Reset Operation — C_D to Q or $\overline{Q}$					
		$V_{DD} = 5V$			250	500	ns
		$V_{DD} = 10V$			125	250	ns
		$V_{DD} = 15V$			95	190	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width A, B, or C_D	$V_{DD} = 5V$			35	70	ns
		$V_{DD} = 10V$			30	60	ns
		$V_{DD} = 15V$			25	50	ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5V$				0	ns
		$V_{DD} = 10V$			0	0	ns
		$V_{DD} = 15V$				0	ns
C_{IN}	Input Capacitance	Pin 2 or 14			10		pF
		other inputs			5	7.5	pF
PW_{OUT}	Output Pulse Width (Q or $\overline{Q}$)	$R_X = 100\,k\Omega$	$V_{DD} = 5V$	208	226	244	μs
	(Note: For typical distribution, see Figure 9)	$C_X = 0.002\,\mu F$	$V_{DD} = 10V$	211	230	248	μs
			$V_{DD} = 15V$	216	235	254	μs
		$R_X = 100\,k\Omega$	$V_{DD} = 5V$	8.83	9.60	10.37	ms
		$C_X = 0.1\,\mu F$	$V_{DD} = 10V$	9.02	9.80	10.59	ms
			$V_{DD} = 15V$	9.20	10.00	10.80	ms
		$R_X = 100\,k\Omega$	$V_{DD} = 5V$	0.87	0.95	1.03	s
		$C_X = 10.0\,\mu F$	$V_{DD} = 10V$	0.89	0.97	1.05	s
			$V_{DD} = 15V$	0.91	0.99	1.07	s
Pulse Width Match between circuits in the same package $C_X = 0.1\,\mu F$, $R_X = 100\,k\Omega$		$R_X = 100\,k\Omega$	$V_{DD} = 5V$		±1		%
		$C_X = 0.1\,\mu F$	$V_{DD} = 10V$		±1		%
			$V_{DD} = 15V$		±1		%
Operating Conditions							
R_X	External Timing Resistance			5.0		*	kΩ
C_X	External Timing Capacitance			0		No Limit	pF

*The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X, leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.

Logic Diagram

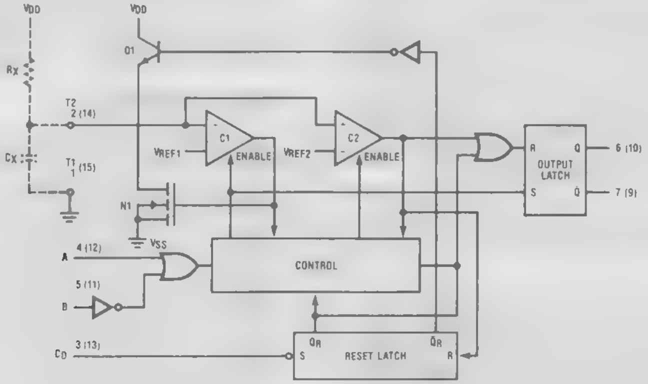
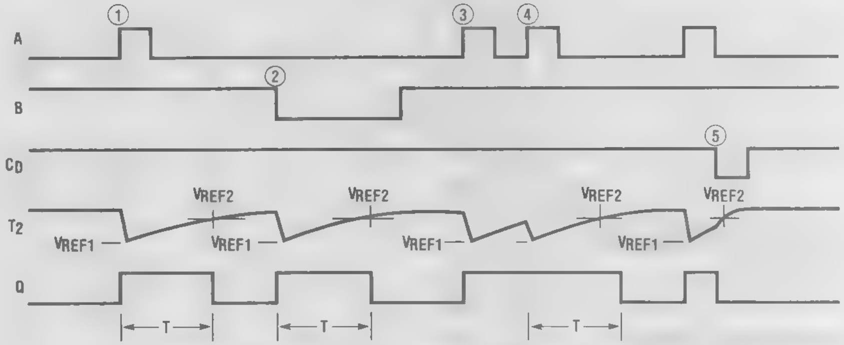


Figure 1.



① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET (PULSE SHORTENING)

Figure 2.

Trigger Operation

The block diagram of the CD4538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})②.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

Retrigger Operation

The CD4538B is retriggered if a valid trigger occurs③followed by another valid trigger④before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated④, the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Applications

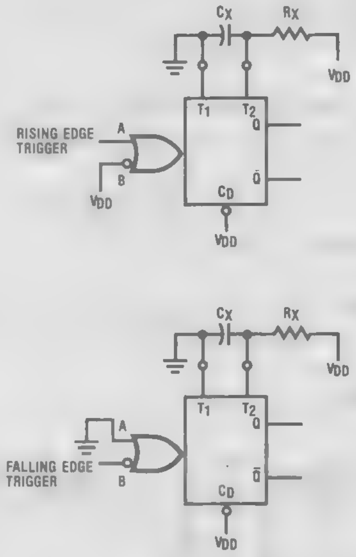


Figure 3. Retriggerable Monostables Circuitry

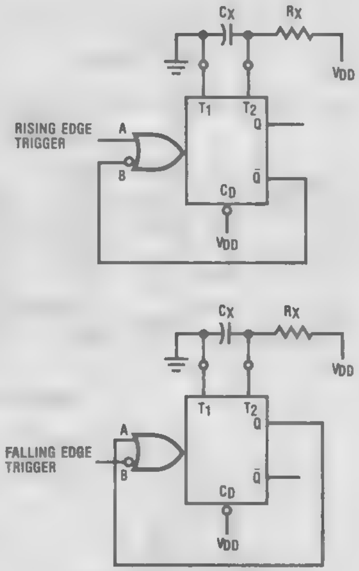


Figure 4. Non-retriggerable Monostables Circuitry

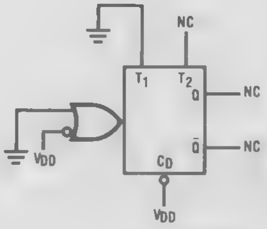


Figure 5. Connection of Unused Sections

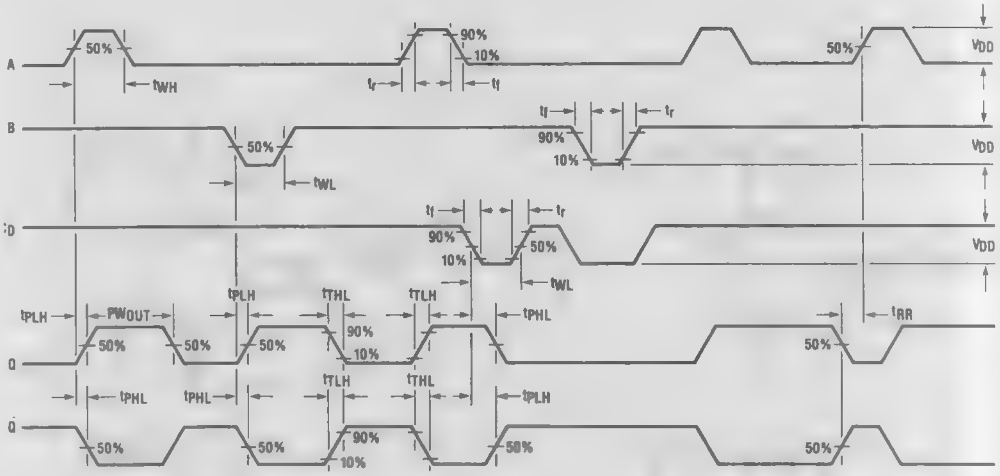
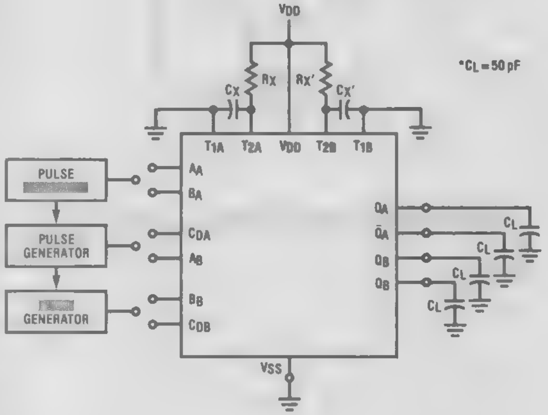


Figure 6. Switching Test Waveforms



INPUT CONNECTIONS

CHARACTERISTICS	CD	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*INCLUDES CAPACITANCE OF PROBES, WIRING, AND FIXTURE PARASITIC

NOTE: SWITCHING TEST WAVEFORMS FOR PG1, PG2, PG3 ARE SHOWN IN FIGURE 6.

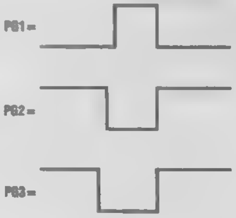
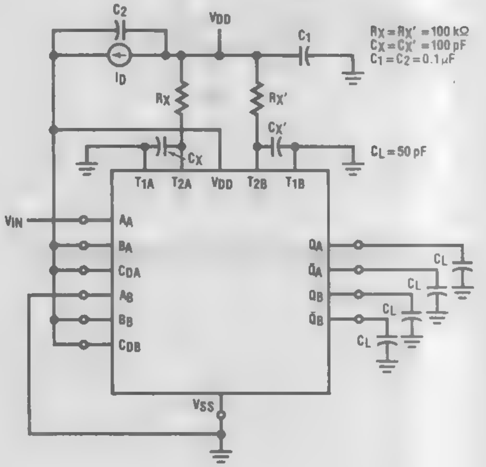


Figure 7. Switching Test Circuit



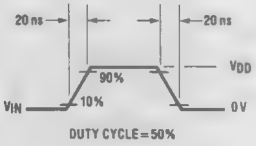


Figure 8. Power Dissipation Test Circuit and Waveforms

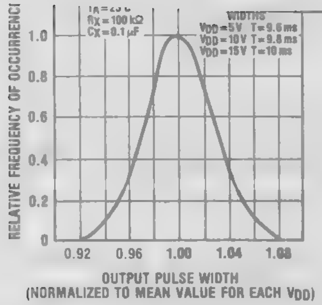


Figure 9. Typical Normalized Distribution of Units for Output Pulse Width

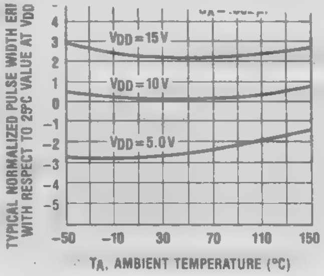


Figure 12. Typical Pulse Width Error Versus Temperature

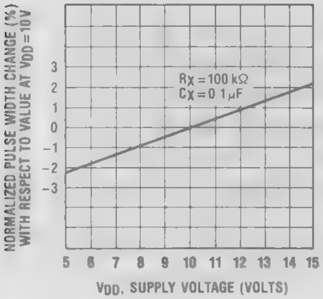


Figure 10. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

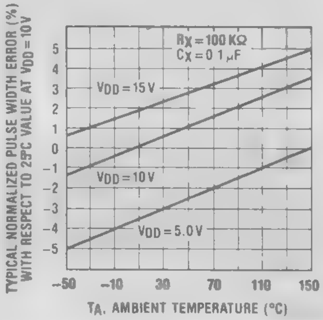


Figure 13. Typical Pulse Width Error Versus Temperature

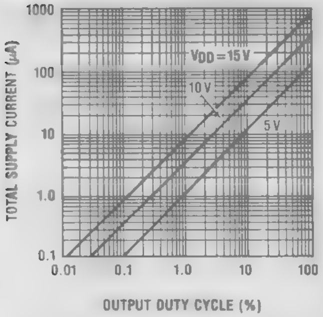


Figure 11. Typical Total Supply Current Versus Output Duty Cycle, $R_X = 100\,k\Omega$, $C_L = 50\,pF$, $C_X = 100\,pF$, One Monostable Switching Only

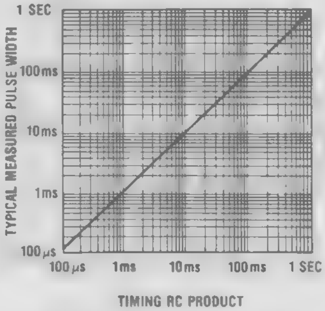


Figure 14. Typical Pulse Width Versus Timing RC Product

General Description

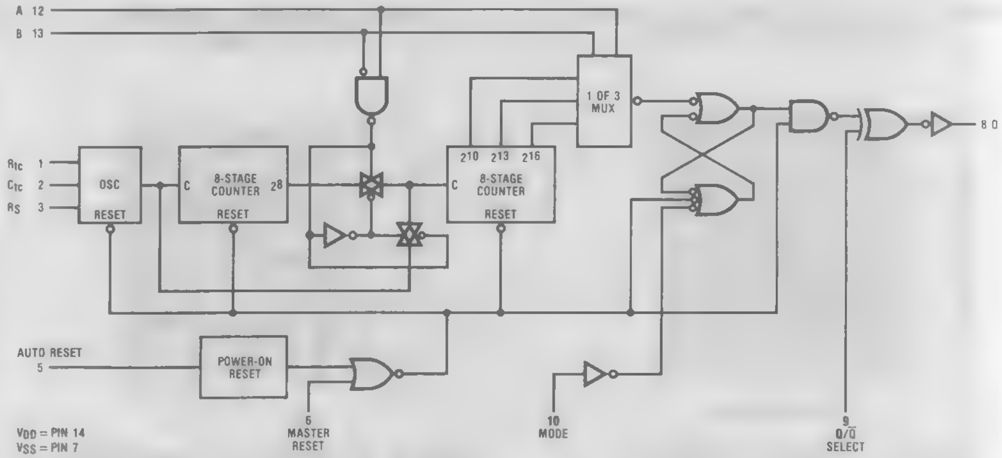
The CD4541B Programmable Timer is designed with a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The special features of the power-on reset circuit are first, no additional static power consumption and second, the part functions across the full voltage range (3-15V) whether power-on reset is enabled or disabled.

Timing and the counter are initialized by turning on power, if the power-on reset is enabled. When the power is already on, an external reset pulse will also initialize the timing and counter. After either reset is accomplished, the oscillator frequency is determined by the external RC network. The 16-stage counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

Features

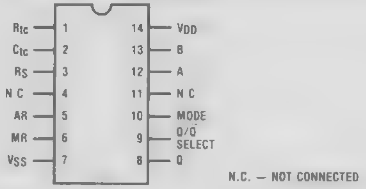
- Available division ratios 2^8, 2^{10}, 2^{13}, or 2^{16}
- Increments on positive edge clock transitions
- Built-in low power RC oscillator (±2% accuracy over temperature range and ±10% supply and ±3% over processing @ < 10kHz)
- Oscillator frequency range ≈ DC to 100kHz
- Oscillator may be bypassed if external clock is available (apply external clock to pin 3)
- Automatic reset initializes all counters when power turns on
- External master reset totally independent of automatic reset operation
- Operates as 2^n frequency divider or single transition timer
- Q/$\overline{Q}$ select provides output logic level flexibility
- Reset (auto or master) disables oscillator during resetting to provide no active power dissipation
- Clock conditioning circuit permits operation with very slow clock rise and fall times
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range
- High output drive (pin 8) min. one TTL load

Logic Diagram



Connection Diagram

Dual-In-Line Package



Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage, V_{DD}	−0.5 to +18V
Input Voltage, V_{IN}	−0.5 to V_{DD} + 0.5V
Storage Temperature Range, T_S	−65°C to +150°C
Package Dissipation, P_D	500 mW
Lead Temperature, T_L (soldering, 10 seconds)	300°C

Recommended Operating Conditions
(Note 2)

Supply Voltage, V_{DD}	3 to 15V
Input Voltage, V_{IN}	0 to V_{DD}
Operating Temperature Range	
CD4541BM	−55°C to +125°C
CD4541BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4541BM

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	μA
		$V_{DD} = 10V$		10		0.010	10		300	μA
		$V_{DD} = 15V$		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	2.85		2.27	3.6		1.6		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	4.96		4.0	9.0		2.8		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	19.3		15.6	34.0		10.9		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 2.5V$	7.96		6.42	13.0		4.49		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	4.19		3.38	8.0		2.37		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	16.3		13.2	30.0		9.24		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4541BC

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.005	20		150	μA
		$V_{DD} = 10V$		40		0.010	40		300	μA
		$V_{DD} = 15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	2.32		1.96	3.6		1.6		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	3.18		2.66	9.0		2.18		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	12.4		10.4	34.0		8.50		mA

DC Electrical Characteristics (Note 2) — CD4541BC (Cont'd)

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 2.5V$	5.1		4.27	13.0		3.5		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	2.69		2.25	8.0		1.85		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	10.5		8.8	30.0		7.22		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	µA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	µA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$ (refer to test circuits)

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{TLH}	Output Rise Time	$V_{DD} = 5V$		50	200	ns
		$V_{DD} = 10V$		30	100	ns
		$V_{DD} = 15V$		25	80	ns
t_{THL}	Output Fall Time	$V_{DD} = 5V$		50	200	ns
		$V_{DD} = 10V$		30	100	ns
		$V_{DD} = 15V$		25	80	ns
t_{PLH}, t_{PHL}	Turn-Off, Turn-On Propagation Delay, Clock to Q (2^8 Output)	$V_{DD} = 5V$		1.8	4.0	µs
		$V_{DD} = 10V$		0.6	1.5	µs
		$V_{DD} = 15V$		0.4	1.0	µs
t_{PHL}, t_{PLH}	Turn-On, Turn-Off Propagation Delay, Clock to Q (2^{16} Output)	$V_{DD} = 5V$		3.2	8.0	µs
		$V_{DD} = 10V$		1.5	3.0	µs
		$V_{DD} = 15V$		1.0	2.0	µs
$t_{WH(CL)}$	Clock Pulse Width	$V_{DD} = 5V$	400	200		ns
		$V_{DD} = 10V$	200	100		ns
		$V_{DD} = 15V$	150	70		ns
f_{CL}	Clock Pulse Frequency	$V_{DD} = 5V$		2.5	1.0	MHz
		$V_{DD} = 10V$		6.0	3.0	MHz
		$V_{DD} = 15V$		8.5	4.0	MHz
$t_{WH(R)}$	MR Pulse Width	$V_{DD} = 5V$	400	170		ns
		$V_{DD} = 10V$	200	75		ns
		$V_{DD} = 15V$	150	50		ns
C_I	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 3)			100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Truth Table

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

Division Ratio Table

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

Operating Characteristics

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3\,R_{tc}C_{tc}} \quad \text{if } (1\,\text{kHz} \leqslant f \leqslant 100\,\text{kHz})$$

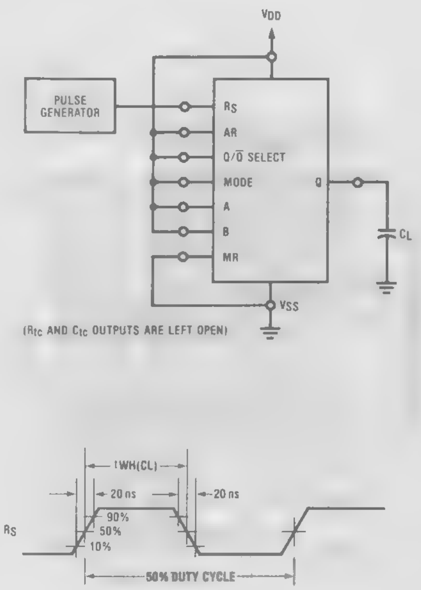
and $R_S \approx 2\,R_{tc}$ where $R_S \geqslant 10\,k\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13}, and 2^{16}). The 2^n counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

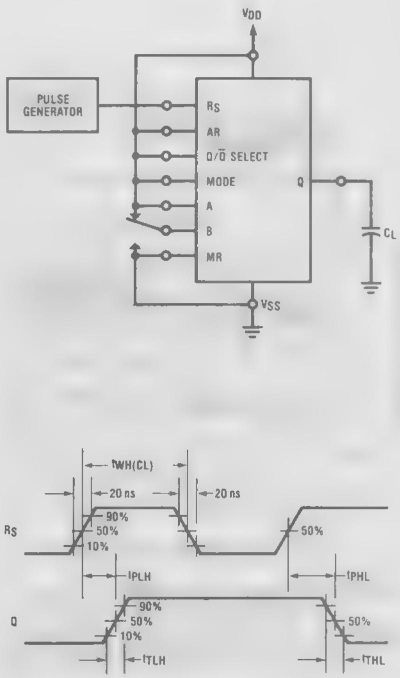
The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0". Correspondingly, when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

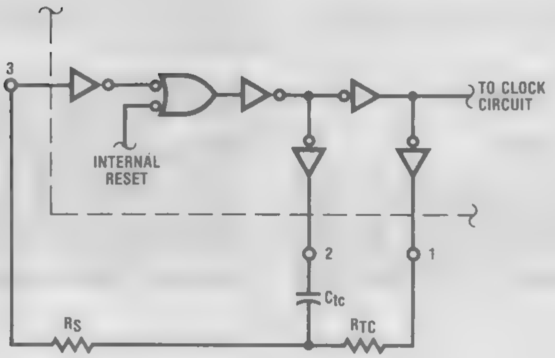
Power Dissipation Test Circuit and Waveform



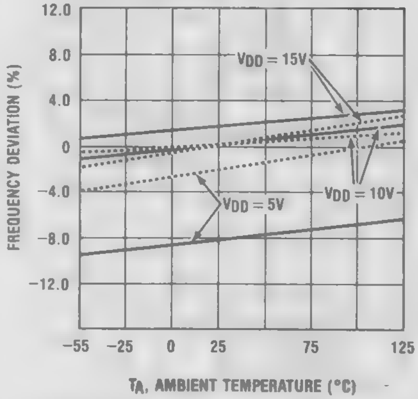
Switching Time Test Circuit and Waveforms



Oscillator Circuit Using RC Configuration



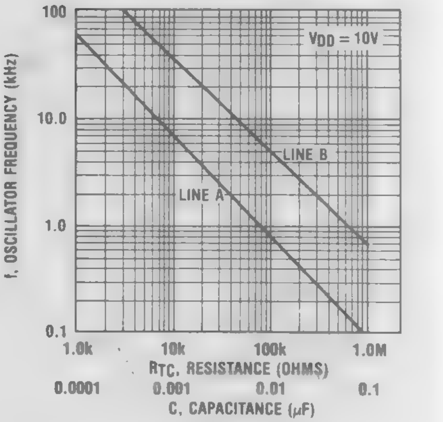
Typical RC Oscillator Characteristics



SOLID LINE = $R_{TC} = 56\ k\Omega$, $R_S = 1\ k\Omega$ AND $C = 1000\ pF$
$f = 10.2\ kHz$ @ $V_{DD} = 10V$ AND $T_A = 25°C$

DASHED LINE = $R_{TC} = 56\ k\Omega$, $R_S = 120\ k\Omega$ AND $C = 1000\ pF$
$f = 7.75\ kHz$ @ $V_{DD} = 10V$ AND $T_A = 25°C$

RC Oscillator Frequency as a Function of R_{TC} and C



LINE A: f AS A FUNCTION OF C AND ($R_{TC} = 56\ k\Omega$; $R_S = 120k$)
LINE B: f AS A FUNCTION OF R_{TC} AND ($C = 1000\ pF$; $R_S = 2\ R_{TC}$)

National Semiconductor

CD4543BM/CD4543BC BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals

General Description

The CD4543BM/CD4543BC is a monolithic CMOS BCD-to-7-segment latch/decoder/driver for use with liquid crystal and other types of displays. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-7-segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI) and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display, and the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

■ Wide supply voltage range	3.0 V to 18 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Low power dissipation	50 nA/package (typ.) at V_{DD} = 5.0 V

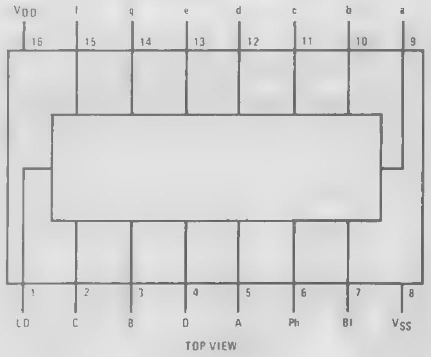
- Latch storage
- Blanking input
- Blank for all illegal inputs
- Direct-drive LCD, LED and VF displays
- Pin-for-pin replacement for CD4056B (with pin 7 tied to V_{SS})
- Pin-for-pin replacement for Motorola MC14543B

Applications

- Instrument (e.g., counter, DVM, etc.) display driver
- Computer/calculator display driver
- Cockput display driver
- Various clock, watch, and timer users

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

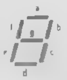
INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as Above

X = Don't care

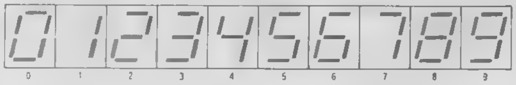
† = Above combinations

* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.

** = Depends upon the BCD code previously applied when LD = 1.



Display Format



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 V_{DC} to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD} V_{DC}$
T_A Operating Temperature Range	
CD4543BM	−55°C to +125°C
CD4543BC	−40°C to +85°C

DC Electrical Characteristics CD4543BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\,\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4543BC (Note 2)

PARAMETER		CONDITIONS	40°C		25 C			85 C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\,\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0			2.4		mA

DC Electrical Characteristics CD4543BC (Note 2) (Continued)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		1.1			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

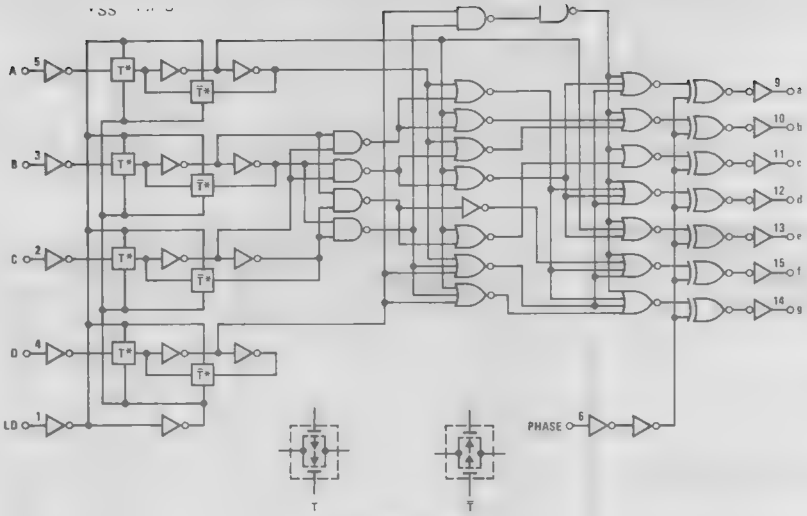
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50$ pF, $V_{SS} = 0$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Output Rise Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_f	Output Fall Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}	Turn-ON Propagation Delay Time	V_{DD} = 5V		450	1100	ns
		V_{DD} = 10V		170	440	ns
		V_{DD} = 15V		110	330	ns
t_{PHL}	Turn-OFF Propagation Delay Time	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		180	440	ns
		V_{DD} = 15V		120	330	ns
t_{SET-UP}	Set-Up Time	V_{DD} = 5V		−5	80	ns
		V_{DD} = 10V		2	30	ns
		V_{DD} = 15V		0	20	ns
t_{HOLD}	Hold Time	V_{DD} = 5V		30	120	ns
		V_{DD} = 10V		20	45	ns
		V_{DD} = 15V		15	30	ns
PW_{LD}	Latch Disable Pulse Width	V_{DD} = 5V		50	250	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		20	80	ns
C_{IN}	Input Capacitance	Per Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	See C_{PD} Measurement Waveforms, (Note 3)		300		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

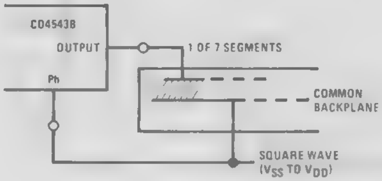
Note 3: C_{PD} determines the no load AC power consumption of a CMOS device. For a complete explanation, see "MM54C/74C Family Characteristics" application note AN-90.



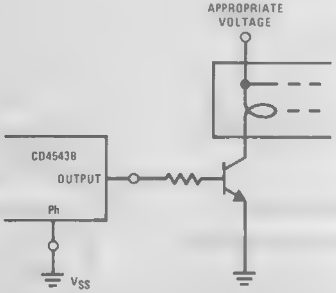
*Transmission gates

Typical Applications

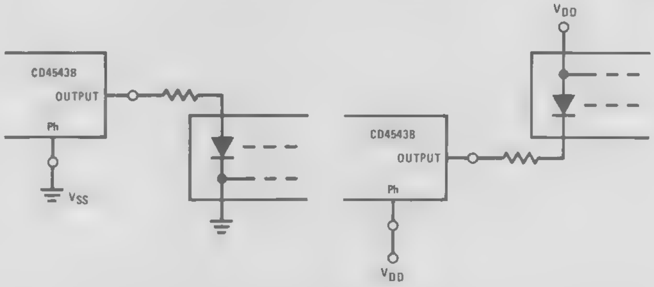
Liquid Crystal (LC) Readout



Incandescent Readout



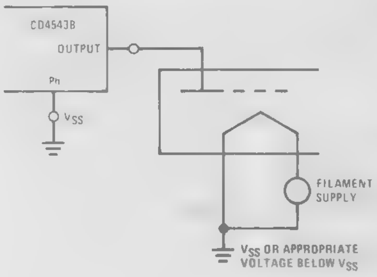
Light Emitting Diode (LED) Readout



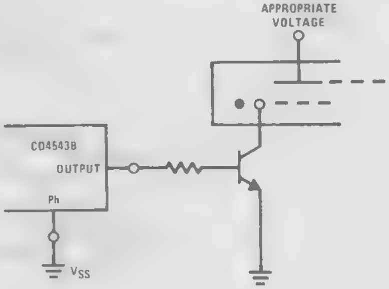
Note. Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{OUT} \geq 10$ mA)

Typical Applications (Continued)

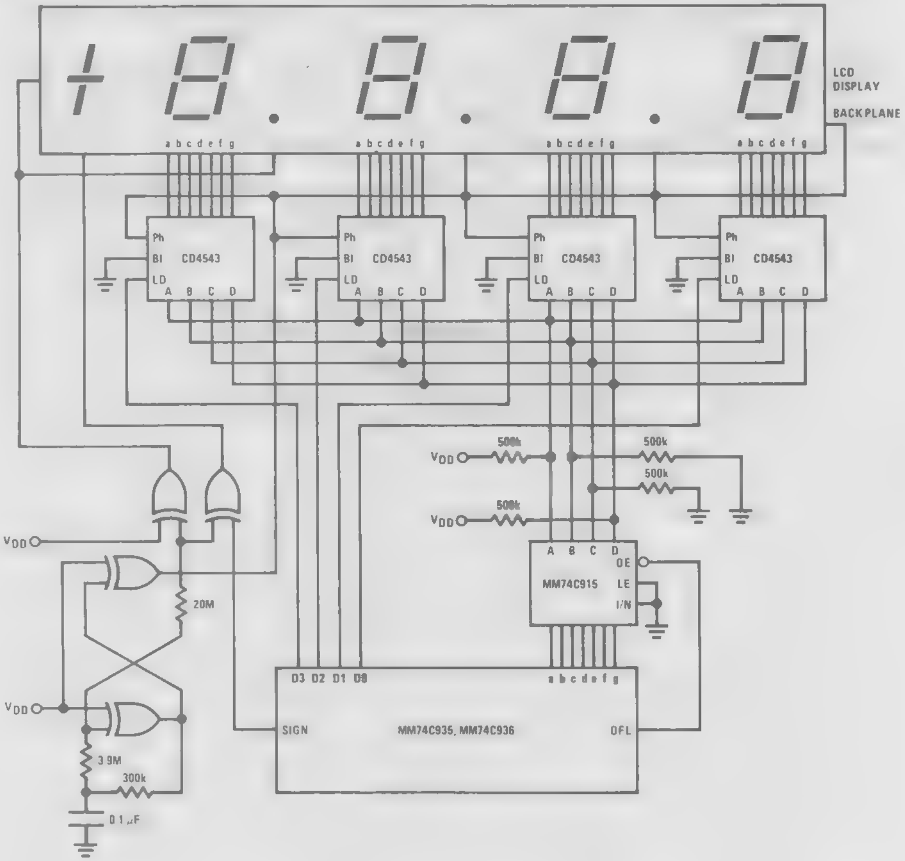
Fluorescent Readout



Gas Discharge Readout



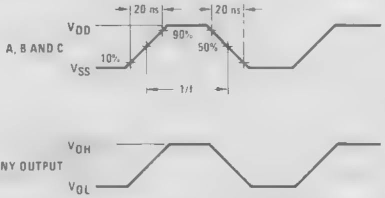
3 1/2-Digit DVM with LCD Display



Display 9.999 when overflowed. All digits can also be blanked at overflow by tying OFL to BI on the CD4543's

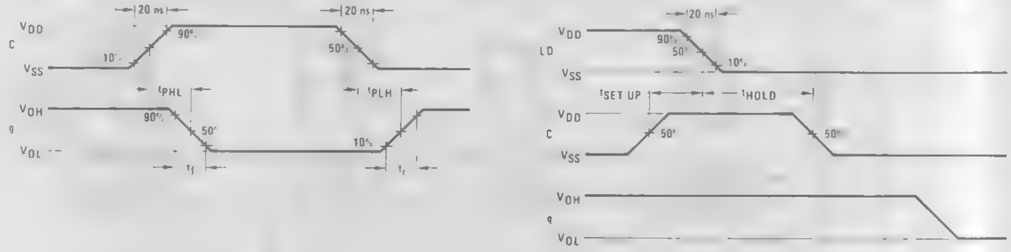
Switching Time Waveforms

C_{PD} Measurement Waveforms



Inputs BI and Ph low, and inputs D and LD high. f in respect to a system clock.
All outputs connected to respective C_L loads.

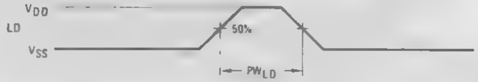
Dynamic Signal Waveforms



(a) Inputs D, Ph and BI low, and inputs A, B and LD high

(b) Inputs D, Ph and BI low, and inputs A and B high

(c) Data DCBA strobe into latches



National Semiconductor

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch
CD4724BM/CD7424BC 8-Bit Addressable Latch

General Description

The CD4723B is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0, A1), an active low enable input ($\overline{E}$), and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0-Q3). The CD4724B is an 8-bit addressable latch with three address inputs (A0-A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0-Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

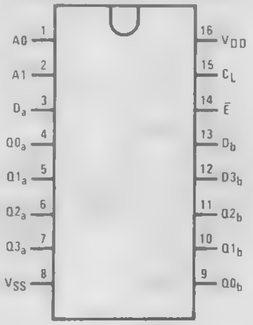
Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

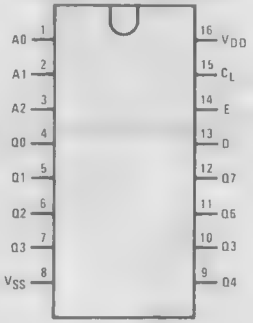
Connection Diagrams

CD4723B
Dual-In-Line and Flat Package



TOP VIEW

CD4724B
Dual-In-Line and Flat Package



TOP VIEW

Truth Table

MODE SELECTION				
$\overline{E}$	CL	ADDRESSED LATCH	UNADDRESSED LATCH	MODE
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4723BM/CD4724BM	−55°C to +125°C
CD4723BC/CD4724BC	−40°C to +85°C

DC Electrical Characteristics CD4723BM/CD4724BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0		0.02	5.0		150	μA
	V_{DD} = 10 V		10		0.02	10		300	μA
	V_{DD} = 15 V		20		0.02	20		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert \leq 1\mu A$								
	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert \leq 1\mu A$								
	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10		9.95		V
	V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4723BC/CD4724BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20		0.02	20		150	μA
	V_{DD} = 10 V		40		0.02	40		300	μA
	V_{DD} = 15 V		80		0.02	80		600	μA
V_{OL} Low Level Output Voltage	$\lvert I_O \rvert \leq 1\mu A$								
	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
	V_{DD} = 10 V		0.05		0	0.05		0.05	V
	V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\lvert I_O \rvert \leq 1\mu A$								
	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V	9.95		9.95	10		9.95		V
	V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 or 4.5 V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

I_{OL}	Low Level Output Current	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$	0.52		0.44	0.88		0.36		
		$V_{DD} = 10\,V$, $V_O = 0.5\,V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15\,V$, $V_O = 1.5\,V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5.0\,V$, $V_O = 4.6\,V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10\,V$, $V_O = 9.5\,V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15\,V$, $V_O = 13.5\,V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD} = 15\,V$, $V_{IN} = 15\,V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PHL}, t_{PLH}	Propagation Delay Date to Output	$V_{DD} = 5.0\,V$		200	400	ns
		$V_{DD} = 10\,V$		75	150	ns
		$V_{DD} = 15\,V$		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	$V_{DD} = 5.0\,V$		200	400	ns
		$V_{DD} = 10\,V$		80	160	ns
		$V_{DD} = 15\,V$		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	$V_{DD} = 5.0\,V$		175	350	ns
		$V_{DD} = 10\,V$		80	160	ns
		$V_{DD} = 15\,V$		65	130	ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	$V_{DD} = 5.0\,V$		225	450	ns
		$V_{DD} = 10\,V$		100	200	ns
		$V_{DD} = 15\,V$		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	$V_{DD} = 5.0\,V$		100	200	ns
		$V_{DD} = 10\,V$		50	100	ns
		$V_{DD} = 15\,V$		40	80	ns
t_{WH}, T_{WL}	Minimum Data Pulse Width	$V_{DD} = 5.0\,V$		100	200	ns
		$V_{DD} = 10\,V$		50	100	ns
		$V_{DD} = 15\,V$		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	$V_{DD} = 5.0\,V$		200	400	ns
		$V_{DD} = 10\,V$		100	200	ns
		$V_{DD} = 15\,V$		65	125	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5.0\,V$		75	150	ns
		$V_{DD} = 10\,V$		40	75	ns
		$V_{DD} = 15\,V$		25	50	ns
t_{SU}	Minimum Set-Up Time Data to E	$V_{DD} = 5.0\,V$		40	80	ns
		$V_{DD} = 10\,V$		20	40	ns
		$V_{DD} = 15\,V$		15	30	ns
t_H	Minimum Hold Time Data to E	$V_{DD} = 5.0\,V$		60	120	ns
		$V_{DD} = 10\,V$		30	60	ns
		$V_{DD} = 15\,V$		25	50	ns
t_{SU}	Minimum Set-Up Time Address to E	$V_{DD} = 5.0\,V$		−15	50	ns
		$V_{DD} = 10\,V$		0	30	ns
		$V_{DD} = 15\,V$		0	20	ns
t_H	Minimum Hold Time Address to E	$V_{DD} = 5.0\,V$		−50	15	ns
		$V_{DD} = 10\,V$		−20	10	ns
		$V_{DD} = 15\,V$		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

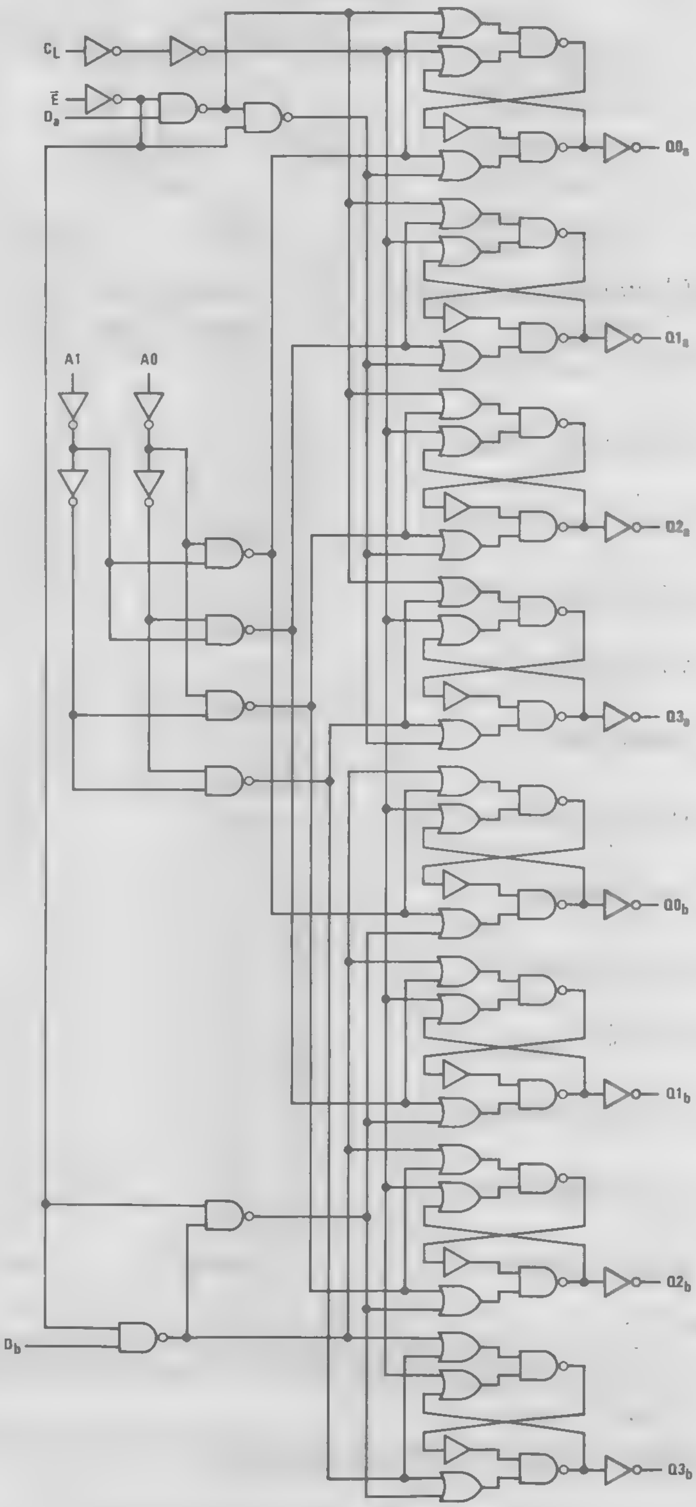
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\,V$ unless otherwise specified.

Note 3: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L)\,V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

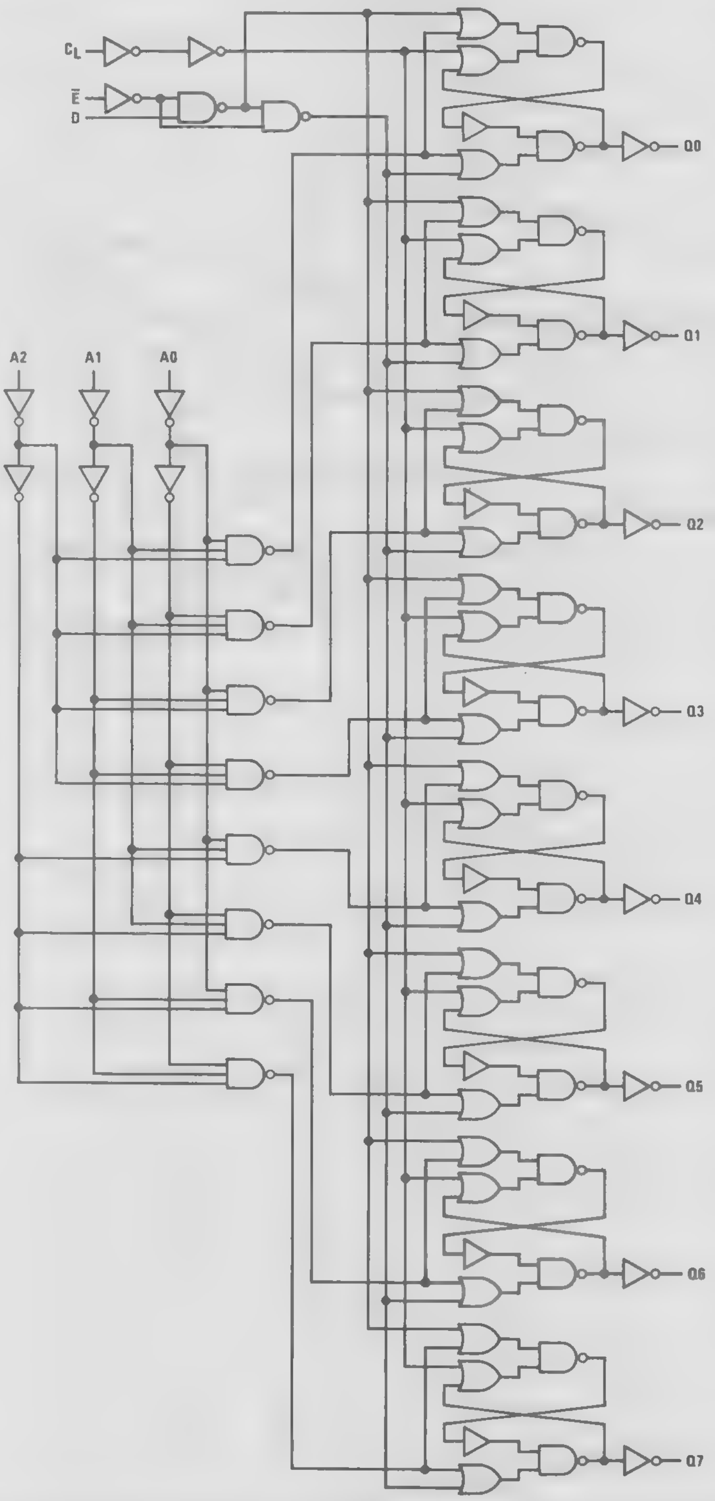
Logic Diagrams

CD4723B

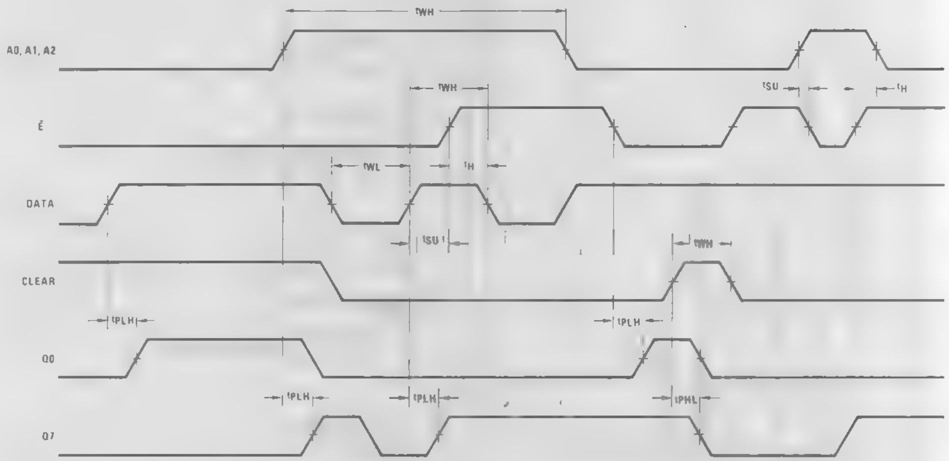


Logic Diagrams (Cont'd.)

CD4724B



Switching Time Waveforms



Section 6

CMOS Compatible Bipolar Interface Circuits

MM54C909/MM74C909 Quad Comparator

General Description

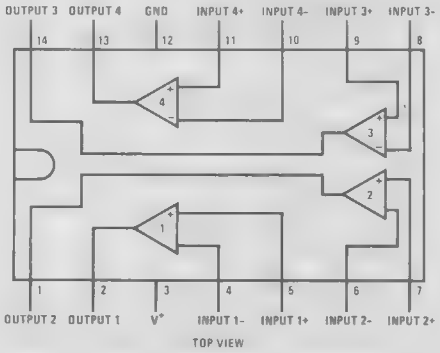
The MM54C909/MM74C909 contains four independent bipolar voltage comparators designed to operate from standard 54C/74C power supplies. The output allows current sinking only, thus the wire OR function is possible using a common resistor pull-up.

Not only does the MM54C909/MM74C909 function as a comparator for analog inputs, but also has many applications as a voltage translator and buffer when interfacing the 54C/74C family to other logic systems.

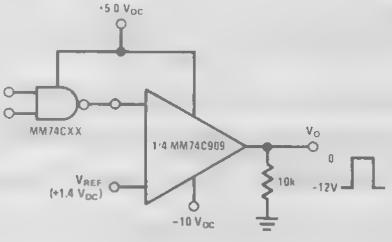
Features

■ Wide supply voltage range	3.0 V to 15 V
■ TTL compatibility	fan out of 1 driving 74
■ Low power consumption	$I_{CC} = 800\,\mu A$ (typ.) at $V_{CC} = 5.0\,V_{DC}$
■ Low input bias current	250 nA max.
■ Low input offset current	±50 nA max.
■ Low input offset voltage	±5.0 mV max.
■ Large common mode input voltage range	0 V to $V_{CC} - 1.5$ V
■ Large differential input voltage range	V_{CC}

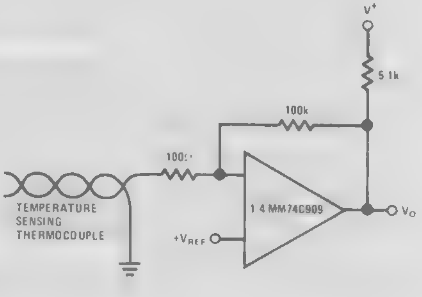
Connection Diagram



Typical Applications $(V^+ = 5.0\ V_{DC})$



CMOS/TTL to MOS Logic Converter



Ground Referenced Thermocouple in Single Supply System

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C909	$-55°C$ to $+125°C$
MM74C909	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation (Notes 2 and 3)	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Input Current ($V_{IN} < -0.3V$) (Note 4)	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted. ($V_{CC} = +5.0\ V_{DC}$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 9)				±9	mV
	$T_A = 25°C$		±2	±5	mV
Input Bias Current ($I_{IN(+)}$ or $I_{IN(-)}$) (Note 5)	$T_A = 25°C$, With Output in Linear Range		25	250 400	nA nA
Input Offset Current ($I_{IN(+)} - I_{IN(-)}$)				±150	nA
	$T_A = 25°C$		±5	±50	nA
Input Common Mode Voltage (Note 6)		0		$V_{CC}-2$	V
	$T_A = 25°C$	0		$V_{CC}-1.5$	V
Supply Current (I_{CC})	$T_A = 25°C$, $R_L = \infty$ On All Outputs		800	2000	µA
Voltage Gain	$T_A = 25°C$, $R_L \geq 15\ k\Omega$		200		V/mV
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Sink Current (I_{SINK}) MM54C909 MM74C909	$V_{CC} = 4.50V$ $V_{CC} = 4.75V$, $V_{OUT} = 0.4V$ $V_{IN(-)} \geq 1.0\ V_{DC}$ $V_{IN(+)} = 0\ V_{DC}$	1.6	3.2		mA
Output Leakage Current	$V_{IN(+)} \geq 1.0\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V_{OUT} = 15\ V_{DC}$			1	µA
	$V_{IN(+)} \geq 1.0\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V_{OUT} = 5\ V_{DC}$, $T_A = 25°C$		0.1		nA
Differential Input Voltage (Note 8)	All V_{IN}'s $\geq 0\ V_{DC}$			15	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operating at high temperatures, the MM74C909 must be derated based on +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies to the device soldered in a printed circuit board, operating in a still air ambient. The MM54C909 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small ($P_d \leq 100$ mW), provided the output sink current is within specified limits.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. There is a lateral NPN parasitic transistor action on the IC chip. The transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than $-0.3V$.

Note 5: The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +15V without damage.

Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: The positive excursions of the input can equal V_{CC} supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$.

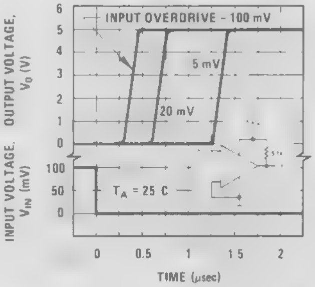
Note 9: At output switch point, $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC} and over the full input common mode range (0V_{DC}) to $V^+ \pm 1.5\ V_{DC}$).

AC Electrical Characteristics R_L = 5.1 kΩ, V_{RL} = 5.0 V_{DC}, unless otherwise specified.

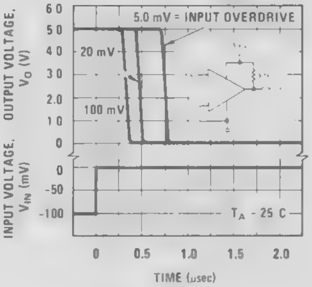
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Response Time	V_{IN} = TTL Swing V_{REF} = 1.4 V_{DC}		300		ns
Response Time	T_A = 25°C		1.3		μs

Typical Performance Characteristics

Response Time for Various Input Overdrives — Positive Transition



Response Time for Various Input Overdrives — Negative Transition



application hints

The MM54C909/MM74C909 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to <10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

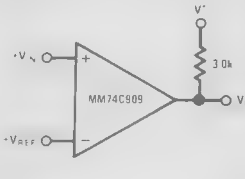
The bias network of the MM54C909/MM74C909 establishes an I_{CC} current which is independent of the magnitude of the power supply voltage over the range of from 3.0V to 15V.

It is usually unnecessary to use a bypass capacitor across the power supply line.

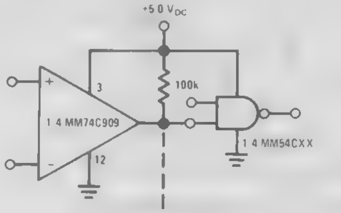
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

Many outputs can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the MM54C909/MM74C909 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the gain of the output device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly.

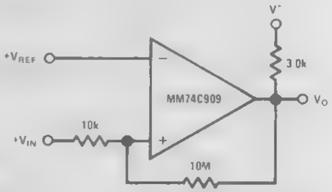
typical applications (con't) (V^+ = 5.0 V_{DC})



Basic Comparator

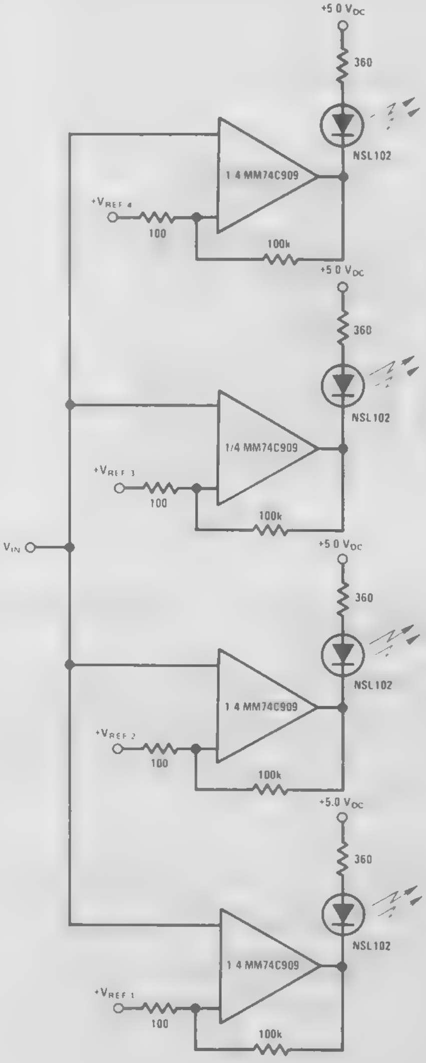


Driving CMOS

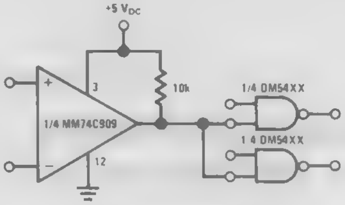


Non-Inverting Comparator with Hysteresis

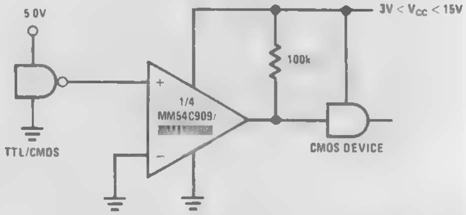
Typical Applications (Cont'd) ($V^+ = 5.0\ V_{DC}$)



Visible Voltage Indicator

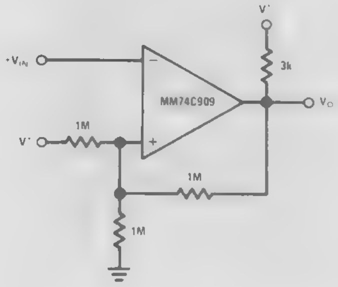


Driving TTL

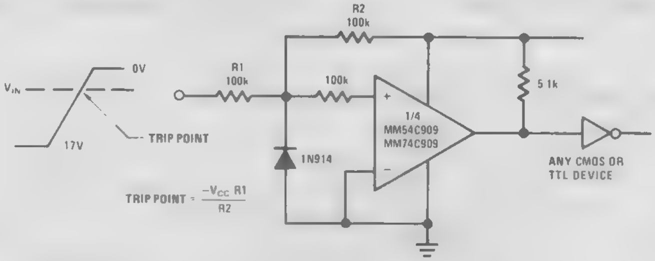


Note: For inverting buffer reverse input connection.

5V Logic to CMOS Operating at $V_{CC} \neq 5V$

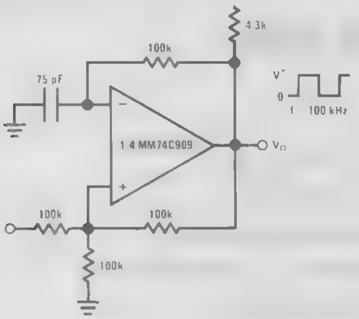


Inverting Comparator with Hysteresis

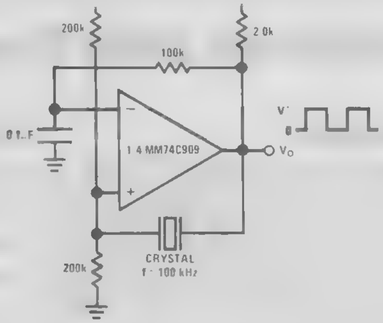


Note: For non inverting buffer reverse input connection.

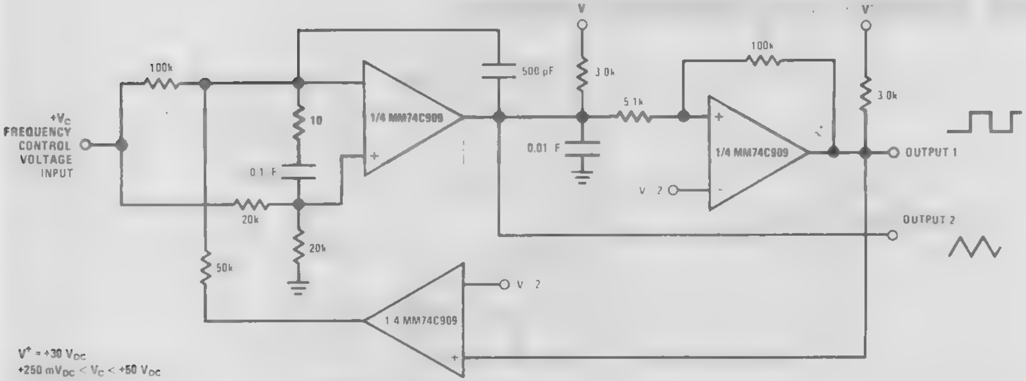
Hi Voltage Inverting PMOS to CMOS or TTL



Squarewave Oscillator

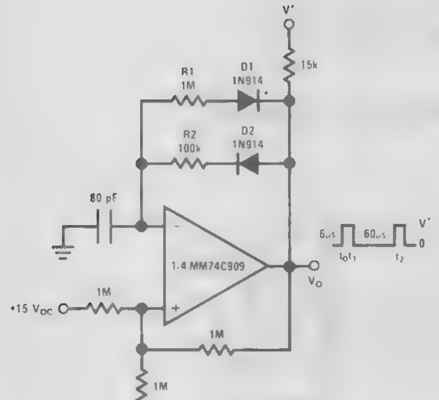


Crystal Controlled Oscillator



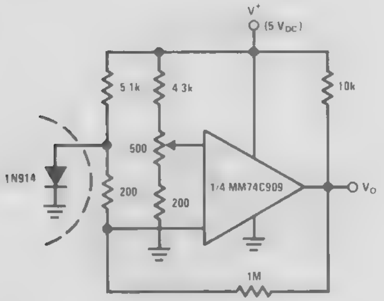
$V^+ = +30\ V_{DC}$
$+250\ mV_{DC} < V_C < +50\ V_{DC}$
$700\ Hz < f_O < 100\ kHz$

Two-Decade High-Frequency VCO



*For large ratios of R1/R2, D1 can be omitted

Pulse Generator



Remote Temperature Sensing

DS1630/DS3630

National Semiconductor

DS1630/DS3630 Hex CMOS Compatible Buffer

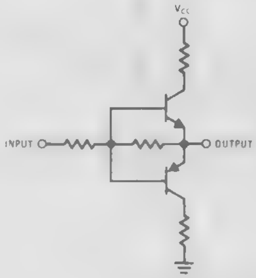
General Description

The DS1630/DS3630 is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630/DS3630 features low quiescent power consumption (typically 50μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630/DS3630 is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

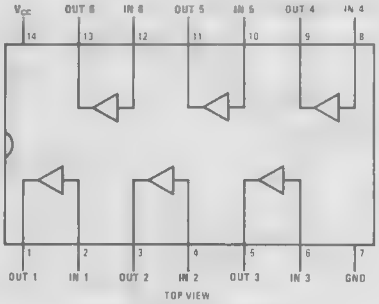
Features

- High-speed capacitive driver
- Wide supply voltage range
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50μW standby power (typ.)
- Fan out of 10 standard TTL loads

Equivalent Schematic and Connection Diagrams

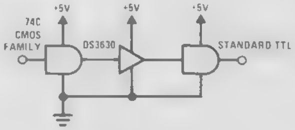


Dual-In-Line Package

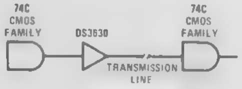


Order Number DS1630J, DS3630J or DS3630N

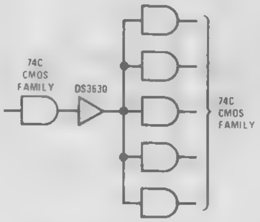
Typical Applications



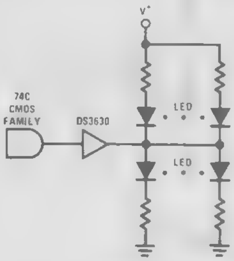
CMOS to TTL Interface



CMOS To Transmission Line Interface



CMOS To CMOS Interface



LED Driver

Absolute Maximum Ratings (Note 1)

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630	−55	+125	°C
DS3630	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{INH} Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630		90	200	μA
		DS3630		90	200	μA
	$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16$ mA	DS1630		0.5	3.2	mA
		DS3630		0.5	1.5	mA
I_{INL} Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		−0.15	−1	mA
		DS3630		V_{CC}−150	−800	μA
V_{OH} Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630	V_{CC}−1	V_{CC}−0.75		V
		DS3630	V_{CC}−0.9	V_{CC}−0.75		V
	$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = 16$ mA	DS1630	V_{CC}−2.5	V_{CC}−2.0		V
		DS3630	V_{CC}−2.5	V_{CC}−2.0		V
V_{OL} Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\mu A$	DS1630		0.75	1	V
		DS3630		0.75	0.9	V
	$V_{IN} = 0V$, $I_{OUT} = 16$ mA	DS1630		0.95	1.3	V
		DS3630		0.95	1.3	V
	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		1.2	1.6	V
		DS3630		1.2	1.5	V

AC Electrical Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} Propagation Delay to a Logical "0"	$C_L = 50$ pF		30	45	ns
	$C_L = 250$ pF		40	60	ns
	$C_L = 500$ pF		50	75	ns
t_{pd1} Propagation Delay to a Logical "1"	$C_L = 50$ pF		15	25	ns
	$C_L = 250$ pF		35	50	ns
	$C_L = 500$ pF		50	75	ns

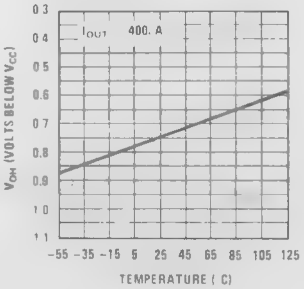
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630 and across the 0°C to +70°C range for the DS3630. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

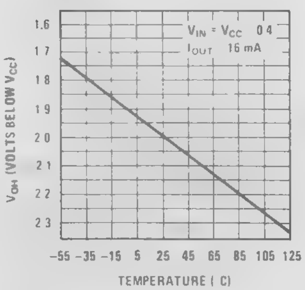
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Performance Characteristics

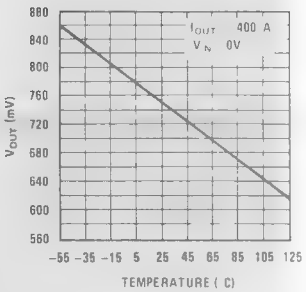
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



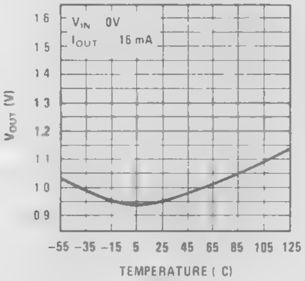
V_{OH} Active vs Temperature



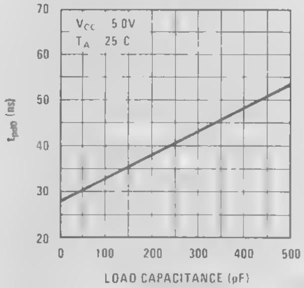
V_{OL} vs Temperature



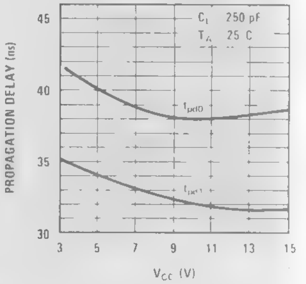
V_{OL} vs Temperature



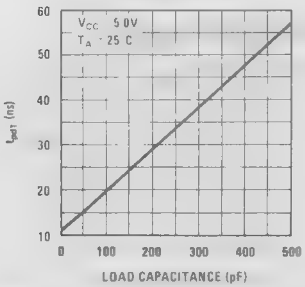
t_{pdo} vs Load Capacitance



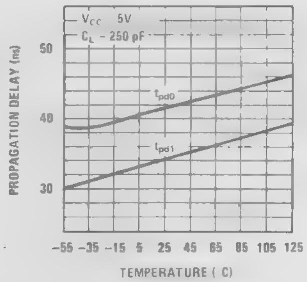
Propagation Delay vs V_{CC}



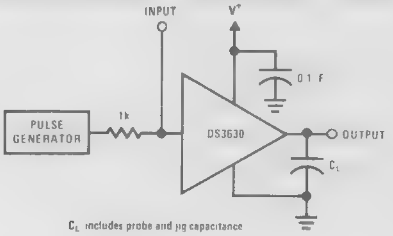
t_{pd1} vs Load Capacitance



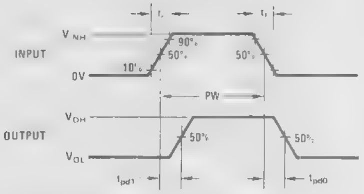
Propagation Delay vs Temperature



AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance



Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, $V_{IN} = 0$ to V_{CC}

DS1631/DS3631, DS1632/DS3632, DS1633/DS3633, DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS-compatible inputs with thresholds that track as a function of V_{CC} (approximately ½ V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56 V at 250 µA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max.) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical $V_{CC} = 5.0$ V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5 V to 15 V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was implied.

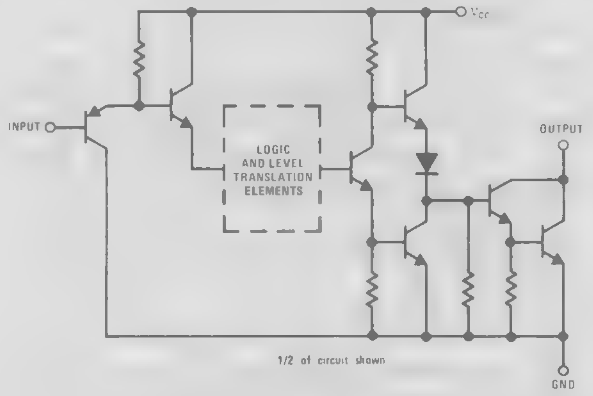
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the DM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL/DTL compatible at $V_{CC} = 5.0$ V.

Features

■ CMOS compatible inputs	
■ TTL/DTL compatible inputs	
■ High impedance inputs	PNP's
■ High output voltage breakdown	56 V min.
■ High output current capability	300 mA max.
■ Same pin-outs and logic functions as DS75451, DS75461, and DS3611 series circuits	
■ Low V_{CC} power dissipation (28 mW both outputs "ON" at 5.0 V)	

Schematic Diagram (Equivalent Circuit)



SEE CONNECTION DIAGRAMS FOR ORDERING INFORMATION

Absolute Maximum Ratings (Note 1)

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} +0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
All Circuits							
V_{IH} Logical "1" Input Voltage	*(Figure 1)*	V_{CC} = 5V		3.5	2.5		V
		V_{CC} = 10V		8.0	5		V
		V_{CC} = 15V		12.5	7.5		V
V_{IL} Logical "0" Input Voltage	*(Figure 1)*	V_{CC} = 5V			2.5	1.5	V
		V_{CC} = 10V			5.5	2.0	V
		V_{CC} = 15V			7.5	2.5	V
I_{IH} Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, *(Figure 2)*				0.1		µA
I_{IL} Logical "0" Input Current	V_{IN} = 0.4V, *(Figure 3)*	V_{CC} = 5V			50		µA
		V_{CC} = 15V			200		µA
V_{OH} Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250µA, *(Figure 1)*			56	65		V
V_{OL} Output Low Voltage	V_{CC} = Min, *(Figure 1)*	I_{OL} = 100 mA			0.9		V
		I_{OL} = 300 mA			1.1		V
DS1631/DS3631							
$I_{CC(0)}$ Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7		mA
		V_{CC} = 15V	Both Drivers		14		mA
$I_{CC(1)}$	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2		mA
		V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5		mA
t_{pd1} Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{pd0} Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1632/DS3632							
$I_{CC(0)}$ Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		8		mA
		V_{CC} = 15V, V_{IN} = 15V			18		mA
$I_{CC(1)}$	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		2.5		mA
		V_{CC} = 15V			9		mA
t_{pd1} Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{pd0} Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1633/DS3633							
$I_{CC(0)}$ Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7.5		mA
		V_{CC} = 15V			16		mA
$I_{CC(1)}$	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2		mA
		V_{CC} = 15V, V_{IN} = 15V			7.2		mA
t_{pd1} Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{pd0} Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Electrical Characteristics (Cont'd.)

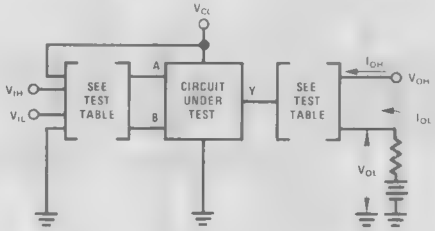
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5		mA
			V_{CC} = 15V, V_{IN} = 15V			18		mA
$I_{CC(1)}$		V_{IN} = 0V *(Figure 4)*	V_{CC} = 5V	Output High		3		mA
			V_{CC} = 15V			11		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the –55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

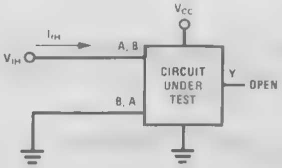
Test Circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
LM3611	V_{IH}	V_{IH}	I_{OH}	V_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
LM3612	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	I_{OH}	V_{OH}
LM3613	V_{IH}	GND	I_{OH}	V_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
LM3614	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	I_{OH}	V_{OH}

Note. Each input is tested separately

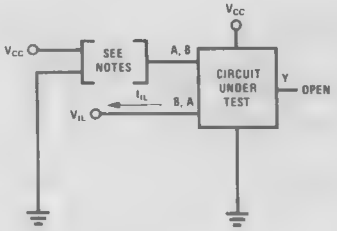
FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}



Each input is tested separately.

FIGURE 2. I_{IH}

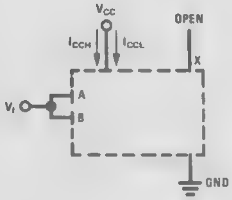
Test Circuits and Switching Time Waveforms



Note A: Each input is tested separately.

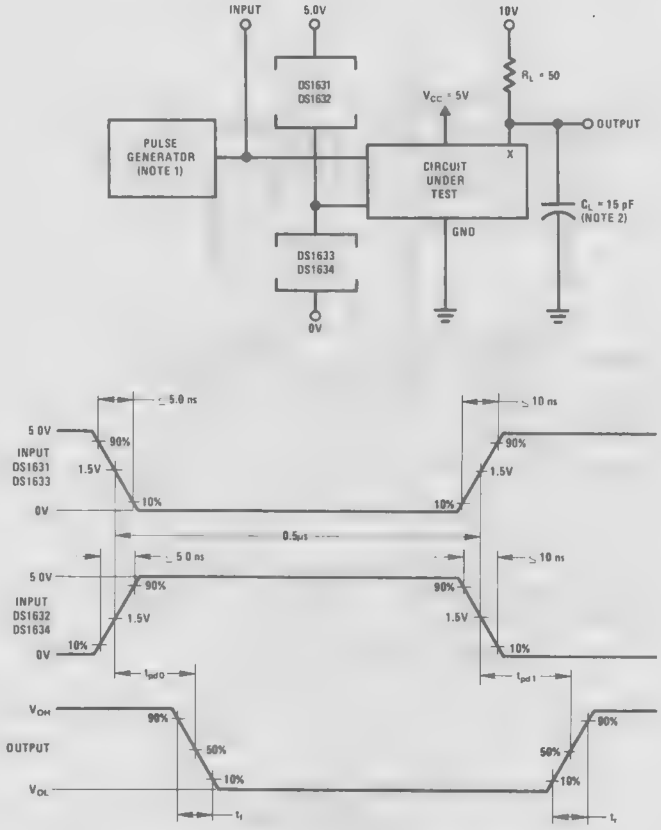
Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

FIGURE 3. I_{IL}



Both gates are tested simultaneously.

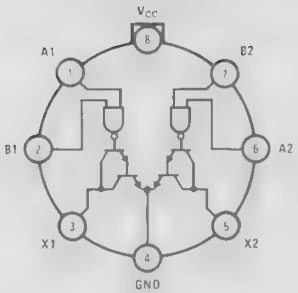
FIGURE 4. I_{CC}



Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 5. Switching Times.

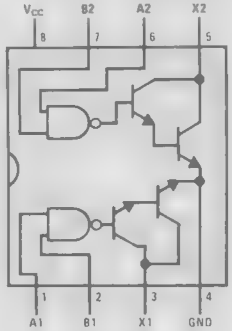


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1631H/DS3631H

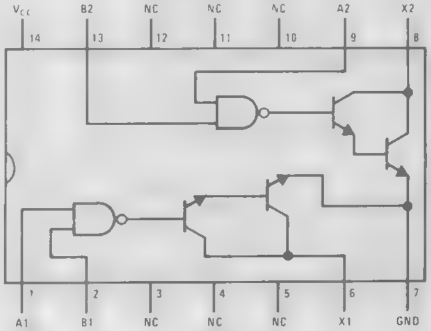
Dual-In-Line Package



TOP VIEW

Order Number 3631N

Dual-In-Line Package

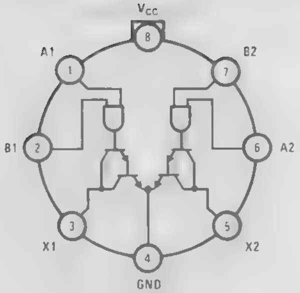


TOP VIEW

Order Number DS1631J/DS3631J

Positive logic: AB=X

A	B	OUTPUT X
0	0	0
1	0	0
0	1	0
1	1	1

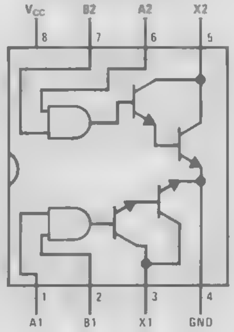


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1632H/DS3632H

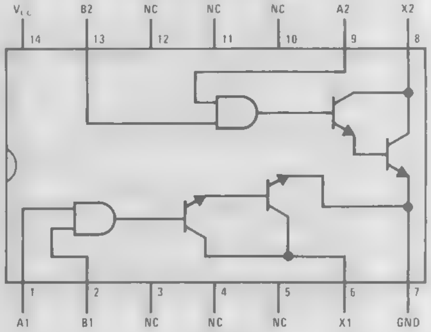
Dual-In-Line Package



TOP VIEW

Order Number DS3632N

Dual-In-Line Package



TOP VIEW

Order Number DS1632J/DS3632J

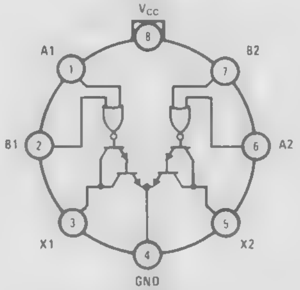
Positive logic: $\overline{AB}=X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Connection Diagrams, Truth Tables, and Ordering Information

DS1633

Metal Can Package

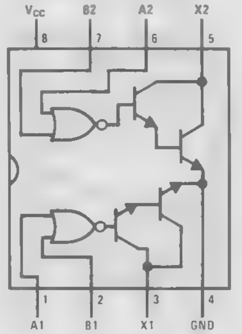


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1633H/DS3633H

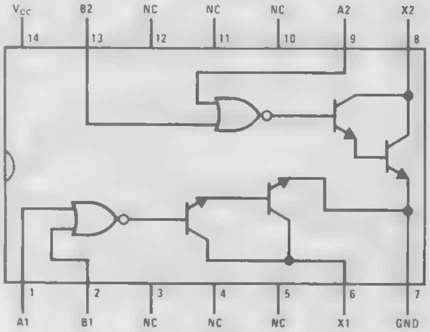
Dual-In-Line Package



TOP VIEW

Order Number DS3633N

Dual-In-Line Package



TOP VIEW

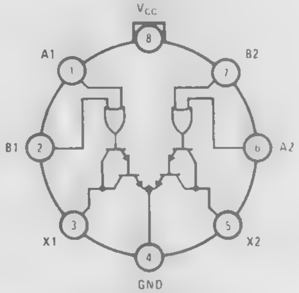
Order Number DS1633J/DS3633J

Positive logic: A + B = X

A	B	OUTPUT X
0	0	0
1	0	1
0	1	1
1	1	1

DS1634

Metal Can Package

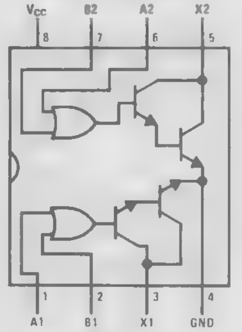


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1634H/DS3634H

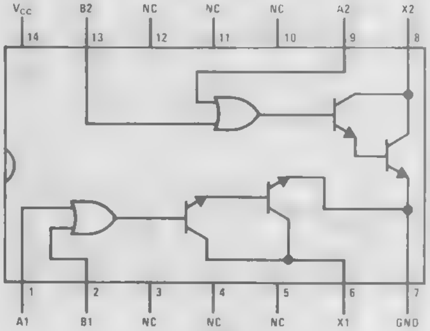
Dual-In-Line Package



TOP VIEW

Order Number DS3634N

Dual-In-Line Package



TOP VIEW

Order Number DS1634J/DS3634J

Positive logic: $\overline{A + B} = X$

A	B	OUTPUT X
0	0	1
1	0	0
0	1	0
1	1	0

National Semiconductor

DS1686/DS3686 Positive Voltage Relay Driver

General Description

The DS1686/DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54 V. Minimum output breakdown (AC/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

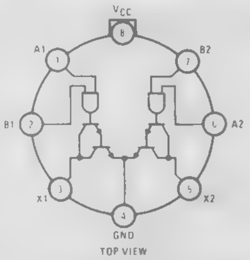
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65 V typ.)
- High output current capability (300 mA max.)
- Internal protection circuit eliminates need for output protection diode in most applications
- Output beakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation [90 mW (typ.) both outputs "ON"]
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

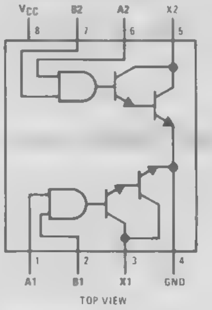
Metal Can Package



Pin 4 is in electrical contact with the case

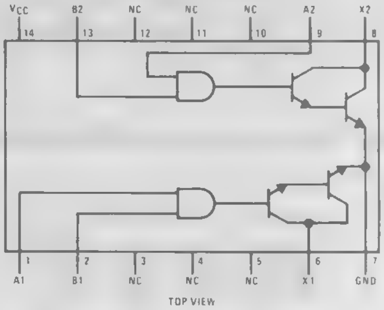
Order Number DS1686H or DS3686H

Dual-In-Line Package



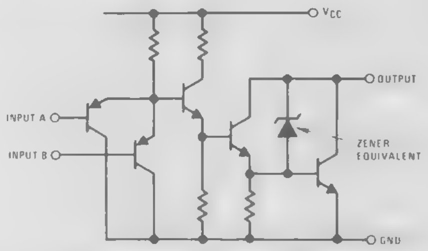
Order Number DS3686N

Dual-In-Line Package



Order Number DS1686J or DS3686J

Schematic Diagram



Truth Table

Positive logic. $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1686	4.5	5.5	V
DS3686	4.75	5.25	V
Temperature, T_A			
DS1686	−55	+125	°C
DS3686	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

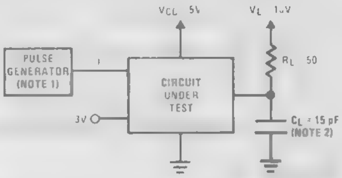
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				0.01	40	μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				60	250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = 5 mA			56	65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = 54V				0.5	250	μA
V_{OL}	Output "ON" Voltage	V_{CC} = Min, V_{IN} = 2V	I_{OUT} = 100μA	DS1686		0.85	1.1	V
				DS3686		0.85	1.0	V
			I_{OUT} = 300μA	DS1686		0.95	1.3	V
				DS3686		0.95	1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2.0	4.0	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18.0	28	mA
t_{pd0}	Propagation Delay to a Logical "0" (Output Turn "ON")	C_L = 15 pF, V_L = 10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				50		ns
t_{pd1}	Propagation Delay to a Logical "1" (Output Turn "OFF")	C_L = 15 pF, V_L = 10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				1.0		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1686 and across the 0°C to +70°C range for the DS3686. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

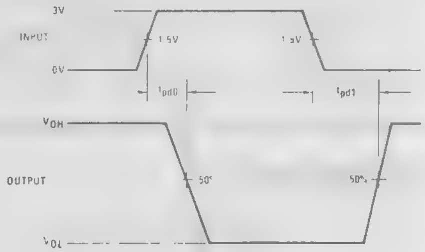
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \geq 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



DS1687/DS3687 Negative Voltage Relay Driver

General Description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (AC/latch breakdown) is specified over temperature at −5mA. This clearly defines the actual breakdown of the device, since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF", by input logic conditions, the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels — base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90mW.

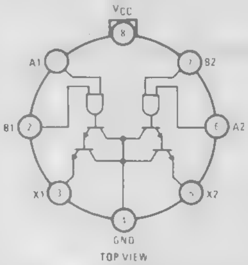
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ.)
- High output current capability (300mA max.)
- Internal protection circuit eliminates need for output protection diode in most applications
- Output breakdown protection if V_{CC} supply is lost
- Low power dissipation [90mW (typ.) both outputs "ON"]
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

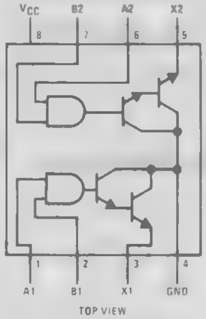
Metal Can Package



Pin 4 is in electrical contact with the case

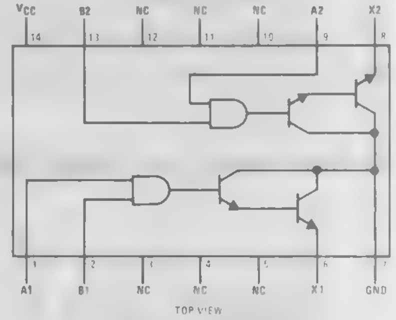
Order Number DS1687H
or DS3687H

Dual-In-Line Package



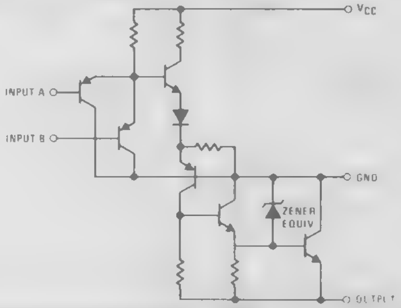
Order Number DS3687N

Dual-In-Line Package



Order Number DS1687J
or DS3687J

Schematic Diagram



Truth Table

Positive logic. $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	65 C to +150 C
Lead Temperature (Soldering, 10 seconds)	300 C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1687	4.5	5 5	V
DS3687	4 75	5 25	V
Temperature, T_A			
DS1687	55	+125	C
DS3687	0	+70	C

Electrical Characteristics (Notes 2 and 3)

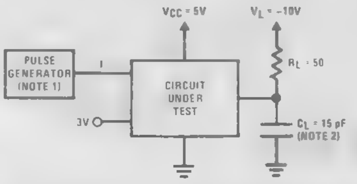
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage				2 0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				0 01	40	μA
V_{IL}	Logical "0" Input Voltage						0 8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				-60	250	μA
V_{CD}	Input Clamp Voltage	V_{CC} 5V, I_{CLAMP} -12 mA, T_A = 25 C				1 0	-1 5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			56	65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V				-0 5	−250	μA
V_{OL}	Output "ON" Voltage	V_{CC} Min, V_{IN} 2V	I_{OUT} 100 mA	DS1687		-0 85	-1 1	V
				DS3687		-0 85	1.0	V
			I_{OUT} 300 mA	DS1687		-0 95	-1 3	V
				DS3687		0 95	1 2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} - Max V_{IN} 0V Outputs Open				2 0	4 0	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max V_{IN} - 3V, Outputs Open				18.0	28	mA
$t_{pd(ON)}$	Propagation Delay to a Logical "0" (Output Turn "ON")	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				50		ns
$t_{pd(OFF)}$	Propagation Delay to a Logical "1" (Output Turn "OFF")	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				1 0		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

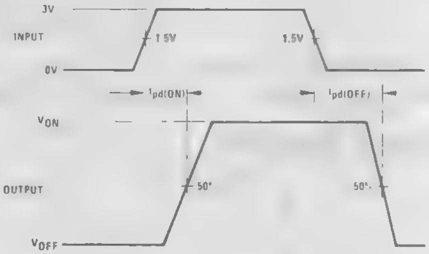
Note 3: All currents into device pins shown as positive, out of device pins as negative; all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \geq 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



National Semiconductor

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

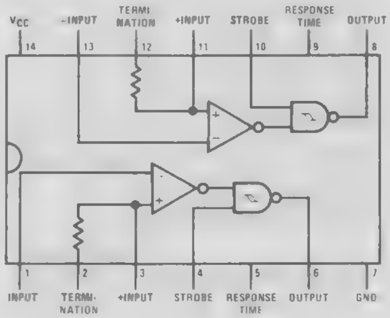
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Full compatibility with EIA Standards RS-232-C, RS-422, and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15 V (differential or common-mode)
- Separate strobe input for each receiver
- ½ V_{CC} strobe threshold for CMOS compatibility
- 5k input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5 V to 15 V

Connection Diagram

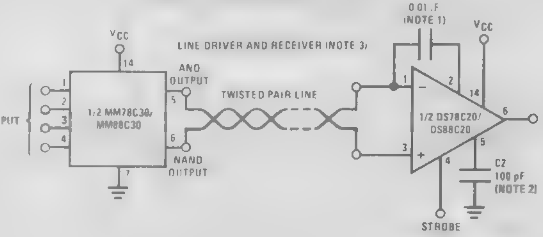
Dual-In-Line and Flat Package



TOP VIEW

Typical Application

RS-422/RS-423 Application



Note 1: (Optional internal termination resistor).

a) Capacitor in series with internal line termination resistor; terminates the line and saves termination power. Exact value depends on line length.

b) Pin 1 connected to pin 2; terminates the line.

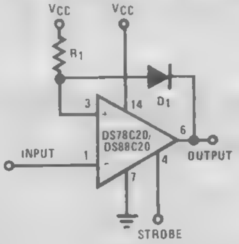
c) Pin 2 open; no internal line termination.

d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

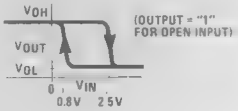
Note 3: V_{CC} = 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to application notes AN-22, AN-83 and AN-108.

RS-232-C Application with Hysteresis



For signals which require fail-safe or have slow rise and fall times, use R_1 and D_1 as shown above; otherwise the positive input (pin 3 or pin 11) may be connected to ground.

V_{CC}	$R_1 \pm 5\%$
5V	4.3kΩ
10V	15 kΩ
15V	24 kΩ



Absolute Maximum Ratings (Note 1)

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V
Differential Input Voltage (V_{DIFF})		≤6	V

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-10V \leq V_{CM} \leq 10V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$	$-10V \leq V_{CM} \leq 10V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$			5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$			2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = 200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A$, $V_{DIFF} = 1V$		$V_{CC} - 1.2$	$V_{CC} - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA$, $V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V$, $V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−0.5	100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$I_{OUT} = 1.6\ mA$, $V_{OL} \leq 0.5V$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5		V
			$V_{CC} = 15V$	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	$I_{OUT} = -200\ \mu A$, $V_{OH} = V_{CC} - 1.2V$	$V_{CC} = 5V$		2.5	1.5	V
			$V_{CC} = 10V$		5.0	2.0	V
			$V_{CC} = 15V$		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 15V$, $V_{STROBE} = 0V$, (Note 4)		−5	−20	−40	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	$C_L = 50\ pF$		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	$C_L = 50\ pF$		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	$C_L = 50\ pF$		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	$C_L = 50\ pF$		100	150	ns

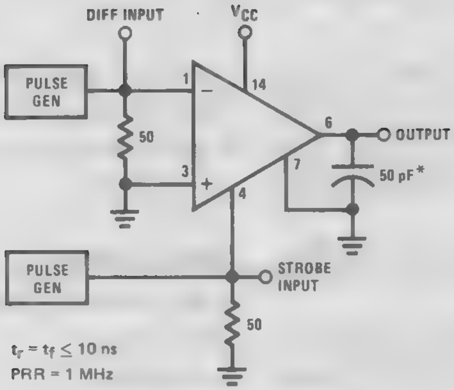
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

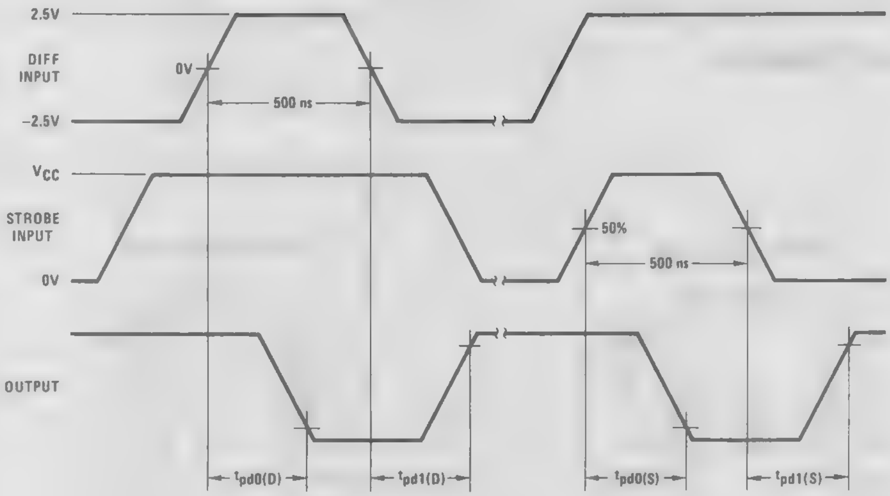
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.



*Includes probe and jig capacitance



National Semiconductor

PRELIMINARY INFORMATION

DP7310/DP8310/DP7311/DP8311 Octal Latched Peripheral Drivers

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30 volts. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are fall through latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

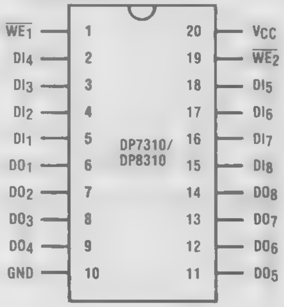
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature.
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber optic LED drivers

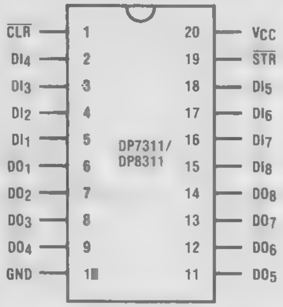
Connection Diagrams

Dual-In-Line Package



Order Number DP7310J, DP8310J DP8310N

Dual-In-Line Package



Order Number DP7311J, DP8311J DP8311N

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Storage Temperature Range	−65°C to +150°C
N Package Power Dissipation @ 70°C	1.3 watts
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature			
DP7310/DP7311	−55	+125	°C
DP8310/DP8311	0	+70	°C
Input Voltage		30	V
Output Voltage		30	V

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Parameter		Conditions	Min.	Typ.	Max.	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V_{CC} = min.				
	DP7310/DP7311	I_{OL} = 75 ma			0.4	V
	DP8310/DP8311	I_{OL} = 100 mA		0.35	0.5	V
I_{OH}	Logical "1" Output Current	Data outputs latched to logical "1", V_{CC} = min.				
	DP7310/DP7311	V_{OH} = 25V			500	μA
	DP8310/DP8311	V_{OH} = 30V		2.5	250	μA
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V, V_{CC} = max.		0.1	25	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 30V, V_{CC} = max.		1	250	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, V_{CC} = max.		−215	−300	μA
V_{clamp}	Input Clamp Voltage	I_{IN} = −12 mA		−0.8	−1.5	V
I_{CC0}	Supply Current, Outputs On	Data outputs latched to a logical "0". All inputs are at logical "1", V_{CC} = max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311			88	117	mA
	DP8311			88	125	mA
I_{CC1}	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I_{CC0}.				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

AC Electrical Characteristics DP7310/DP8310: $V_{CC} = 5V$, $T_A = 25°C$

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}	High to Low Propagation Delay Write Enable Input to Output	Figure 1		40		ns
t_{pd1}	Low to High Propagation Delay Write Enable Input to Output	Figure 1		70		ns
t_{SETUP}	Minimum Set-Up Time Data In to Write Enable Input	$t_{HOLD} = 0ns$ Figure 1		12		ns
t_{pWH}, t_{pWL}	Minimum Write Enable Pulse Width	Figure 1		20		ns
t_{THL}	High to Low Output Transition Time	Figure 1		16		ns
t_{TLH}	Low to High Output Transition Time	Figure 1		38		ns
C_{IN}	"N" Package Note 4			5	15	pF

AC Electrical Characteristics DP7311/DP8311: $V_{CC} = 5V$, $T_A = 25°C$

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}	High to Low Propagation Delay Data In to Output	Figure 2		30		ns
t_{pd1}	Low to High Propagation Delay Data In to Output	Figure 2		70		ns
t_{SETUP}	Minimum Set-Up Time Data In to Strobe Input	$t_{HOLD} = 0ns$ Figure 2		25		ns
t_{pWL}	Minimum Strobe Enable Pulse Width	Figure 2		45		ns
t_{pdC}	Propagation Delay Clear to Data Output	Figure 2		70		ns
t_{pWC}	Minimum Clear Input Pulse Width	Figure 2		10		ns
t_{THL}	High to Low Output Transition Time	Figure 2		16		ns
t_{TLH}	Low to High Output Transition Time	Figure 2		38		ns
C_{IN}	Input Capacitance — Any Input	Note 4		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min./max. limits apply across the −55°C to +125°C temperature range for the DP7310/DP7311 and across the 0°C to +70°C for the DP8310/DP8311. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

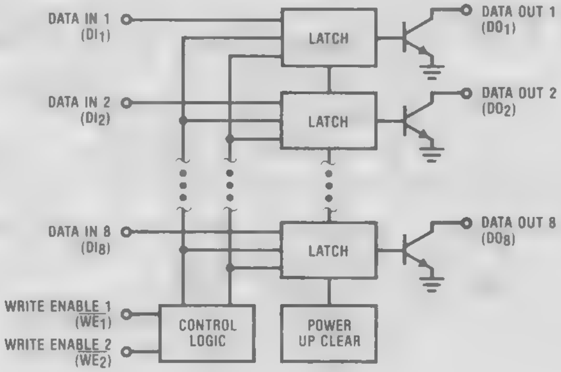
Note 4: Input capacitance is guaranteed by periodic testing. $f_{TEST} = 10\,KHz$ at 300 mV, $T_A = 25°C$

0	0	X	Q
0	↑	0	1
0	↑	1	0
↑	0	0	1
↑	0	1	0
0	1	X	Q
1	0	X	Q
1	1	X	Q

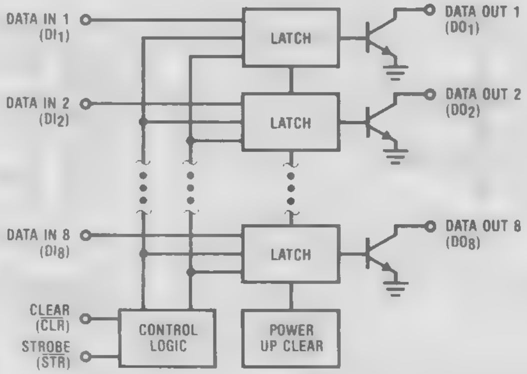
1	1	X	Q
1	0	0	1
1	0	1	0
0	X	X	1

X = Don't Care
1 = Outputs Off
0 = Outputs On
Q = Pre-existing Output
↑ = Positive Edge Transition

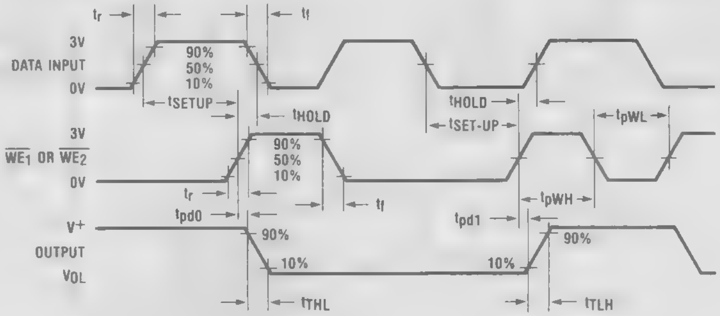
Block Diagram DP7310/DP8310



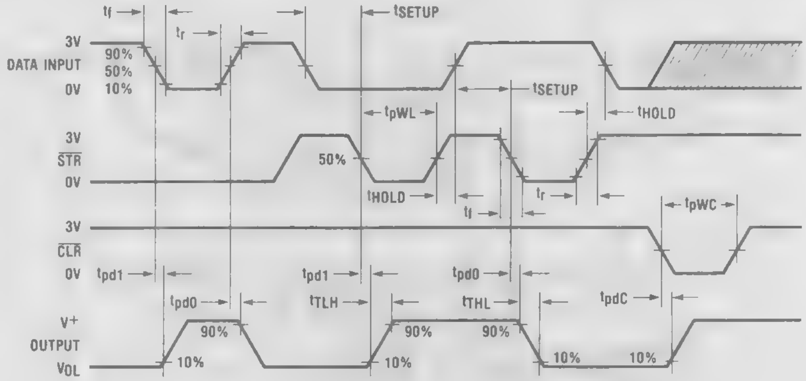
Block Diagram DP7311/DP8311



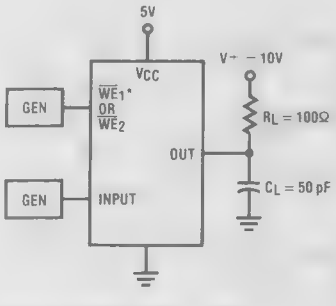
Switching Time Waveforms DP7310/DP8310



Switching Time Waveforms DP7311/DP8311

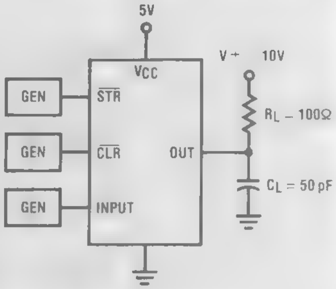


Switching Time Test Circuits DP7310/DP8310 DP7311/DP8311



*$\overline{WE_1}$ = 0V WHEN THE INPUT = $\overline{WE_2}$

Figure 1

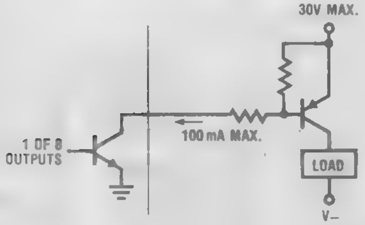


PULSE GENERATOR CHARACTERISTICS.
$Z_0 = 50\Omega$, $t_r = t_f = 5\,ns$

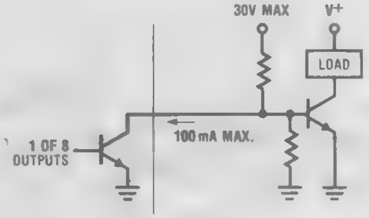
Figure 2

Typical Applications DP8310/11 Buffering High Current Device (Notes 5 and 6)

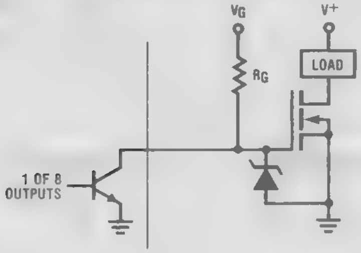
PNP High Current Driver



NPN High Current Driver

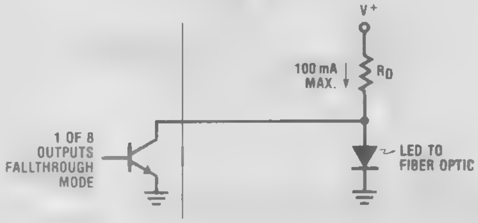


VMOS High Current Driver

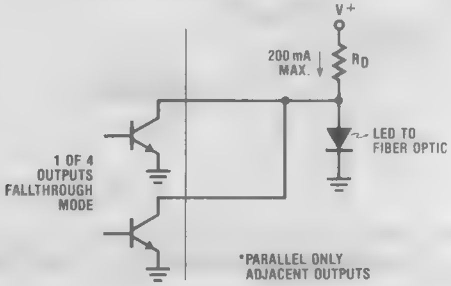


Eight Output/Four Output Fiber Optic LED Driver

DP8311 100 mA Drivers



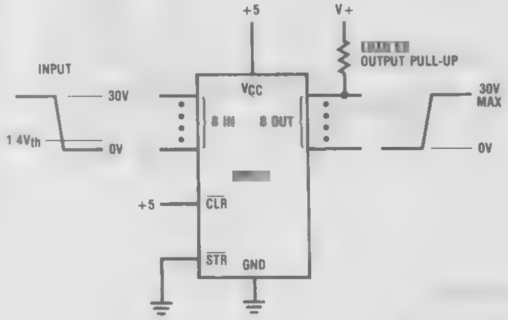
DP8311 Parallel Outputs (200 mA) Drivers*



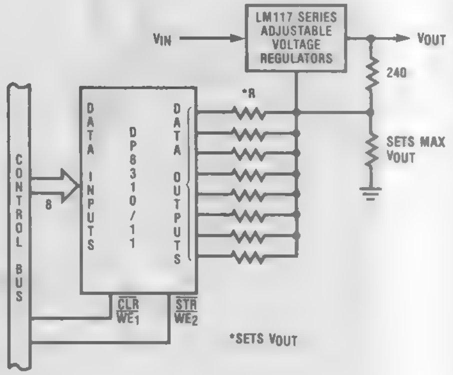
*PARALLEL ONLY ADJACENT OUTPUTS

Typical Applications (cont'd)

8-Bit Level Translator-Driver

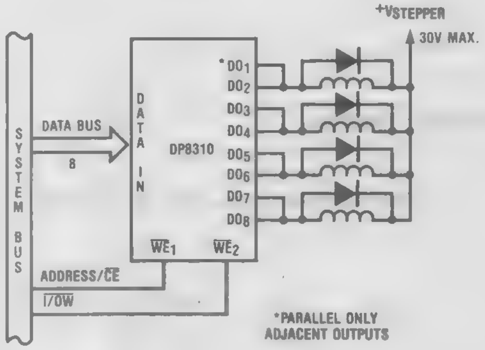


Digital Controlled 256 Level Power Supply from 1.2 Volts to 30 Volts



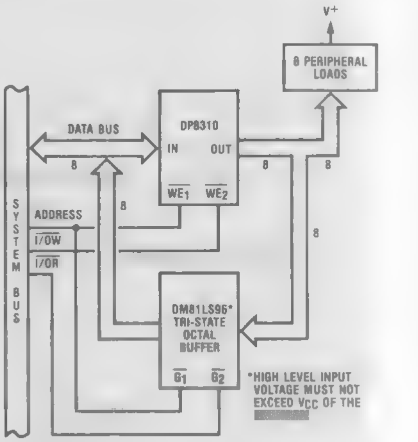
*SETS V$_{OUT}$

200 mA Drive for a 4 Phase Bifilar Stepper Motor



*PARALLEL ONLY ADJACENT OUTPUTS

Reading the State of the Latched Peripherals



*HIGH LEVEL INPUT VOLTAGE MUST NOT EXCEED V$_{CC}$ OF THE [redacted]

Note 5: Always use good V$_{CC}$ bypass and ground techniques to suppress transients caused by peripheral loads.

Note 6: Printed circuit board mounting is required if these devices are operated at maximum rated temperature and current (all outputs on DC).

LM195/LM295/LM395 Ultra Reliable Power Transistors

General Description

The LM195/LM295/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0 A and can switch 40 V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking cause the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

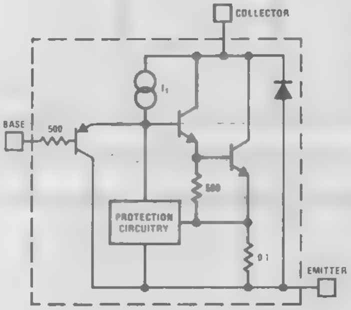
The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

The LM195/LM295/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from −55°C to +150°C, the LM295 from −25°C to +150°C, and the LM395 from 0°C to +125°C.

Features

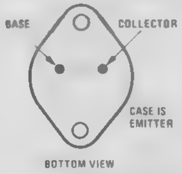
- Internal thermal limiting
- Greater than 1.0 A output current
- 3.0 μA typical base current
- 500 ns switching time
- 2.0 V saturation
- Base can be driven up to 40 V without damage
- Directly interfaces with CMOS or TTL

Simplified Circuit and Connection Diagrams

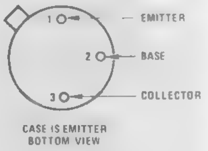


Simplified Circuit of the LM195

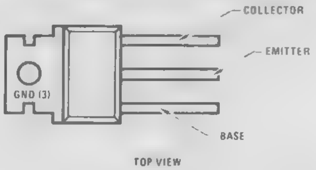
TO-3 Metal Can Package



TO-5 Metal Can Package



TO-220 Power Package



Absolute Maximum Ratings

Collector to Emitter Voltage	
LM195, LM295	42V
LM395	36V
Collector to Base Voltage	
LM195, LM295	42V
LM395	36V
Base to Emitter Voltage (Forward)	
LM195, LM295	42V
LM395	36V
Base to Emitter Voltage (Reverse)	20V
Collector Current	Internally Limited
Power Dissipation	Internally Limited
Operating Temperature Range	
LM195	−55°C to +150°C
LM295	−25°C to +150°C
LM395	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

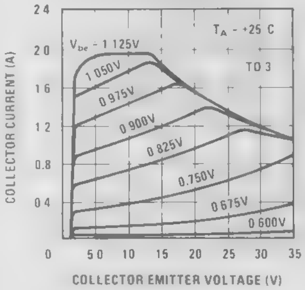
PARAMETER	CONDITIONS	LM195, LM295			LM395			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector Emitter Operating Voltage	$I_Q < I_C < I_{MAX}$			42			36	V
Base to Emitter Breakdown Voltage	$0 < V_{CE} \leq V_{CEMAX}$	42			36	60		v
Collector Current								
TO-3	$V_{CE} < 15V$	1.2	2.0		1.0	2.0		A
TO-5	$V_{CE} < 7.0V$	1.2	2.0		1.0	2.0		A
TO-220	$V_{CE} \leq 15V$				1.0	2.0		A
Saturation Voltage	$I_C \leq 1.0A$		1.8	2.0		1.8	2.2	v
Base Current	$0 < I_C < I_{MAX}$ $0 < V_{CE} < V_{CEMAX}$		3.0	5.0		3.0	10	μA
Quiescent Current	$V_{be} = 0$ $0 \leq V_{CE} < V_{CEMAX}$		2.0	5.0		2.0	10	mA
Base to Emitter Voltage	$I_C = 1.0A$, $T_A = +25°C$		0.9			0.9		V
Switching Time	$V_{CE} = 36V$, $R_L = 36\Omega$, $T_A = +25°C$		500			500		ns
Thermal Resistance Junction to Case (Note 2)	TO-3 Package		2.3	3.0		2.3	3.0	°C/W
	TO-5 Package		12	15		12	15	°C/W

Note 1: Unless otherwise specified, these specifications apply for $-55°C \leq T_j \leq +150°C$ for the LM195, $-25°C \leq T_j \leq +150°C$ for the LM295 and $0°C \leq +125°C$ for the LM395.

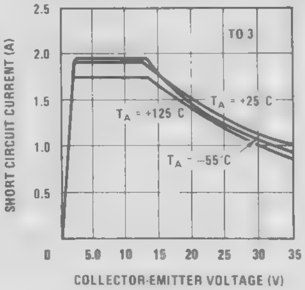
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about +150°C/W, while that of the TO-3 package is +35°C/W.

Typical Performance Characteristics

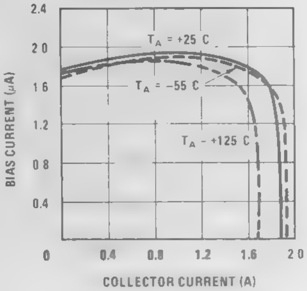
Collector Characteristics



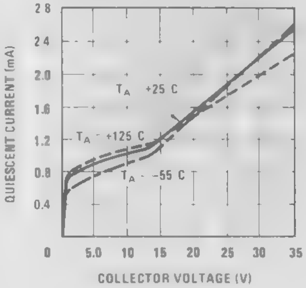
Short Circuit Current



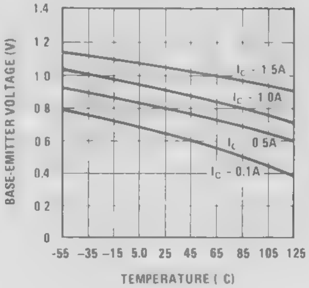
Bias Current



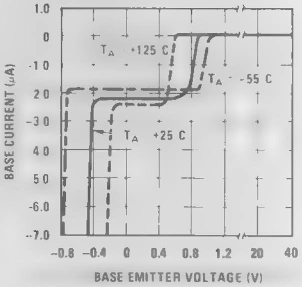
Quiescent Current



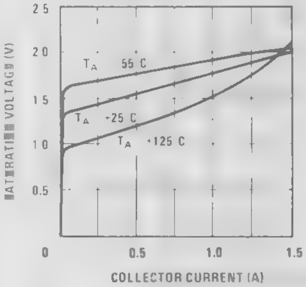
Base Emitter Voltage



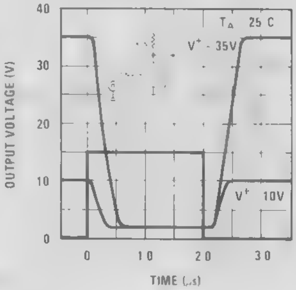
Base Current



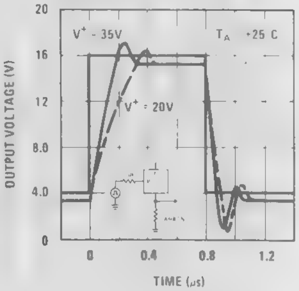
Saturation Voltage



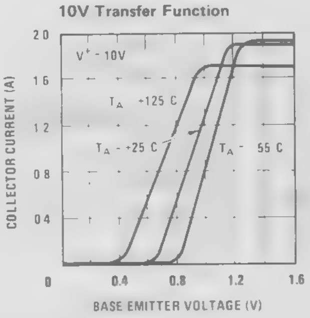
Response Time

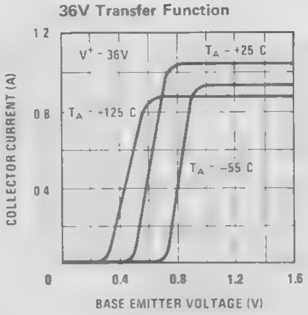


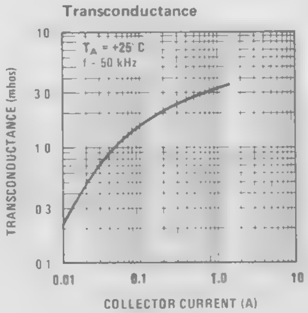
Response Time

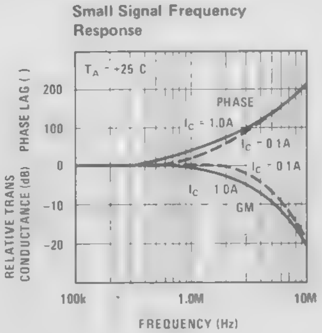


Typical Performance Characteristics (Cont'd.)

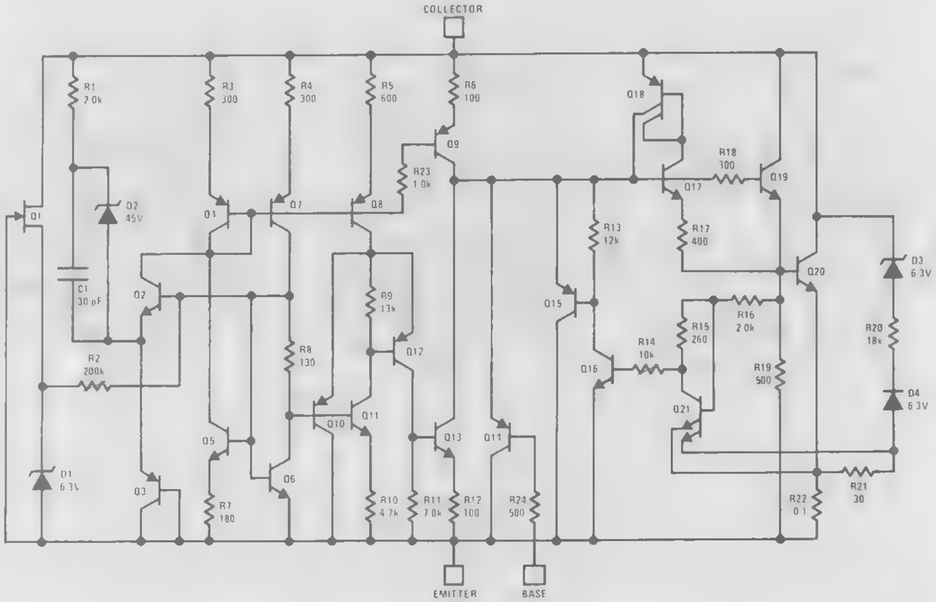

10V Transfer Function

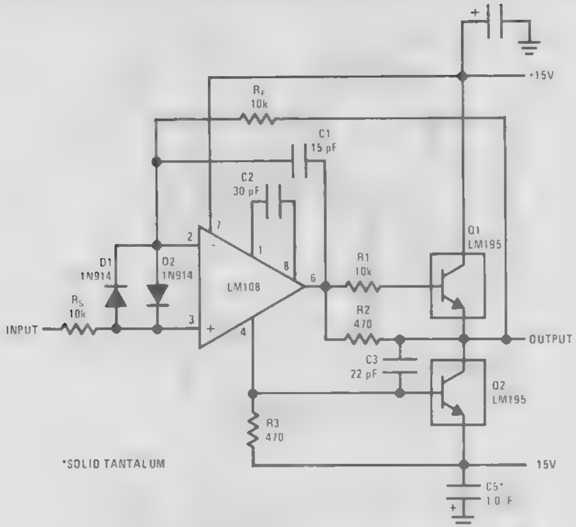

36V Transfer Function


Transconductance


Small Signal Frequency Response

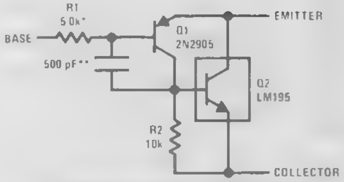
Schematic Diagram





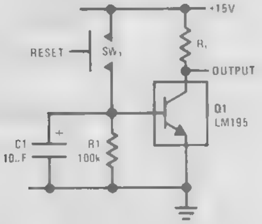
*SOLID TANTALUM

1.0 Amp Voltage Follower

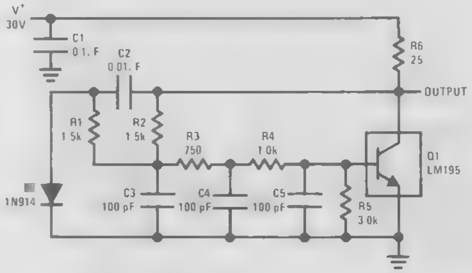


*PROTECTS AGAINST EXCESSIVE BASE DRIVE
**NEEDED FOR STABILITY

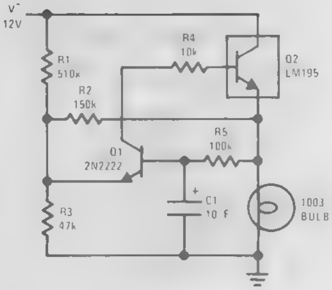
Power PNP



Time Delay

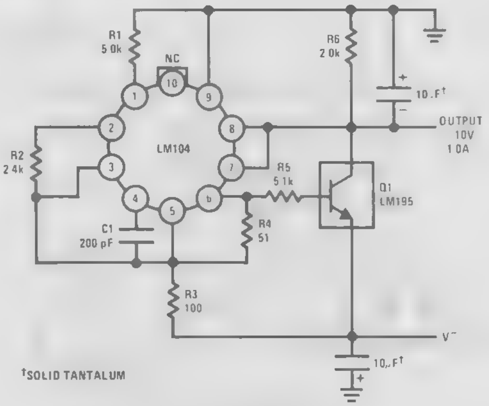


1.0 MHz Oscillator



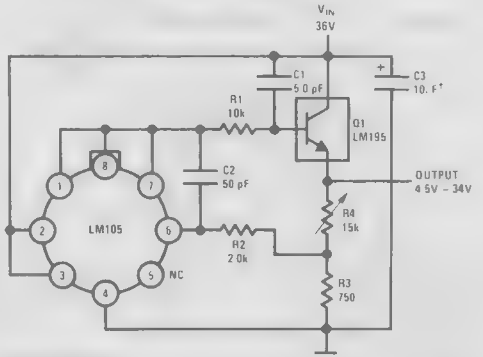
1.0 Amp Lamp Flasher

Typical Applications (Cont'd.)



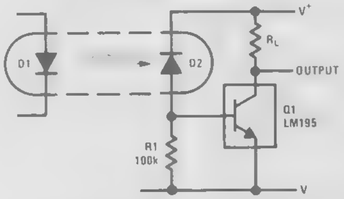
†SOLID TANTALUM

1.0 Amp Negative Regulator

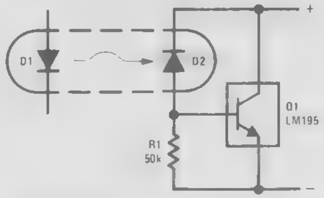


†SOLID TANTALUM

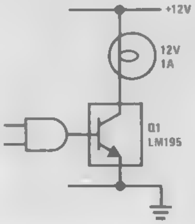
1.0 Amp Positive Voltage Regulator



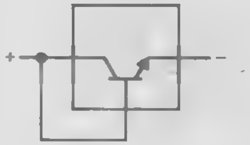
Fast Optically Isolated Switch



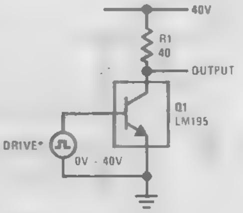
Optically Isolated Power Transistor



CMOS or TTL Lamp Interface



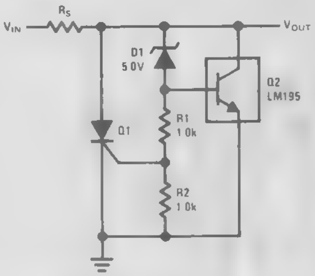
Two Terminal Current Limiter



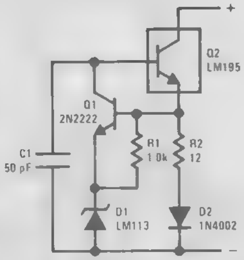
*DRIVE VOLTAGE 0V TO 1.0V 42V

40V Switch

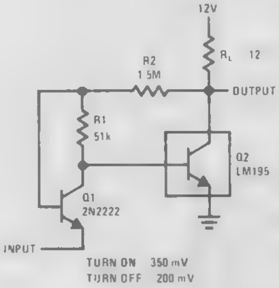
Typical Applications (Cont'd.)



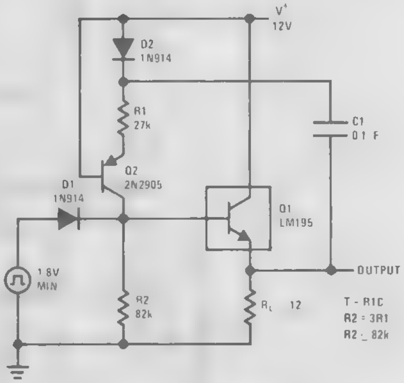
6.0V Shunt Regulator with Crowbar



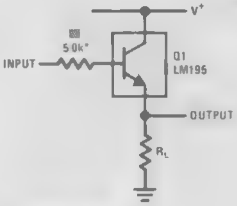
Two Terminal 100 mA Current Regulator



Low Level Power Switch

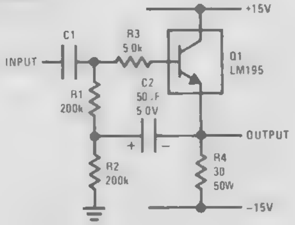


Power One-Shot

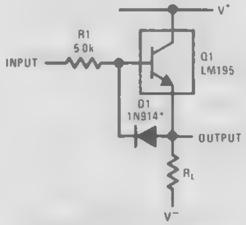


*NEED FOR STABILITY

Emitter Follower



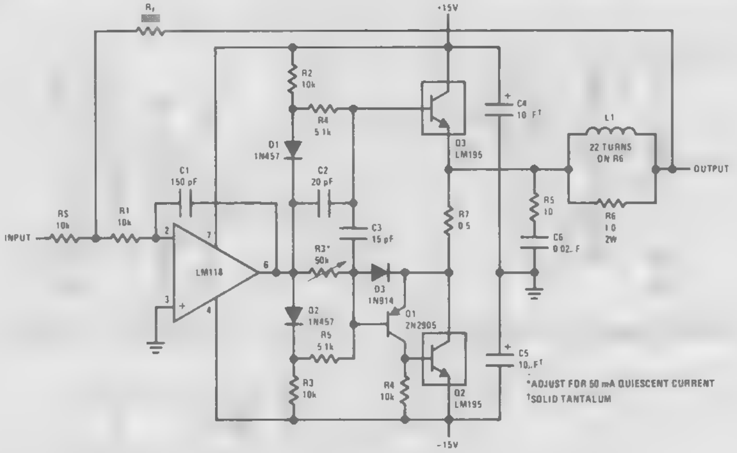
High Input Impedance AC Emitter Follower



*PREVENTS STORAGE WITH FAST FALL TIME SQUARE WAVE DRIVE

Fast Follower

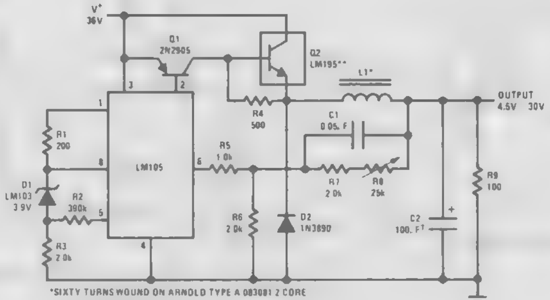
Typical Applications (Cont'd.)



*ADJUST FOR 50 mA QUIESCENT CURRENT

†SOLID TANTALUM

Power Op Amp



*SIXTY TURNS WOUND ON ARNOLD TYPE A 083081 2 CORE

**FOUR DEVICES IN PARALLEL

†SOLID TANTALUM

6.0 Amp Variable Output Switching Regulator

Section 7

High Reliability/Radiation Hardened CMOS Programs

National Semiconductor

883B/RETS™ Program

The National Semiconductor 883B/RETS™ Program was conceived with the intent of offering our customers a standardized, off-the-shelf, integrated circuit fully compliant to the current revision of MIL-STD-883.

The following specification outlines the program qualification, quality conformance and processing requirements. Records and data substantiating the testing as specified herein are controlled and administered through National Semiconductor Quality Assurance and Reliability group (located in Santa Clara, California) and are available for review.

As a complement to this program, the National Quality system is designed to encompass the requirements of MIL-Q-9858 and associated documents.

Tom Griffiths, Director
Quality Assurance and Reliability
National Semiconductor Corporation

1.0 Scope

1.1 Purpose

This specification establishes the requirements for screening and processing of integrated circuits in accordance with MIL-STD-883, Class B.

1.2 Intent

This specification is intended to provide the user with the ability to procure standardized, off-the-shelf integrated circuits manufactured by National Semiconductor Corporation that are fully compliant to MIL-STD-883.

2.0 Applicable Documents

The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

2.1 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits
MIL-C-45662	Calibration System Requirements
MIL-Q-9858	Quality System Requirements

2.2 Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.3 Detail Specifications

The detail specification for a particular 883B/RETS^{TM} microcircuit is the manufacturer's RETS (Reliability Electrical Test Specification, see *Figure 2*).

3.0 General Requirements

The individual requirements shall be as specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements and electrical test methods shall be as specified in the detail specification.

3.1 Process Conditioning, Testing, Reliability and Quality Assurance Screening

Process conditioning, screening and testing shall be as specified in Section 4.0.

MIL-STD-883 Q.A. Process Level	Applicable Process Flow Chart	Suffix Level Indicator
B	*Figure 1a*	/883B

3.1.1 Qualification

The 883B/RETS^{TM} microcircuits furnished under this specification shall be products which have been produced and tested and have passed the qualification tests specified herein. Successful qualification for a given level results in qualification approval for that level and all lower products assurance levels of that device (reference appendix E MIL-M-38510D).

3.1.2 Alternate Qualification

In lieu of meeting the requirements of 3.1.1, the manufacturer may establish qualification by performing an initial, one time qualification test. Qualification testing shall be performed on each generic family supplied. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 months.

3.2 Quality Conformance Inspection

The 883B/RETS^{TM} microcircuits furnished under this specification shall be products which have been produced and tested in conformance with all the provisions of this specification for the applicable level. Devices which have been accepted as conforming to a given product assurance level may be furnished as conforming to any other level for which they meet or exceed the quality conformance requirements.

3.3 Marking

3.3.1 Marking on Each Device

The following marking shall be placed on each microcircuit:

a) Index point (see 3.3.4)
b) Part number (see 3.3.5)
c) Product assurance level (see 3.3.6)
d) Inspection lot identification code (see 3.3.8)
e) Manufacturer's Identification (see 3.3.9)

3.3.2 Marking on Initial Container

All of the marking specified in 3.3.1, except the index point, shall appear on the initial protection or wrapping for delivery.

3.3.3 Marking Permanence

Marking shall be permanent in nature and remain legible after testing. Damage to marking caused by mechanical fixturing in Group B and C tests shall not be cause for lot rejection.

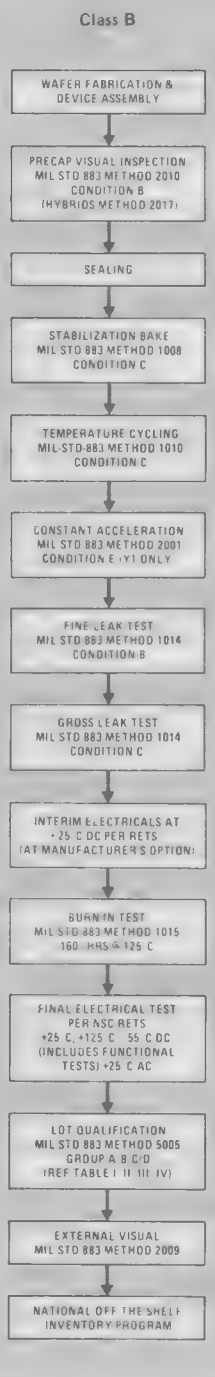

Class B
WAFER FABRICATION & DEVICE ASSEMBLY
PRECAP VISUAL INSPECTION MIL STD 883 METHOD 2010 CONDITION B (HYBRIDS METHOD 2017)
SEALING
STABILIZATION BAKE MIL STD 883 METHOD 1008 CONDITION C
TEMPERATURE CYCLING MIL-STD-883 METHOD 1010 CONDITION C
CONSTANT ACCELERATION MIL STD 883 METHOD 2001 CONDITION E (Y1 ONLY
FINE LEAK TEST MIL STD 883 METHOD 1014 CONDITION B
GROSS LEAK TEST MIL STD 883 METHOD 1014 CONDITION C
INTERIM ELECTRICALS AT +25 C DC PER RETS (AT MANUFACTURER S OPTION)
BURN IN TEST MIL STD 883 METHOD 1015 160 HRS @ 125 C
FINAL ELECTRICAL TEST PER NSC RETS +25 C, +125 C 55 C DC (INCLUDES FUNCTIONAL TESTS) +25 C AC
LOT QUALIFICATION MIL STD 883 METHOD 5005 GROUP A B C/D (REF TABLE I II III IV)
EXTERNAL VISUAL MIL STD 883 METHOD 2009
NATIONAL OFF THE SHELF INVENTORY PROGRAM

FIGURE 1. MIL-STD-883 Screening

RETS4001BX
Revision C

Burn-In Circuits:
DIP: 8900HR; FLAT: 9118HR

Test System: **Teradyne J-283**
RC4601BXRB RC4601BXHB RC4601BXLB

NOTES	Parameter	Symbol	Test Conditions (Unless Otherwise Specified)	Test Number	Subgroup 1 +25°C Min	Subgroup 1 +25°C Max	Subgroup 2 +125°C Min	Subgroup 2 +125°C Max	Subgroup −55°C Min	Subgroup −55°C Max
	Logical "0" Output Voltage	V_{OL}	V_{DD} = 10V, I_{OUT} = 0μA, V_{IH} = 10V, V_{IL} = 0V	120, 121		0.05		0.05		0
			V_{DD} = 5V, I_{OUT} = 0μA, V_{IH} = 5V, V_{IL} = 0V	112, 113		0.05		0.05		0
			V_{DD} = 15V, I_{OUT} = 0μA, V_{IH} = 15V, V_{IL} = 0V	126, 127		0.05		0.05		0.0
	Logical "1" Output Voltage	V_{OH}	V_{DD} = 10V, I_{OUT} = 0μA, V_{IH} = 10V, V_{IL} = 0V	70, 71	9.95		9.95		9.95	
			V_{DD} = 15V, I_{OUT} = 0μA, V_{IH} = 15V, V_{IL} = 0V	76, 77	14.95				14.95	
			V_{DD} = 5V, I_{OUT} = 0μA, V_{IH} = 5V, V_{IL} = 0V	62, 63	4.95		4.95		4.95	
	Logical "1" Input Current	I_{IH}	V_{DD} = 15V, V_{IN} = 15V (all inputs tied)	33		100		1000		10
	Logical "0" Input Current	I_{IL}	V_{DD} = 15V, V_{IN} = 0V (all inputs tied)	34		100		-1000		10
	Output Source Current	I_{SOURCE}	V_{DD} = 15V, V_{OUT} = 13.5V, V_{IH} = 15V, V_{IL} = 0V	74, 75	3.4		2.4		4.2	
			V_{DD} = 10V, V_{OUT} = 9.5V, V_{IH} = 10V, V_{IL} = 0V	66, 67	1.3		0.9		1.6	
			V_{DD} = 5V, V_{OUT} = 4.6V, V_{IH} = 5V, V_{IL} = 0V	56, 57	0.51		0.36		0.64	
			V_{DD} = 5V, V_{OUT} = 0V, V_{IH} = 5V, V_{IL} = 0V	60, 61	1.85		1.26		2.2	
	Output Sink Current	I_{SINK}	V_{DD} = 15V, V_{OUT} = 1.5V, V_{IH} = 15V, V_{IL} = 0V	124, 125	3.4		2.4		4.2	
			V_{DD} = 10V, V_{OUT} = 0.5V, V_{IH} = 10V, V_{IL} = 0V	116, 117	1.3		0.9		1.6	
			V_{DD} = 5V, V_{OUT} = 0.4V, V_{IH} = 5V, V_{IL} = 0V	102-105	0.51		0.36		0.64	
			V_{DD} = 5V, V_{OUT} = 5V, V_{IH} = 5V, V_{IL} = 0V	106-111	2.06		1.4		2.2	
	Power Supply Current	I_{DD}	V_{DD} = 15V, V_{IH} = 15V, V_{IL} = 0V	42-45		1.0		30		1.0
			V_{DD} = 10V, V_{IH} = 10V, V_{IL} = 0V	46-51		0.5		15		0.5
			V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V	52-55		0.25		7.5		0.2
			V_{DD} = 18V, V_{IH} = 18V, V_{IL} = 0V	36-41		50				
1 4	Logical "1" Input Current	V_{IH}	V_{DD} = 5V, V_{OUT} = 4.5V, (min)	(64, 65)	3.5		3.5		3.5	
			V_{DD} = 10V, V_{OUT} = 9.0V (min)	(72, 73)	7		7		7	
			V_{DD} = 15V, V_{OUT} = 13.5V (min)	(100, 101)	11		11		11	
1 4	Logical "0" Input Voltage	V_{IL}	V_{DD} = 5V, V_{OUT} = 0.5V (max)	(130B, 131B)		1.5		1.5		1.5
			V_{DD} = 10V, V_{OUT} = 1.0V (max)	(122, 123)		3		3		3
			V_{DD} = 15V, V_{OUT} = 1.5V (max)	(130A, 131A)		4		4		4
			Note 4: V_{OUT} is measured with inputs at V_{IH}, V_{IL}							
					subgroup 4					
2	Input Capacitance	C_{IN}				7.5				
					subgroup 9					
3	Propagation Delay Time	t_{pd0}, t_{pd1}	V_{DD} = 5V			250				
3	Transition Time	t_{t0}, t_{t1}	V_{DD} = 5V			200				
2	Propagation Delay Time	t_{pd0}, t_{pd1}	V_{DD} = 10V			100				
			V_{CC} = 15V			70				
2	Transition Time	t_{t0}, t_{t1}	V_{DD} = 10V			100				
			V_{DD} = 15V			80				

Note 1 Parameter tested go no go only, cannot be data logged

Note 2 Guaranteed parameter, no testing is available

Note 3. Guaranteed parameter, may be tested only on a s

Device: CD4001BM (MM4601B) **Function:** CMOS Buffered Quad 2-Input NOR Gate

RETS54C00X
Revision A

Burn-In-Circuits:
DIP: 8900HR; FLAT: 9118HR

Test System: **Teradyne J-283**
RC54C00BRA RC54C00BHA RC54CBLA

NOTES	Parameter	Symbol	Test Conditions (Unless Otherwise Specified)	Test Number	Subgroup 1 +25°C		Subgroup 2 +125°C		Subgroup 3 −55°C		Optional Drift Δ Limits (25°C)	Units of Measure
					Min	Max	Min	Max	Min	Max		
	Logical "1" Output Voltage	V_{OH}	V_{CC} = 5V, I_{OUT} = −10μA, V_{IN} = 1.5V (all inputs)	45	4.5		4.5		4.5			V
			V_{CC} = 10V, I_{OUT} = −10μA, V_{IN} = 2V (all inputs)	47	9.0		9.0		9.0			V
			V_{CC} = 4.5V, I_{OUT} = −360μA, V_{IN} = 1V (all inputs)	43	2.4		2.4		2.4			V
	Logical "0" Output Voltage	V_{OL}	V_{CC} = 5V, I_{OUT} = 10μA, V_{IN} = 3.5V (all inputs)	46		0.5		0.5		0.5		V
			V_{CC} = 10V, I_{OUT} = 10μA, V_{IN} = 8V (all inputs)	50		1.0		1.0		1.0		V
			V_{CC} = 4.5V, I_{OUT} = 360μA, V_{IN} = 4V (all inputs)	44		0.4		0.4		0.4		V
	Logical "1" Input Current	I_{IH}	V_{CC} = 15V, V_{IN} = 15V, other inuts at 0V	33		.15		1.0		.15		μA
	Logical "0" Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V, other inputs at 15V	34		−.15		−1.0		−.15		μA
	Quiescent Device Current	I_{CC}	V_{CC} = 15V, V_{IH} = 15V, V_{IL} = 0V	40, 41, 42		.15		15		15	±.05	μA
	Output Source Current	I_{SOURCE}	V_{CC} = 5V, V_{OUT} = 0V, V_{IN} = 5V (1 input per gate, other inputs at 0V)	51, 52	−1.75		−1.2		−1.75		± 5	mA
			V_{CC} = 10V, V_{OUT} = 0V, V_{IN} = 10V (1 input per gate, other inputs at 0V)	53, 54	−8.0		−5.6		8.0			mA
	Output Sink Current	I_{SINK}	V_{CC} = 5V, V_{OUT} = 5V, V_{IN} = 5V (all inputs)	55	1.75		1.20		1.75		±.5	mA
			V_{CC} = 10V, V_{OUT} = 10V, V_{IN} = 10V (all inputs)	56	8.0		5.6		8.0			mA
			V_{CC} = 4.5V, V_{OUT} = .4V, V_{IN} = 4V (all inputs)	57	360		360		360			μA
1	Logical "1" Input Voltage	V_{IH}	V_{CC} = 5V		3.5		3.5		3.5			V
			V_{CC} = 10V		8.0		8.0		8.0			V
			V_{CC} = 4.5V (LP to CMOS)		3.0		3.0		3.0			V
			V_{CC} = 4.5V (CMOS to LP)		4.0		4.0		4.0			V
1	Logical "0" Input Voltage	V_{IL}	V_{CC} = 5V			1.5		1.5		1.5		V
			V_{CC} = 10V			2.0		2.0		2.0		V
			V_{CC} = 4.5V (LP to CMOS)			0.8		0.8		0.8		V
			V_{CC} = 4.5V (CMOS to LP)			1.0		1.0		1.0		V
1	Power Dissipation	P_D	V_{CC} = 15V			2.25		225		2.25		μW
2	Logical "1" Output Voltage	V_{OH}	V_{CC} = 4.5V, , I_{OUT} = −10μA		4.4		4.4		4.4			V
2	Logical "0" Output Voltage	V_{OL}	V_{CC} = 4.5V, I_{OUT} = 10μA			0.4		0.4		0.4		V
					subgroup 9							
3	Propagation Delay Time	t_{pd1}	V_{CC} = 5V, C_L = 50pF			90						ns
		t_{pd0}	V_{CC} = 5V, C_L = 50pF			90						ns
2	Propagation Delay Time	t_{pd1}	V_{CC} = 10V, C_L = 50pF			60						ns
		t_{pd0}	V_{CC} = 10V, C_L = 50pF			60						ns

Note 1 Parameter tested go no go only, cannot be data logged.
Note 2 Guaranteed parameter, no testing is available
Note 3. Guaranteed parameter, may be tested only on a special order basis

Device: MM54C00
Function: CMOS Quad 2-Input NAND Gate

3.3.4 Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

3.3.5 Part Number

The part number shall be the manufacturer's generic part number.

3.3.6 Product Assurance Level

Integrated circuits shall be marked with a code indicating the product assurance level to which they have been tested and found to conform. The code shall consist of /883 followed by the letter B.

3.3.7 Formation of Lots

Microcircuits shall be assembled into inspection lots as required to meet the product assurance inspection and test requirements of this specification. An inspection sublot shall consist of microcircuits of a single type contained on a single detail specification, manufactured on the same production line(s) through final seal by the same product techniques, and to the same device design rules and package with the same material requirements, and within the same period not exceeding 6 weeks.

3.3.8 Inspection Lot Identification Code

Integrated circuits shall be marked by a 4-digit date code indicating the date the lot was submitted for inspection. The first 2 numbers in the code shall be the last 2 digits of the number of the year. The third and fourth numbers shall be 2 digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right, the code number shall designate year, year, week, week.

3.3.9 Manufacturer's Identification

Integrated circuits shall be marked with the name, logo, or trademark of the manufacturer.

4.0 Conditions and Methods of Test

Conditions and methods of test shall be in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application.

4.1 Internal Visual Inspection (Precap)

Internal visual inspection shall be performed per MIL-STD-883, Method 2010, Condition B. Hybrid internal visual shall be performed per Method 2017.

4.2 Stabilization Bake

Stabilization bake shall be performed per MIL-STD-883, Method 1008, Condition C. The devices shall be stored for 24 hours minimum at 150°C minimum. No end point measurements shall be performed.

4.3 Temperature Cycling

Temperature cycling shall be performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from −65°C to +150°C.

4.4 Constant Acceleration

Constant acceleration shall be performed per MIL-STD-883, Method 2001. Condition E, at 30,000 G's, in Y1 plane only.

4.5 Hermeticity

Hermeticity tests shall be performed per the following:

Fine Leak Testing

Fine leak testing shall be performed per MIL-STD-883, Method 1014, Condition B. The criterion for rejection will be in accordance with MIL-STD-883.

Gross Leak Testing

Gross leak testing shall be performed per MIL-STD-883, Method 1014, Condition C. The rejection criterion will be per MIL-STD-883.

4.6 Interim Electrical Parameters

Interim electrical parameters shall be the 25°C DC parameters, specified in the detail specification (RETS). (Interim electrical parameters are performed at the manufacturer's option.) .

4.7 Burn-In

Burn-in shall be performed per MIL-STD-833, Method 1015; Conditions A, B, C or D on all Class B devices. (Burn-in condition varies with product type.)

The ambient temperature shall be 125°C.

4.8 Final Electrical Parameters

Final electrical parameters shall be as specified in the applicable detail specification (RETS). DC testing shall be performed at 25°C, −55°C, 125°C. AC testing shall be performed at 25°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to DC measurements at 25°C.

4.9 External Visual Inspection

All 883B/RETS™ microcircuits shall receive external visual inspection per MIL-STD-883, Method 2009.

5.0 Quality Assurance Provisions

5.1 Quality Conformance Inspection

Quality conformance inspection shall be in accordance with Tables I, II, III and IV. Inspection lot sampling shall be in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for a given product assurance level shall be rejected.

5.1.1 Group A Inspection

Group A inspection shall consist of the electrical parameters in the RETS (Reliability Electrical Test Specification). If an inspection lot is made up of a collection of sublots, each sublot shall be subjected to Group A, as specified, (see Table 1).

5.1.2 Group B Inspection

Group B inspection consists of construction testing. This sample test sequence includes physical dimensions, resistance to solvents, internal visual and mechanical, bond strength and solderability (see Table II). The Group B qualifies the inspection sublot the sample is pulled from. It also qualifies all generically similar devices if the date code is within 6 weeks of the sample date code.

5.1.3 Group C Inspection

Group C inspection consists of die stress testing. This sample test sequence includes operating life, temperature cycling, constant acceleration, hermeticity, visual examination and end point electricals (see Table III). A Group C qualifies the lot the sample is pulled from and all generically similar die types for a period of 90 days.

5.1.4 Group D Inspection

Group D testing further stresses the package and the die. The Group D tests include physical dimensions, lead integrity, hermeticity, thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration variable frequency, constant acceleration, salt atmosphere, visual examination, and end point electricals (see Table IV). A Group D qualifies the lot the sample is pulled from and all devices built in the same package for a period of 6 months.

TABLE I. GROUP A ELECTRICAL TEST

SUBGROUPS	CLASS B LTPD
Subgroup 1 Static tests at 25°C	5
Subgroup 2 Static tests at maximum rated operating temperature	7
Subgroup 3 Static tests at minimum rated operating temperature	7
Subgroup 4 Dynamic tests at 25°C	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	7
Subgroup 6 Dynamic tests at minimum rated operating temperature	7
Subgroup 7 Functional tests at 25°C	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperature	10
Subgroup 9 Switching tests at 25°C	7

TABLE IV. GROUP D INSPECTION

TEST	METHOD	CONDITIONS	CLASS B LTPD (MAX ACC = 1)
Subgroup 1			
Physical dimensions	2016		15
Internal water vapor	1018		3 devices (No failures)
Subgroup 2			
Lead integrity	2004	Test conditions B2 (lead fatigue)	
Seal	1014	As applicable	
Fine			
Gross			
Subgroup 3			
Thermal shock	1011	Test condition B – 15 cycles	15
Temperature cycling	1010	Test condition C – 100 cycles	
Moisture resistance	1004		
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1004		
End point electrical parameters		As specified in the applicable device specification (+25°C)	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration variable freq.	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y, Axis	
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1010 or 1011		
End point electrical parameters		As specified in the applicable device specification (+25°C)	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Seal	1014	As applicable	
Visual examination	1009	Paragraph 3.3.1 of Method 1009	

TABLE II. GROUP B INSPECTION

TEST	METHOD	CONDITIONS	CLASS B
Subgroup 1 Physical dimension	2016		2 devices (No failures)
Subgroup 2 a) Resistance to solvents	2015		3 devices (No failures)
Subgroup 3 Solderability	2003	Soldering temperature of 260±10°C	15 leads (3 units min No failures)
Subgroup 4 Internal visual and mechanical	2014	Failure criteria from design & construction requirements of applicable procurement document	1 device (No failures)
Subgroup 5 Bond strength	2011	Test condition C or D	15 Bonds (10 units min No failures)

TABLE III. GROUP C INSPECTION

TEST	METHOD	CONDITIONS	CLASS B LTPD (MAX ACC = 1)
Subgroup 1			
Operating Life Test	1005	Test conditions to be specified 1000 hours @ +125°C	5
End point electricals		as specified in the applicable detail specification (+25°C)	
Subgroup 2			
Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E, Y1 axis	
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1010		
End point electrical parameters		As specified in applicable device specification (+25°C)	

883 PROCESS FLOW

TEST	MIL-STD-883 METHOD	TTL, LS, LOW POWER CMOS, LINEAR, MOS/LSI, MEMORY	HYBRID
Internal visual	2010, Cond. B	100%	100% (Method 2017)
Bake	1008, Cond. C	100%	100%
Temperature cycling	1010, Cond. C	100%	100%
Constant acceleration	2001, Cond. E	100%	100%
Fine leak	1014, Cond. B	100%	100%
Gross leak	1014, Cond. C	100%	100%
Burn-in	1015, Cond. A, B, C or D	100%	100%
Electrical test	Per the applicable detail specification	100% RETS	
Group A		LTPD Sample (RETS)	
External visual	2009	100%	100%

6.0 DATA

6.1 Certificate of Conformance

All 883B/RETS™ microcircuits shipped shall be accompanied by a Certificate of Conformance as shown on the opposite page.

6.2 Attributes Data

Attributes data for 100% screening will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

6.3 Quality Conformance Data

Quality conformance data will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

883B/RETS™ MICROCIRCUITS FROM National Semiconductor Corporation

CERTIFICATE OF CONFORMANCE

TEST	MIL-STD-883 METHOD**	REQUIREMENT
INTERNAL VISUAL	2010B	100%
STABILIZATION BAKE	1008 C 24 HRS @ +150°C	100%
TEMPERATURE CYCLING	1010 C 10 CYCLES −65°C/+150°C	100%
CONSTANT ACCELERATION	2001 E	100%
FINE LEAK	1014 B 5×10^{-8}	100%
GROSS LEAK	1014 C2	100%
BURN-IN	1015 160 HRS @ +125°C	100%
FINAL ELECTRICAL	+25°C DC PER NSC RETS	100%
PDA	10% MAX ALLOWABLE	
	+125°C DC PER NSC RETS	100%
	−55°C DC PER NSC RETS	100%
	+25°C AC PER NSC RETS	100%
QA ACCEPTANCE	LTPD SAMPLE	
EXTERNAL VISUAL	2009	100%

* RETS = REL ELECTRICAL TEST SPECIFICATION

** All METHODS TO CURRENT REVISION LEVELS

THIS IS TO CERTIFY THAT ALL 883B/RETS™ MICROCIRCUITS SUPPLIED TO YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS AND DOCUMENTS PERTINENT TO NATIONAL'S 883B/RETS™ MICROCIRCUIT PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

Part Number ____________________

P.O. Number ____________________

Date Code(s) ____________________

Lot Code(s) ____________________

____

QUALITY ASSURANCE REPRESENTATIVE

National Semiconductor

1.0 Scope

1.1 Purpose

This document establishes the requirements for screening and processing of integrated circuits in accordance with MIL-STD-883, Class S where such devices are not available as M38510 Class S devices. These products shall be referred to as 883S/RETS™ microcircuits.

1.2 Intent

This program is intended to provide the user with the ability to procure 883S/RETS™ microcircuits. These are standardized integrated circuits manufactured and processed by National Semiconductor Corporation in accordance with the requirements of MIL-STD-883, for Class S devices.

2.0 Applicable Documents

The following specifications and standards of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

2.1 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits
MIL-C-45662	Calibration System Requirements
MIL-Q-9858	Quality System Requirements
MIL-STD-1331	Microelectronics Terms and Definitions

2.2 Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Prodedure for Microelectronics
MIL-STD-976	Certification Requirements for Microcircuits

2.3 Detail Specifications

The detail specification for a particular device is the National Semiconductor RETS (Reliability Electrical Test Specification, see Figure 1). The RETS is a one page translation of the National Semiconductor electrical test programs used to test 883B/RETS™ and 883S/RETS™ microcircuits. For devices available as JM38510, Class S, the detail specification shall be the applicable MIL-M-38510 slash sheet, and all applicable requirements of MIL-M-38510 shall apply.

3.0 Requirements

3.1 General

The individual requirements shall be as specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements for the integrated circuits and electrical test methods shall be as specified in the detail specification.

3.1.1 Conflicting Requirements

In the event of conflict between the requirements of this specification and other requirements of the applicable device specification, the precedence in which requirements shall govern, in decending order, is as follows:

a) Applicable device specification (detail specification).
b) This specification.
c) Specifications, standards, and other documents referenced in 2.1.

3.1.2 Terms, Definitions, and Symbols

For the purpose of this specification, the terms, definitions, and symbols of MIL-STD-883, MIL-STD-1331, and paragraph 3.1.3 of MIL-M-38510 shall apply and shall be used wherever they are pertinent, except as follows:

a) Procuring Activity (see MIL-M-38510, paragraph 3.1.3 (n)) shall be that organization (either OEM manufacturer or government agency) which generates the actual purchase order or contract used to procure material under this specification. For material purchased through a franchised distributor, the procuring activity shall be that organization which places the purchase order or contract with the distributor.

b) The Qualifying Activity (see MIL-M-38510, paragraph 3.1.3 (o)) shall be National's Quality Assurance Department.

RETS4001BX
Revision C

Burn-In-Circuits:
DIP: 8900HR; FLAT: 9118HR

Test System: **Teradyne J-283**
RC4601BXRB RC4601BXHB RC4601BXLB

NOTES	Parameter	Symbol	Test Conditions (Unless Otherwise Specified)	Test Number	Subgroup 1 +25°C		Subgroup 2 +125°C		Subgroup 3 −55°C		Optional Drift Δ Limits (25°C)	Units of Measure
					Min	Max	Min	Max	Min	Max		
	Logical "0" Output Voltage	V_{OL}	$V_{DD} = 10V, I_{OUT} = 0\mu A, V_{IH} = 10V, V_{IL} = 0V$	120, 121		0.05		0.05		0.05		V
			$V_{DD} = 5V, I_{OUT} = 0\mu A, V_{IH} = 5V, V_{IL} = 0V$	112, 113		0.05		0.05		0.05		V
			$V_{DD} = 15V, I_{OUT} = 0\mu A, V_{IH} = 15V, V_{IL} = 0V$	126, 127		0.05		0.05		0.05		V
	Logical "1" Output Voltage	V_{OH}	$V_{DD} = 10V, I_{OUT} = 0\mu A, V_{IH} = 10V, V_{IL} = 0V$	70, 71	9.95		9.95		9.95			V
			$V_{DD} = 15V, I_{OUT} = 0\mu A, V_{IH} = 15V, V_{IL} = 0V$	76, 77	14.95				14.95			V
			$V_{DD} = 5V, I_{OUT} = 0\mu A, V_{IH} = 5V, V_{IL} = 0V$	62, 63	4.95		4.95		4.95			V
	Logical "1" Input Current	I_{IH}	$V_{DD} = 15V, V_{IN} = 15V$ (all inputs tied)	33		100		1000		100		nA
	Logical "0" Input Current	I_{IL}	$V_{DD} = 15V, V_{IN} = 0V$ (all inputs tied)	34		−100		−1000		−100		nA
	Output Source Current	I_{SOURCE}	$V_{DD} = 15V, V_{OUT} = 13.5V, V_{IH} = 15V, V_{IL} = 0V$	74, 75	−3.4		−2.4		−4.2		±.75	mA
			$V_{DD} = 10V, V_{OUT} = 9.5V, V_{IH} = 10V, V_{IL} = 0V$	66, 67	−1.3		−0.9		−1.6			mA
			$V_{DD} = 5V, V_{OUT} = 4.6V, V_{IH} = 5V, V_{IL} = 0V$	56, 57	−0.51		−0.36		−0.64			mA
			$V_{DD} = 5V, V_{OUT} = 0V, V_{IH} = 5V, V_{IL} = 0V$	60, 61	−1.85		−1.26		−2.2			mA
	Output Sink Current	I_{SINK}	$V_{DD} = 15V, V_{OUT} = 1.5V, V_{IH} = 15V, V_{IL} = 0V$	124, 125	3.4		2.4		4.2		±.75	mA
			$V_{DD} = 10V, V_{OUT} = 0.5V, V_{IH} = 10V, V_{IL} = 0V$	116, 117	1.3		0.9		1.6			mA
			$V_{DD} = 5V, V_{OUT} = 0.4V, V_{IH} = 5V, V_{IL} = 0V$	102-105	0.51		0.36		0.64			mA
			$V_{DD} = 5V, V_{OUT} = 5V, V_{IH} = 5V, V_{IL} = 0V$	106-111	2.06		1.4		2.2			mA
	Power Supply Current	I_{DD}	$V_{DD} = 15V, V_{IH} = 15V, V_{IL} = 0V$	42-45		1.0		30		1.0	±.3	μA
			$V_{DD} = 10V, V_{IH} = 10V, V_{IL} = 0V$	46-51		0.5		15		0.5		μA
			$V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V$	52-55		0.25		7.5		0.25		μA
			$V_{DD} = 18V, V_{IH} = 18V, V_{IL} = 0V$	36-41		50						μA
1, 4	Logical "1" Input Current	V_{IH}	$V_{DD} = 5V, V_{OUT} = 4.5V$, (min)	(64, 65)	3.5		3.5		3.5			V
			$V_{DD} = 10V, V_{OUT} = 9.0V$ (min)	(72, 73)	7		7		7			V
			$V_{DD} = 15V, V_{OUT} = 13.5V$ (min)	(100, 101)	11		11		11			V
1, 4	Logical "0" Input Voltage	V_{IL}	$V_{DD} = 5V, V_{OUT} = 0.5V$ (max)	(130B, 131B)		1.5		1.5		1.5		V
			$V_{DD} = 10V, V_{OUT} = 1.0V$ (max)	(122, 123)		3		3		3		V
			$V_{DD} = 15V, V_{OUT} = 1.5V$ (max)	(130A, 131A)		4		4		4		V
			Note 4. V_{OUT} is measured with inputs at V_{IH}, V_{IL}									
					subgroup 4							
2	Input Capacitance	C_{IN}				7.5						pF
					subgroup 9							
3	Propagation Delay Time	t_{pd0}, t_{pd1}	$V_{DD} = 5V$			250						ns
3	Transition Time	t_{t0}, t_{t1}	$V_{DD} = 5V$			200						ns
2	Propagation Delay Time	t_{pd0}, t_{pd1}	$V_{DD} = 10V$			100						ns
			$V_{CC} = 15V$			70						ns
2	Transition Time	t_{t0}, t_{t1}	$V_{DD} = 10V$			100						ns
			$V_{DD} = 15V$			80						ns

Note 1 Parameter tested go no go only, cannot be data logged
Note 2 Guaranteed parameter no testing is available
Note 3 Guaranteed parameter, may be tested only on a special order basis

Device: CD4001BM (MM4601B) **Function:** CMOS Buffered Quad 2-Input NOR Gate

RETS54C00X
Revision A

Burn-In-Circuits:
DIP: 8900HR; FLAT: 9118HR

Test System: **Teradyne J-283**
RC54C00BRA RC54C00BHA RC54CBLA

NOTES	Parameter	Symbol	Test Conditions (Unless Otherwise Specified)	Test Number	Subgroup 1 +25°C Min	Subgroup 1 +25°C Max	Subgroup 2 +125°C Min	Subgroup 2 +125°C Max	Subgroup 3 −55°C Min	Subgroup 3 −55°C Max	Optional Drift Δ Limits (25°C)	Units of Measure
	Logical "1" Output Voltage	V_{OH}	$V_{CC} = 5V, I_{OUT} = -10\mu A, V_{IN} = 1.5V$ (all inputs)	45	4.5		4.5		4.5			V
			$V_{CC} = 10V, I_{OUT} = -10\mu A, V_{IN} = 2V$ (all inputs)	47	9.0		9.0		9.0			V
			$V_{CC} = 4.5V, I_{OUT} = -360\mu A, V_{IN} = 1V$ (all inputs)	43	2.4		2.4		2.4			V
	Logical "0" Output Voltage	V_{OL}	$V_{CC} = 5V, I_{OUT} = 10\mu A, V_{IN} = 3.5V$ (all inputs)	46		0.5		0.5		0.5		V
			$V_{CC} = 10V, I_{OUT} = 10\mu A, V_{IN} = 8V$ (all inputs)	50		1.0		1.0		1.0		V
			$V_{CC} = 4.5V, I_{OUT} = 360\mu A, V_{IN} = 4V$ (all inputs)	44		0.4		0.4		0.4		V
	Logical "1" Input Current	I_{IH}	$V_{CC} = 15V, V_{IN} = 15V$, other inuts at 0V	33		15		1.0		15		µA
	Logical "0" Input Current	I_{IL}	$V_{CC} = 15V, V_{IN} = 0V$, other inputs at 15V	34		-15		-1.0		-15		µA
	Quiescent Device Current	I_{CC}	$V_{CC} = 15V, V_{IH} = 15V, V_{IL} = 0V$	40, 41, 42		15		15		15	+.05	µA
	Output Source Current	I_{SOURCE}	$V_{CC} = 5V, V_{OUT} = 0V, V_{IN} = 5V$ (1 input per gate, other inputs at 0V)	51, 52	1.75		-1.2		-1.75		+5	mA
			$V_{CC} = 10V, V_{OUT} = 0V, V_{IN} = 10V$ (1 input per gate, other inputs at 0V)	53, 54	8.0		5.6		-8.0			mA
	Output Sink Current	I_{SINK}	$V_{CC} = 5V, V_{OUT} = 5V, V_{IN} = 5V$ (all inputs)	55	1.75		1.20		1.75		+5	mA
			$V_{CC} = 10V, V_{OUT} = 10V, V_{IN} = 10V$ (all inputs)	56	8.0		5.6		8.0			mA
			$V_{CC} = 4.5V, V_{OUT} = .4V, V_{IN} = 4V$ (all inputs)	57	360		360		360			µA
1	Logical "1" Input Voltage	V_{IH}	$V_{CC} = 5V$		3.5		3.5		3.5			V
			$V_{CC} = 10V$		8.0		8.0		8.0			V
			$V_{CC} = 4.5V$ (LP to CMOS)		3.0		3.0		3.0			V
			$V_{CC} = 4.5V$ (CMOS to LP)		4.0		4.0		4.0			V
1	Logical "0" Input Voltage	V_{IL}	$V_{CC} = 5V$			1.5		1.5		1.5		V
			$V_{CC} = 10V$			2.0		2.0		2.0		V
			$V_{CC} = 4.5V$ (LP to CMOS)			0.8		0.8		0.8		V
			$V_{CC} = 4.5V$ (CMOS to LP)			1.0		1.0		1.0		V
1	Power Dissipation	P_D	$V_{CC} = 15V$			2.25		225		2.25		µW
2	Logical "1" Output Voltage	V_{OH}	$V_{CC} = 4.5V, I_{OUT} = -10\mu A$		4.4		4.4		4.4			V
2	Logical "0" Output Voltage	V_{OL}	$V_{CC} = 4.5V, I_{OUT} = 10\mu A$			0.4		0.4		0.4		V
					subgroup 9							
3	Propagation Delay Time	t_{pd1}	$V_{CC} = 5V, C_L = 50pF$			90						ns
		t_{pd0}	$V_{CC} = 5V, C_L = 50pF$			90						ns
2	Propagation Delay Time	t_{pd1}	$V_{CC} = 10V, C_L = 50pF$			60						ns
		t_{pd0}	$V_{CC} = 10V, C_L = 50pF$			60						ns

Note 1: Parameter tested go no go only, cannot be data logged

Note 2: Guaranteed parameter, no testing is available.

Note 3: Guaranteed parameter, may be tested only on a special order basis

Device: MM54C00 **Function:** CMOS Quad 2-Input NAND Gate

3.1.3 Country of Manufacture

All 883S/RETS™ microcircuits provided under this specification shall be manufactured, assembled and tested within the U.S. and its territories.

3.1.4 Line Certification

All 883S/RETS™ microcircuits provided under this specification shall be fabricated and assembled in the United States on lines which have been certified for the fabrication and assembly of JAN microcircuits in accordance with the requirements of MIL-STD-976 and paragraph 3.4.1.2 of MIL-M-38510. (Note: This is not to be interpreted as implying in any way that parts supplied to this specification are JAN qualified devices or are equivalent to JAN qualified devices.)

3.2 Product Assurance Requirements

883S/RETS™ microcircuits shall be those which have been subjected to, and passed all applicable requirements, tests, and inspections detailed herein, including wafer lot acceptance screening, qualification, and quality conformance inspection requirements. Where shown, method references are per MIL-STD-883.

3.2.1 Qualification

883S/RETS™ microcircuits furnished under this specification shall be products which have been produced and tested and have passed the qualification tests specified herein. The required qualification tests shall be Group A, Group B, and Group D testing as specified in Tables I, II, and III of this specification.

3.2.2 Screening

All 883S/RETS™ microcircuits to be delivered in accordance with this specification shall have been subjected to, and passed, all the screening tests detailed in method 5004 of MIL-STD-883 for Class S devices (See Figure 2). Sampling inspections shall not be an acceptable substitute for any specified screening test.

3.2.3 Quality Conformance Inspection

Microcircuits shall not be accepted or approved for delivery until the inspection lot has passed quality conformance inspection (See Section 5.1).

3.2.4 Wafer Lot Acceptance

883S/RETS™ microcircuits furnished under this specification shall be products from wafer lots that are subjected to and successfully meet the wafer lot acceptance inspections and tests specified in Table IV.

3.2.5 Traceability

For 883S/RETS™ microcircuits, each delivered microcircuit shall be traceable to the inspection and wafer lots.

3.2.6 In Process Verification and Die Attach Lead Bonding

Die attach and bonding operations shall be monitored in accordance with paragraph 4.1.1.2 of MIL-M-38510. Samples will be taken at the beginning of the shift and every two hours thereafter.

3.3 Design Documentation

National Semiconductor shall retain on file the design and construction information required by paragraph 3.5.4 of MIL-M-38510.

3.4 Internal Conductors

Internal thin film conductors on silicon die (metallization stripes, contact areas, bonding interfaces, etc.) shall meet the requirements of paragraph 3.5.4 of MIL-M-38510.

3.5 Lead Material and Finish

Lead material and finish shall be as defined in MIL-M-38510, paragraph 3.5.6.

3.6 Glassivation

All 883S/RETS™ microcircuits shall be glassivated. The minimum glassivation thickness shall be 6,000 Å for SiO_2 or 2,000 Å for Si_3N_4. The glassivation/nitridation shall cover all electrical conductors except the bonding pads.

3.7 Die Thickness

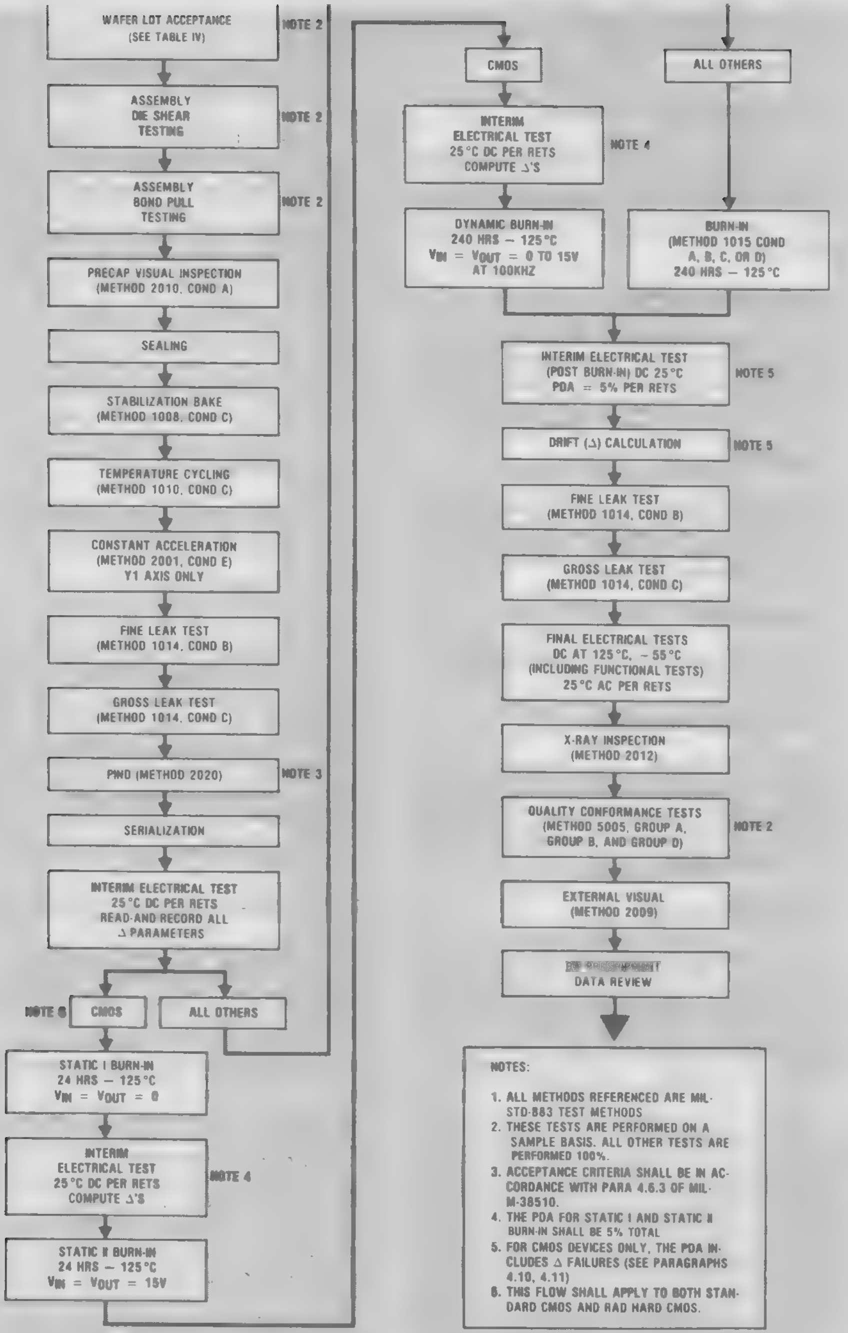
Unless otherwise specified, the minimum die thickness for all microcircuits shall be 0.006 inch (0.15mm).

3.8 Marking

3.8.1 Marking on Each Device

The following marking shall be placed on each integrated circuit:

a) Index point (see 3.8.4)
b) Part number (see 3.8.5)
c) Product assurance level (see 3.8.6)
d) Inspection lot identification code (see 3.8.8)



NOTES:

1. ALL METHODS REFERENCED ARE MIL-STD-883 TEST METHODS
2. THESE TESTS ARE PERFORMED ON A SAMPLE BASIS. ALL OTHER TESTS ARE PERFORMED 100%.
3. ACCEPTANCE CRITERIA SHALL BE IN ACCORDANCE WITH PARA 4.6.3 OF MIL-M-38510.
4. THE PDA FOR STATIC I AND STATIC II BURN-IN SHALL BE 5% TOTAL
5. FOR CMOS DEVICES ONLY, THE PDA INCLUDES Δ FAILURES (SEE PARAGRAPHS 4.10, 4.11)
6. THIS FLOW SHALL APPLY TO BOTH STANDARD CMOS AND RAD HARD CMOS.

Figure 2
883S/RETS™ PRODUCT SCREENING FLOW
(PER MIL-STD-883, METHOD 5004 AND MIL-M-38510)

e) National Semiconductor Identification (see 3.8.9)
f) Country of Origin (see 3.8.10)
g) Serial number (see 3.8.11)
h) SEM acceptance lot number (3.8.12)

3.8.2 Marking on Initial Container

All of the marking specified in 3.8.1, except the index point, shall appear on the initial protection or wrapping for delivery. The serial number range shall be shown rather than individual serial numbers.

3.8.3 Marking Permanence

Marking shall be permanent in nature and remain legible after testing. Damage to marking caused by mechanical fixturing in Group B and D tests shall not be cause for lot rejection.

3.8.4 Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

3.8.5 Part Number

The part number shall be the National Semiconductor part number.

3.8.6 Product Assurance Level

883S/RETS™ microcircuits shall be marked with a code indicating the product assurance level to which they have been tested and found to conform. The code shall consist of /883 followed by the letter S.

3.8.7 Formation of Lots

883S/RETS™ microcircuits shall be assembled into inspection lots and sublots as required to meet the product assurance inspection and test requirements of this specification. An inspection lot and sublot shall be as defined in MIL-M-38510, paragraphs 3.1.3b and 3.1.3d.

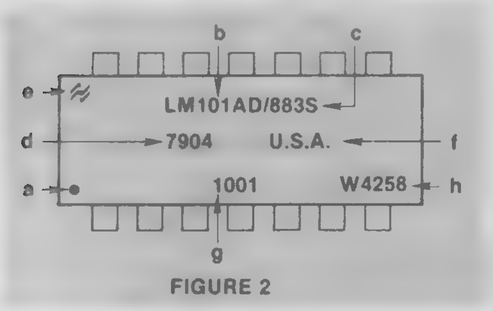


FIGURE 2

3.8.8 Inspection Lot Identification Code

Integrated circuits shall be marked by a 4-digit date code indicating the date the lot was submitted for inspection. The first 2 numbers in the code shall be the last 2 digits of the number of the year. The third and fourth numbers shall be 2 digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. When more than one wafer lot is used to assemble an inspection lot, an alpha character will be suffixed to the date code to differentiate between wafer lots and to maintain wafer lot traceability (see paragraph 3.2.5).

3.8.9 National Semiconductor Identification

Integrated circuits shall be marked with the National Semiconductor logo (NS or ≈).

3.8.10 Country of Origin

The letters "U.S.A." shall be marked below or adjacent to the other specified markings.

3.8.11 Serialization

Prior to the first recorded electrical measurement in screening each 883S/RETS™ microcircuit shall be marked with a unique serial number assigned consecutively within the inspection lot. This serial number allows traceability of test results to the individual microcircuit within that inspection lot. Inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer lot from which the devices originated.

3.8.12 SEM Acceptance Lot Number

Each 883S/RETS™ microcircuit shall be marked with an identifying number providing traceability to SEM acceptance and wafer lot acceptance data by metallization run number.

3.8.13 Marking Location and Sequence

Unless otherwise specified, the part number, inspection lot identification code, and serialization (where applicable), shall be located on the top surface of flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO-99 and similar configurations). The index point shall be marked as specified in appendix C of MIL-M-38510. The balance of the markings may be placed in any suitable location so as to perform their required functions and not interfere with the other markings. Where package size prohibits marking of all information shown in 3.8.1, the order of priority for inclusion shall be a, b, g, c, e, d, f, h.

4.0 Conditions and Methods of Test

Conditions and methods of test shall be in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and test methods for this program. The purpose of these tests is to assure the quality and reliability of the product to a level commensurate with the product's intended application.

4.1 Internal Visual Inspection (Precap)

Internal visual inspection shall be performed per MIL-STD-883, Method 2010 Condition A.

4.2 Stabilization Bake

Stabilization bake shall be performed per MIL-STD-883, Method 1008, Condition C. The devices shall be stored for 24 hours minimum at 150°C minimum.

4.3 Temperature Cycling

Temperature cycling shall be performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from −65°C to +150°C.

4.4 Constant Acceleration

Constant acceleration shall be performed per MIL-STD-883, Method 2001, Condition E, at 30,000 G's, in Y1 axis only.

4.5 Hermeticity

Hermeticity test shall be performed per the following to determine the seal integrity of the package.

Fine Leak Testing

Fine leak testing shall be performed per MIL-STD-883, Method 1014, Condition B. The rejection criterion shall be per MIL-STD-883.

Gross Leak Testing

Gross leak testing shall be performed per MIL-STD-883, Method 1014, Condition C. The rejection criteria shall be per MIL-STD-883.

4.6 Particle Impact Noise Detection (PIND)

Particle impact noise detection testing shall be performed in accordance with MIL-STD-883, Method 2020 and paragraph 4.6.3 of MIL-M-38510

4.7 Serialization

Each unit shall be serialized (see paragraph 3.8.11).

4.8 Interim Electrical Parameters (Pre Burn-In)

Interim electrical parameters shall be the 25°C DC parameters, specified in the detail specification (RETS). All parameters for which drift limits (Δ's) are specified on the RETS shall be read-and-recorded. (Note: Δ parameters are specified for all device types.)

4.9 Burn-in

Burn-in shall be performed per MIL-STD-883, Method 1015, Conditions A, B, C or D, at the supplier's discretion. (Burn-in condition varies with product type.) For CMOS devices, the burn-in sequence shall include Static I, Static II, and Dynamic Burn-in (as shown in figure 1).

The ambient temperature shall be 125°C, and the duration shall be 240 hours minimum. For CMOS devices, the Static I and Static II burn-in shall each be 24 hours in duration.

4.10 Interim Electrical Parameters (Post Burn-In)

The measurements defined in paragraph 4.8 shall be repeated. The PDA shall be 5%. For CMOS, the PDA shall be 5% for the Static I and Static II burn-ins combined and 5% for the Dynamic Burn-in. Drift limits (see 4.11) will be included in the PDA only for CMOS.

4.11 Delta Calculation

Deltas shall be computed for all parameters for which drift limits are established by the RETS. All units failing the drift limits shall be removed from the lot. Drift limit failures shall be included in the PDA (see 4.10) only for CMOS devices.

4.12 Hermeticity Testing

Fine and gross leak testing shall be performed as defined in paragraph 4.5.

4.13 Final Electrical Parameters

Final electrical parameters shall be as defined in the applicable detail specification. DC testing shall be performed at 25°C, −55°C, and +125°C (except that any 25°C tests performed in 4.8 need not be repeated), and AC tests shall be performed at 25°C.

4.14 Radiographic Inspection

Radiographic inspection shall be performed in accordance with MIL-STD-883. Method 2012.

4.15 Quality Conformance Testing

Samples shall be randomly selected from the lot, and quality conformance inspection shall be performed in accordance with 5.0.

4.16 External Visual Inspection

All 883S/RETS™ microcircuits shall receive external visual inspetion per MIL-STD-883, Method 2009.

5.0 Quality Assurance Provisions

5.1 Quality Conformance Inspection

Quality conformance inspection shall be in accordance with Tables I, II, and III. Inspection lot sampling shall be in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for the Class S product assurance level shall be rejected.

5.1.1 Group A Inspection

Group A inspection shall consist of the electrical parameters in the RETS. If an inspection lot is made up of a collection of sublots, each sublot shall be subjected to Group A (See Table I).

5.1.2 Group B Inspection

Group B inspection consists of those tests specified in Table II. Group B tests will be performed on every inspection lot.

5.1.3 Group D Inspection

Group D testing consists of those package oriented tests specified in Table III. Group D testing will be performed within National's 883B/RETS™ program once every 6 months per package type.

6.0 Data

6.1 Data Shipped with Parts

One copy of the following data shall be provided with each shipment of 883S/RETS™ microcircuits:

a) Attributes and variables data for 100% screening.
b) A reject list showing, by serial number, all rejected devices and cause for rejection.
c) X-ray report.
d) Certificate of Conformance for water lot acceptance.

6.2 Data Retained on File

The following data will be maintained on file at National Semiconductor for 3 years (but may be provided with shipment upon special order).

a) X-ray film (radiographs).
b) SEM photos
c) Attributes and variables data for Quality Conformance testing.

7.0 Hybrid Devices

Hybrid devices are not available through the 883S/RETS™ product program, but modified Class S flows are available on a special order basis.

TABLE 1. GROUP A ELECTRICAL TEST
(PER METHOD 5005, TABLE I)

SUBGROUPS	CLASS S LTPD
Subgroup 1 Static tests at 25°C	5
Subgroup 2 Static tests at 125°C	7
Subgroup 3 Static tests at −55°C	7
Subgroup 4 (note 1) Dynamic tests at 25°C	5
Subgroup 5 (note 1) Dynamic tests at 125°C	7
Subgroup 6 (note 1) Dynamic tests at −55°C	7
Subgroup 7 (note 1) Functional tests at 25°C	5
Subgroup 8 (note 1) Functional tests at 125°C and −55°C	10
Subgroup 9 Switching tests at 25°C	7
Subgroup 10 Switching tests at 125°C	10
Subgroup 11 Switching tests at −55°C	10

NOTES:

1. NATIONAL WILL NORMALLY PERFORM THESE SUBGROUPS AT THE SAME TIME AS SUBGROUPS 1, 2, AND 3 RESPECTIVELY.
2. MAXIMUM ACCEPT NUMBER FOR EACH SUBGROUP SHALL BE 1.

TEST	MIL-STD-883 METHOD	CONDITIONS	CLASS S LTPD OR SAMPLE SIZE
Subgroup 1			
Physical dimensions	2016		2 devices (no failures)
Internal Water Vapor Content	1018	(note 5)	3 devices (no failures)
Subgroup 2 (note 1)			
a) Resistance to solvents	2015		3 devices (No failures)
b) Visual and mechanical	2013 and 2014	Failure criteria from design & construction requirements of applicable procurement document	2 devices (no failures)
c) Bond strength	2011	Test condition C or D	2 devices all wires (no failures)
d) Die shear	2019	Per table I of Method 2019 for applicable die size	3 devices (no failures)
Subgroup 3			LTPD = 15
Solderability (note 2)	2003	Soldering temperature of 260 ± 10°C	15 leads (3 units min, no failures)
Subgroup 4			
a) Lead integrity	2004	Test condition B2	2 devices (no failures)
b) Seal (fine and gross)	1014	Cond B or C, As applicable	
Subgroup 5 (note 3)			LTPD = 5
a) Electrical parameters		Per applicable RETS (25°, DC)	
b) Operating life	1005	Test condition A, B, C or D	77 devices (one failure)
c) Electrical parameters		Per applicable RETS (25°C, DC)	
Subgroup 6 (note 3)			
a) Electrical parameters		Per applicable RETS (25°C, DC)	12 devices (no failures)
b) Temperature cycling	1010	Test condition C, 100 cycles min.	
c) Constant acceleration	2001	Test condition E, Y1 axis only	
d) Seal (fine and gross)	1014	Cond B or C, As applicable	
e) Electrical parameters		Per applicable RETS (25°C, DC)	

NOTES:

1. Samples subjected to this subgroup shall have been through the entire sequence of subgroup 6 testing.
2. All samples shall have seen 240 hours at 125°C (or equivalent)
3. Electrical measurements shall be recorded for those parameters for which deltas (Δ) are specified, and Δ's will be computed.
4. Resubmission of failed lots shall be in accordance with paragraph 4.3.3.1 of MIL-M-38510.
5. Required only for packages containing a dessicant.

TABLE III. GROUP D INSPECTION
(PER METHOD 5005, TABLE IV)

TEST	MIL-STD-883 METHOD	CONDITIONS	CLASS S LTPD AND B
Subgroup 1			LTPD = 15
Physical dimensions	2016		15 devices (no failures)
Internal water vapor content	1018		3 devices (no failures)
Subgroup 2 (note 1)			LTPD = 15
Lead integrity	2004	Test conditions B2 (lead fatigue)	15 devices (no failures)
Seal (fine and gross)	1014	Cond B or C, As applicable	
Subgroup 3			LTPD = 5
Thermal shock	1011	Test condition B — 15 cycles	15 devices (no failures)
Temperature cycling	1010	Test condition C — 100 cycles	
Moisture resistance	1004		
Seal (fine and gross)	1014	Cond B or C, As applicable	
Visual examination	1004		
End point electrical parameters		Per applicable RETS (DC, 25°C)	
Subgroup 4			LTPD = 15
Mechanical shock	2002	Test condition B	15 devices (no failures)
Vibration variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y1 axis only	
Seal	1014	Cond B or C, As applicable	
Fine			
Gross			
Visual examination	1010		
End point electrical parameters		Per applicable RETS (DC, 25°C)	
Subgroup 5 (note 1)			LTPD = 15
Salt atmosphere	1009	Test condition A	15 devices (no failures)
Seal (fine and gross)	1014	Cond B or C, As applicable	
Visual examination	1009	Paragraph 3.3.1 of Method 1009	

Note 1: Electrical rejects from the same inspection lot may be used.
Note 2: Resubmission of failed lots shall be in accordance with paragraph 4 3 3.2 of MIL-M-38510

TABLE IV WAFER LOT ACCEPTANCE

TEST	LIMIT	SAMPLING PLAN	NOTES
1. Wafer Thickness	Design Nominal ±2 mil (±.002 inches) 6 mil (.006 inches)	Two Wafers Per Wafer Lot At Incoming Inspection	1
2. Metallization Thickness	Design Nominal ±2KÅ 8KÅ Minimum For Single Level Metal and Top Layer of Multi-Level Metal. 6KÅ Minimum for Lower Level Metal Barrier Metal: ±20% of Design Nominal	One Wafer Per Metallization Run	
3. Thermal Stability	Bipolar: ΔV_{FB} or $\Delta V_T \leq 1.0V$	Once Per Month and After Each Tube Change	2, 3
	MOS: ΔV_{FB} or $\Delta V_T \leq .5V$	Once Per Week and After Each Tube Change	2,5
4. SEM	Per MIL-STD-883, Method 2018	Two Wafers Per Metallization Run	
5. Glassivation Thickness	±20% From Design Nominal 6KÅ Minimum	Two Wafers Or Test Chips Per Glassivated Lot	
6. Gold Backing Thickness	4.5KÅ Minimum 15KÅ Maximum	One Wafer Per Lot	4

NOTES:

1. This test is not required when the finished wafer design thickness is greater than 10 mils (.010 inches).
2. Required only for bipolar digital operating at 10V or more, all linear, and all MOS.
3. For a wafer run to be acceptable, both the readings taken before and after the run must be verified
4. Required only for gold-backed wafers.
5. For Rad Hard CMOS devices, this test will be performed on every wafer lot.

National and Mil-M-38510

Introduction

A major thrust exists among integrated circuit users, suppliers, and the U.S. Government to avoid proliferation of military procurement specifications by turning instead to standardized reliability processed products. National Semiconductor endorses and supports such trends.

One major program to which National is heavily committed is the JAN 38510 IC program. This is a standardization program administered by the U.S. Defense Department which allows a user to purchase a broad line of standard products from a variety of qualified suppliers.

There is only one 38510 program. National is committed to supplying only QPL devices, and discourages any "pseudo-38510" alternates.

The purpose of this brochure is to explain and clarify the program while highlighting its advantages and benefits to users.

There are three quality levels currently available — S, B, and C. S is typically specified for space flight application while B is used for aircraft and ground systems. C is sometimes specified for ground systems but, since it requires virtually all of the screening that B requires (except burn-in), B is most universally specified. This brochure concentrates on the requirement for *B* level devices

Mil-M-38510

The Defense Electronic Supply Center (DESC) administers the integrated circuit standardization program known as Mil-M-38510, sometimes referred to as the JAN IC Program. The specification set used to define the program consists of four primary documents: general specification Mil-M-38510, which is a comprehensive definition of the detail processing and testing, referenced to Mil-STD-883 test methods to which IC devices produced under the program will be subjected, detail specifications, often referred to as "slash sheets," each of which explicitly defines the performance parameters of a unique generic device or a family of devices; Mil-STD-883, which defines specific screening procedures, and Mil-STD-976, which defines line certification requirements.

When a user orders a Mil-M-38510 device, he is guaranteed that he will get a device fully conformant with the detailed requirements and which has been subjected to the general testing and processing requirements. DESC requires semiconductor suppliers to become formally qualified under the 38510 program and listed on the current Qualified Products List (QPL) before they are allowed to legally ship JAN devices.

Advantages to the User

The JAN 38510 program has numerous advantages for the integrated circuit user.

- A single explicit specification eliminates guesswork concerning what electrical characteristics or processing flow the devices receive. (See Table 1 for details of the 38510 IC processing flow.)
- A rigorous schedule of quality conformance testing is a mandatory part of the Mil-M-38510 program, assuring the user that long-term reliability has been statistically sampled and documented.
- Since the electrical characteristics of the devices are at least as tight as the "standard industry data sheet" parameters, device performance will meet the vast majority of system design requirements. Additionally, there are more min/max values in lieu of data sheet typicals, thus aiding in circuit design and worst case design analysis.
- The user is spared the expense of researching and preparing his own procurement document.
- The user is spared the expense of qualification testing. The QPL tells him which suppliers have qualified the devices he requires.
- The QPL gives the user a choice of qualified suppliers for devices that are fully interchangeable. In addition, the availability of several sources guarantees competitive pricing which will typically be lower than the pricing for devices to a user's own spec.
- Since 38510 is a standard program, procurement lead times will be shorter. With the vast proliferation of programs using JAN devices, distributors and manufacturers are increasing their inventories of JAN devices. National in particular is committed to maintaining finished goods and work-in-process inventories to support user needs.
- Spare parts will be readily available.
- Device markings are consistent from one manufacturer to another.
- The program is extremely cost effective. A user can purchase a few devices for engineering evaluation and prototyping and know that they will be identical to the devices he will get during production. When the cost factors associated with spec writing, supplier qualification, maintaining voluminous parts control documentation, and the more intangible benefits of device availability are totaled, use of JAN ICs is overwhelmingly the most cost effective approach.

Advantages to the Supplier

What motivates a supplier like National to be so heavily committed to the 38510 program? National has the *broadest* range of reliability processed products available in the semiconductor industry. A program such as Mil-M-38510 helps to standardize the processing required and minimize the number of individual user specifications. This allows National to concentrate more resources on this program, thereby improving product quality and availability.

Q. WHAT DOES A MANUFACTURER HAVE TO DO TO GET PARTS LISTED ON THE QPL?

A. There are two things which a manufacturer is required to do. First, he must get his facilities (including wafer fab, assembly, and rel processing areas) certified by DESC. This requires that each fab area used for QPL devices must be approved. Second, for each specific device and package combination listed on the QPL, the manufacturer must perform extensive qualification testing and provide detailed device information to DESC. This data is typically supplied in two phases. In the first phase, the manufacturer must supply detailed information concerning the device construction and electrical characteristics. Once this data bas been verified by DESC to confirm that the manufacturer's device meets the 38510 requirements, the manufacturer is listed on Part II of the QPL. At this point the manufacturer is legally able to supply full JAN qualified devices meeting ALL of the 38510 requirements. The manufacturer then must perform the full qualification testing of method 5005 of 883 as specified in paragraph 4.4 of 38510. Once this data has been reviewed and accepted by DESC, the manufacturer is listed on Part I of the QPL.

Q. IS THERE ANY DIFFERENCE IN THE DEVICES A USER GETS FROM A MANUFACTURER WHO IS LISTED ON PART II OF THE QPL COMPARED TO THOSE FROM A MANUFACTURER ON PART I?

A. There is absolutely *no difference*. A supplier must meet all of the device screening and quality conformance requirements no matter what his QPL status.

Q. HOW DOES A USER KNOW WHAT DEVICES ARE COVERED BY THE SLASH SHEET SPECIFICATION?

A. Supplement 1 to Mil-M-38510 contains a listing of the slash sheet specifications and a cross reference to the generic part types This is updated as new slash sheets are released.

Q. HOW DOES A USER GET COPIES OF THE QPL. SUPPLEMENT 1 OF 38510, MIL-M-38510 ITSELF, AND MIL-STD-883?

A. Copies of these and other related items may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(215) 697-2179

Q. WHAT HAPPENS WHEN A USER CANNOT OBTAIN HIS COMPLETE PARTS NEEDS FROM QPL LISTED DEVICES?

A. The ultimate aim of a standardization program must be to furnish *all* parts. Requests for addition of a part to 38510 should be made to DESC Directorate of Engineering, Dayton, Ohio 45444, indicating a need for slash sheets and/or suppliers to be qualified for the additional devices. National has a form (available through local sales offices) which may be used for this purpose. This form is shown in figure 1. In addition, if only some parts are available, a user can still see significant savings on those that are available.

Q. HOW IS A *JAN QPL* DEVICE MARKED?

A. Tables II and III explain the details of the marking for JAN QPL ICs.

A. *Absolutely not.* There is only one QPL product — it is a JM38510 marked device. "JAN Equivalent" is expressly forbidden by paragraphs 3.1 and 3.6.7 of Mil-M-38510. National does not support these "equivalent" products.

Q. HOW LONG CAN A SUPPLIER REMAIN ON PART II OF THE QPL?

A. A manufacturer can remain on Part II for two years or until 30 days after another supplier becomes qualified for the same device package, screening level, and lead finish combination on Part I of the QPL.

Q. WHEN ANOTHER SUPPLIER OBTAINS PART I QUALIFICATION, ARE THE OTHER QUALIFIED SUPPLIERS REMOVED FROM PART II IMMEDIATELY?

A. No. The supplier is given 30 days before being removed from Part II. During that time a supplier may legally accept orders for those devices. After the end of the 30-day period, he may no longer accept orders but may complete and ship those orders received prior to that time, no matter how long it takes him to complete them.

Q. IS A SUPPLIER EVER REMOVED FROM PART I QUALIFICATION?

A. Generally not. As long as a supplier continues to manufacture the device, maintains appropriate facility approvals, and submits all required reports and information to DESC within stipulated time limits he will retain QPL I listing. Violation of these requirements can be cause for removal from QPL.

Q. CAN AN AUTHORIZED DISTRIBUTOR SHIP *JAN* DEVICES FROM HIS SHELVES IF THE MANUFACTURER HAS LOST HIS *QPL* LISTING FOR THOSE DEVICES?

A. Yes. As long as those devices were ordered by the authorized distributor while the manufacturer had QPL listing for those devices, the distributor may subsequently ship those devices from his shelves.

Q. CAN A MANUFACTURER LEGALLY SHIP JAN QPL MATERIAL HE ASSEMBLED AND TESTED BEFORE HE RECEIVED A QPL LISTING?

A. Yes. The manufacturer must assemble and screen parts to prove his ability to comply with the specifications before he can be placed on QPL. As a result, his first lot of material, which is fully conformant to QPL product requirements, will have a date code that is earlier than the date he is placed on the QPL.

Q. WHAT IS THE RELATIONSHIP BETWEEN MIL-M-38510 AND MIL-STD-883?

A. Mil-M-38510 defines complete program requirements and the detail device electrical performance parameters. The device processing requirements are specified using the test methods defined in Mil-STD-883.

Q. SUPPOSE DEVICES ARE KEPT ON A MANUFACTURER'S OR DISTRIBUTOR'S SHELVES FOR A PERIOD OF TIME; MUST THEY EVER BE RETESTED TO VALIDATE THAT THEY MEET SLASH SHEET CHARACTERISTICS?

A. Yes. Devices held by a manufacturer or his authorized distributor for more than 24 months must be retested by the manufacturer in accordance with Group A sampling requirements prior to shipment to a customer.

Q. WHY SHOULD A USER SPECIFY "X" IN THE LEAD FINISH DESIGNATOR FOR A PART TYPE?

A. A manufacturer who receives an order for a specific lead finish for which he is qualified but has no inventory at the time of order may not be able to fill the order in a timely manner, even though he might have substantial inventory of another lead finish. Unless a user has a specific reason for wanting a particular lead finish, he should allow his suppliers the flexibility of shipping whatever finish is most readily available.

Q. WHAT DATA IS A MANUFACTURER REQUIRED TO SHIP WITH A JAN PART?

A. A certificate of conformance is all that is required. However, he must retain all data for three years.

Q. CAN A DEVICE FOR WHICH THERE IS NO SLASH SHEET BE PROCESSED TO 38510?

A. Since Mil-M-38510 invokes a combination of the processing requirements of Mil-STD-883 and the detail device performance parameters contained in each individual slash sheet, the answer is obviously no. However, National's 883/RETS program provides parts which meet all of the screening requirements of the MIL-STD-883 specification.

Q. WHAT DOES A QPL LISTING LOOK LIKE AND HOW DO YOU READ IT?

A. Sample QPL listings are shown below:

Government Designation					
Device Type	**Device Class**	**Case Outline**	**Lead Mat & Finish**	**Test Report Number**	**Manufacturer's Name (Address on Last Page)**
JM38510/001					
05	B	A---	A or C	38510-261-72	National Semiconductor
08	C	C---	B only		Corporation
JM38510/057					
05	B	E	B	38510-93-77	National Semiconductor
	C	F	C		Corporation

The first listing covers the following devices.

JM38510/00105	BAA	JM38510/00108	BAA
	BAC		BAC
	BCB		BCB
	CAA		CAA
	CAC		CAC
	CCB		CCB

The second listing covers the following devices

JM38510/05705	BEB	JM38510/05705	CEB
	BEC		CEC
	BFB		CFB
	BFC		CFC

Q. WHAT QUALITY CONFORMANCE TESTS ARE CONDUCTED? ARE ALL DEVICES IN A GENERIC FAMILY EVENTUALLY SUBJECTED TO QUALITY CONFORMANCE TESTING?

A. For B level devices quality conformance tests must be conducted as follows:

Group A — Each inspection lot.

Group B — Each inspection lot for each package type and lead finish on each detail specification.

Group C — Periodically at 90-day intervals on one device type or one inspection lot from each microcircuit group in which a manufacturer has qualified device types.

Group D — Periodically at a six-month interval for each package type for which a manufacturer holds qualifications.

Different devices within a generic family are chosen for successive quality conformance tests until all of the devices have been subjected to testing. The sequence is then repeated. The manufacturer must submit attributes data to DESC for all quality conformance tests performed. Tables IV, V, VI, and VII contain the details of the Group A, B, C, and D tests respectively.

Q. HOW IS AN INSPECTION LOT DEFINED?

A. For Class B devices, each inspection lot shall consist of microcircuits of a single type, in a single package type and lead finish, or may consist of inspection sublots of several different types, in a single package type and lead finish, defined by a single detail specification. Each inspection lot shall be manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and case with the same material requirements, and sealed within the same period not exceeding six weeks.

Table I

JAN Device Processing Flow — Level B
(per Method 5004 of MIL-STD-883)

Screen	Method	Requirement
Internal Visual (Precap)	2010B	100%
Stabilization Bake	1008, Test Condition C 24 hrs min	100%
Temperature Cycling	1010, Test Condition C 10 cycles min	100%
Constant Acceleration	2001, Test Condition E Y_1 axis, 30,000 Gs	100%
Hermeticity a Fine b Gross	1014	100%
Interim Electrical Parameters	per Applicable Slash Sheet	100%
Burn in Test	1015, 160 hrs at 125°C min	100%
Final Electrical Test a Static Tests	per Applicable Slash Sheet PDA on static tests at 25°C is 10%	100%
1 25°C 2 Max & Min Rated Operating Temp		
b Dynamic Tests 25°C c Functional Test 25°C		
Qualification or Quality Conformance Inspection	5005	Sample per Method 5005
External Visual	2009	100%

Table II
The Mil-M-38510 Part Number

JM38510/XXXXXYYY

the Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable.
the Device Package (see Table III)
the Screening Level S, B, or C
the Device Number on the Slash Sheet
the Slash Sheet Number
Mil-M-38510
The JAN prefix (which may be applied only to a fully conformant device per paragraphs 3.6.2.1 and 3.6.7 of Mil-M-38510)

Example: JM38510/10107BGC is the Mil-M-38510 part number for a QPL LM118 to B screening level in an 8-pin TO-99 can with gold plate lead finish.

Table IV
Group A Electrical Test

Subgroups	Class B LTPD
Subgroup 1 Static tests at 25°C	5
Subgroup 2 Static tests at maximum rated operating temperature	7
Subgroup 3 Static tests at minimum rated operating temperature	7
Subgroup 4 Dynamic tests at 25°C	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	7
Subgroup 6 Dynamic tests at minimum rated operating temperature	7
Subgroup 7 Functional tests at 25°C	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperature	10
Subgroup 9 Switching tests at 25°C	7
Subgroup 10 Switching tests at maximum rated operating temperature	10
Subgroup 11 Switching tests at minimum rated operating temperature	10

Table III
JAN Package Codes

38510 Package Designation	Microcircuit Industry Description	National Equivalent Package
A	14-pin 1/4'' x 1/4'' (metal) flat pack	F
B	14-pin 3/16'' x 1/4'' flat pack	None
C	14-pin 1/4'' x 3/4'' dual-in-line	J/D
D	14-pin 1/4'' x 3/8'' (ceramic) flat pack	W
E	16-pin 1/4'' x 7/8'' dual-in-line	J/D
F	16-pin 1/4'' x 3/8'' (metal or ceramic) flat pack	F/W
G	8-pin TO-99 can or header	H
H	10-pin 1/4'' x 1/4'' (metal) flat pack	F
I	10-pin TO-100 can or header	H
J	24-pin 1/2'' x 1 1/4'' dual in line	J/D
K	24-pin 3/8'' x 5/8'' flat pack	None
M	12-pin TO-101 can or header	G
Q	40-pin 0.6'' x 2.0'' dual-in-line	J/D
V	18-pin 0.3'' x 0.9'' dual-in-line	J/D
W	22-pin 0.4'' x 1.1'' dual-in-line	J/D

Table V
Group B Inspection

Test	Method	Conditions	Class B
Subgroup 1			
a. Physical dimension	2016		2 devices (no failures)
b. Internal water vapor content	1018	1000 ppm max water content at 100°C	3 devices (no failures)
Subgroup 2			
a. Resistance to solvents	2015		3 devices (no failures)
b. Internal visual and mechanical	2014	Failure criteria from design & construction requirements applicable procurement document	1 device (no failures)
c. Bond strength	2011	Test condition C or D	15 bonds (10 units min no failures)
Subgroup 3			
Solderability	2003	Soldering temperature of 260°C ± 10°C	15 leads (3 units min no failures)

Table VI
Group C Inspection

Test	Method	Conditions	Class B LTPD
Subgroup 1			
Operating Life Test	1005	Test conditions to be specified (1000 hours at 125°C)	5
Subgroup 2			
Temperature Cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E, Y_1 axis	
Seal Fine Gross	1014	As applicable	
Visual examination	1010		
End point electrical parameters		As specified in applicable device specification	

Table VII
Group D Inspection

Test	Method	Conditions	Class B LTPD
Subgroup 1			
Physical dimensions	2016		15
Internal water vapor content	1018	5000 ppm max water content at 100°C	3 devices (no failures)
Subgroup 2			
Lead integrity	2004	Test condition B2 (lead fatigue)	15
Seal Fine Gross	1014	As applicable	
Subgroup 3			
Thermal shock	1011	Test condition B — 15 cycles minimum	15
Temperature cycling	1010	Test condition C — 100 cycles minimum	
Moisture resistance	1004		
Seal Fine Gross	1014	As applicable	
Visual examination	1004		
End point electrical parameters		As specified in applicable device specification	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration, variable freq	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y_1 axis	
Seal Fine Gross	1014	As applicable	
Visual examination	1010		
End point electrical parameters		As specified in device specification	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Seal Fine Gross	1014	As applicable	
Visual examination	1009	Paragraph 3.3.1 of Method 1009	

TO:
Defense Electronics Supply Center
Dayton, Ohio 45444
Attention: Director Engineering Standardization, DESC E

FROM: ______________________________
Name ______________________________
Company ______________________________
Address ______________________________

Currently, I am defining requirements and preparing parts lists for the ______________________________ Program. For this program, I am attempting to utilize standard parts from the 38510 QPL list. Although I have been able to utilize some QPL listed parts, there are a number of devices for which slash sheets apparently have not yet been generated and/or for which there are no qualified sources. I have included those devices in the following list. I have also indicated the time frame in which I will need production quantities as well as the quality level.

Generic Device Type	Production Quantity	Production Need Date	Quality Level (S or B)	for DESC use only DESC Status*

Your help in setting appropriate priorities for generating these slash sheets and/or encouraging suppliers to become qualified will be beneficial to this program and is appreciated.

A space is provided to indicate the current status of each device. Please return the second page of this form to me.

Sincerely,

*DESC Status Codes
1—Spec in negotiation
2—Currently qualifying supplier
3—New input — will advise
4—No current plans for slash sheet

compliments of National Semiconductor Corporation

RADIATION HARDENED TECHNOLOGIES FROM NATIONAL SEMICONDUCTOR

For many years, military, aerospace and satellite programs have depended on bipolar transistor and integrated circuit technology in the fabrication of airborne systems. Development of bipolar technology is an outgrowth, in part, of avionics and space applications needs. Despite their relatively high immunity or resistance to high levels of both constant and burst radiation in the form of gamma rays, x-rays, cosmic rays, and so on, bipolar devices have one drawback: high power consumption, which adds to the power supply requirements and subtracts from the usable payload of spacecraft and missiles. The spacecraft and missile industry has long needed a radiation hardened logic technology with low power consumption. A second problem seen in this area has been the limited radiation tolerance of many linear devices. The purpose of this brochure is to provide some information to the potential user regarding National Semiconductor's solutions to both of these problems.

CMOS Radiation Hardened Products

In recent years, the development of sophisticated space, satellite and military systems and mission requirements has fostered an active search for a radiation hardened logic circuit technology that consumes less power and offers a higher degree of circuit integration on a single silicon chip. Metal oxide semiconductor (MOS) devices, particularly complementary MOS (CMOS), seemed to promise just such an alternative. But standard CMOS devices, even those qualified to MIL-M-38510 (JAN) requirements, proved sensitive to relatively low radiation levels. Until recently, mass producible radiation hardened or resistant CMOS devices have been able to withstand only 10^5 rads (Si)[1], while many space, satellite and missile systems require circuitry resistance levels at least ten times higher, 10^6 rads (Si).

Now, National Semiconductor offers a solution to this problem: a complete line of megarad hardened CMOS logic products utilizing a radiation hardening process that is compatible with volume processing. Megarad hardened products [devices capable of tolerating total dose radiation of 10^6 rads (Si)] are the result of an intensive two-year research and development program which has enabled National Semiconductor to offer radiation hard versions of virtually our entire metal-gate CMOS product line. Devices ranging in complexity from simple gates to large scale integration (LSI) random access memories have now been hardened using the processes we have developed. To achieve this level of radiation resistance in a mass production CMOS process, major modifications were made in the basic commercial process, relating to gate oxidation, substrate and P-tub surface concentrations, and metallization.

Bipolar vs. CMOS

The inherently higher radiation resistance of bipolar over CMOS devices results from a basic difference in their structures. Bipolar devices are vertical structures. The basic elements—emitter, collector, and base—are laid down vertically, layer upon layer, by diffusion. As figure 1 shows, current flows through the bulk silicon, some distance below the silicon-silicon dioxide interface. Thus, there is some inherent protection from the interface effects of ionizing radiation in bipolar devices.

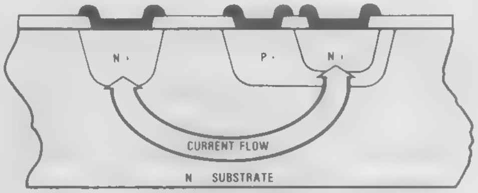


FIGURE 1 BIPOLAR IC TRANSISTOR

CMOS devices are surface effect devices. The equivalent operating elements, gate, source and drain, are at the surface, and the flow of current occurs horizontally across the device, very close to the silicon-silicon dioxide interface. Changes in interface parameters created by the introduction of surface ionic charge during gamma or x-radiation have a first order effect on MOS transistor performance, in contrast to the second order effect they have on bipolar devices. Thus, the basic physics of CMOS transistor structures needs to be addressed to minimize ionizing radiation effects without substantially impacting performance.

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[1] *One rad (Si) is the quantity of any type of ionizing radiation which imparts 100 ergs of energy per gram of silicon.*

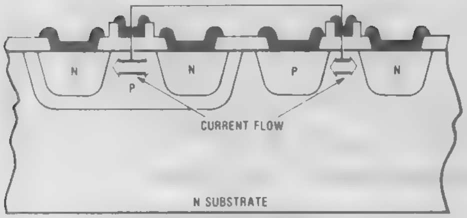

FIGURE 2 CMOS IC TRANSISTORS

CMOS Transistor Structure

Complementary MOS, or CMOS, combines two types of MOS devices, P-channel and N-channel structures, into a single functioning unit. The lower power dissipation and high stability resulting from this complementary combination is particularly attractive in the design of portable battery-powered electronic units, or for applications where a battery provides standby power.

MOS structures, both N- and P-types, perform in two modes; enhancement and depletion. In a P-channel enhancement mode MOS device, for example, the gate controls the current flow between the source and drain. In this device, when a negative voltage is applied to the gate with respect to the source, a field is set up accross the gate dielectric, producing a positively charged conductive path, a channel, between the source and the drain. This is known as an enhancement mode device because zero gate to source voltage turns off the device. In the alternative mode, depletion, current flows despite the gate voltage being zero, because sufficient field is still present within the gate to induce a conductive path between the device source and drain regions. the N-channel MOS transistor is similar to the P-channel alternative, except that positive voltage applied to the gate, with respect to source, induces a negatively charged conductive path between source and drain to turn the device on.

Conventional CMOS logic circuits are produced with only enhancement mode N- and P-channel devices. The process is designed to give turn on (threshold) voltage values for both types of devices which insure proper circuit performance. Figure 3 illustrates the cross section of a CMOS structure connected in a simple inverter configuration. To form the standard metal gate CMOS structure, a lightly doped P-tub is formed by diffusion into an N-type subtrate with the tub becoming the subtrate for the N-Channel transistor. The N+ and P+ impurities are diffused into P-tub and N-substrates to become the N- and P- channel transistors' source and drain regions, respectively. These diffusions also serve as contacting regions to the positively biased N-substrate and the normally grounded P-tub regions (V_{DD} and V_{SS} respectively).

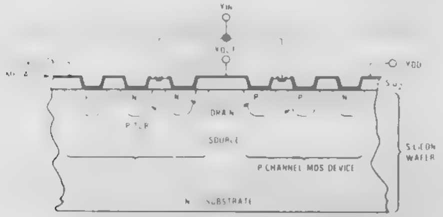

FIGURE 3 CMOS TRANSISTOR STRUCTURE IN SIMPLE INVERTER CONFIGURATION

A gate oxide is grown such that a thin film of dielectric oxide material bridges the source/drain regions over the entire circuit. Finally, contact apertures are etched to the source/drain regions and an aluminum film evaporated and etched to form gate electrodes, contacts to device terminals, and interconnection conductor lines.

Effects of Ionizing Radiation

A CMOS transistor's radiation resistance is primarily determined by formation of the gate structures in both P-channel and N-channel devices. The gate structures are used to turn the MOS devices on or off; that is, to start or stop a flow of current from the source to the drain. Ionizing radiation induces unwanted positive charge into the gate oxide structure, resulting in lowering the threshold voltage of actual circuit devices and parasitic field oxide devices by values of as much as 30V or more. Figure 4 shows the charge buildup mechanisms in an N-channel gate oxide during irradiation under worst case bias. In establishing a radiation hardened CMOS process, it is necessary to incorporate processing steps which minimize these radiation induced shifts in critical locations of the IC structure.

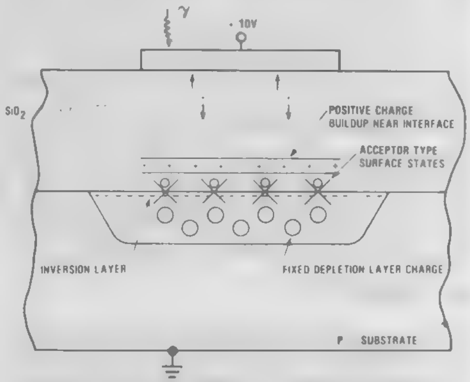
γ
+10V
SiO2
POSITIVE CHARGE BUILDUP NEAR INTERFACE
ACCEPTOR TYPE SURFACE STATES
INVERSION LAYER
FIXED DEPLETION LAYER CHARGE
P SUBSTRATE

FIGURE 4 CHARGE BUILD UP MECHANISMS IN AN N CHANNEL GATE OXIDE DURING IRRADIATION UNDER WORST CASE BIAS

The impact of radiation induced oxide charge on operating CMOS devices is to decrease the N-channel threshold voltage, V_{TN}, and increase the magnitude of the P-channel threshold voltage, V_{TP}. The most serious problem occurs when sufficient reduction in V_{TN} occurs to cause the N-channel device to go from enhancement to depletion mode operation. This results in excessive power supply current drain and loss of circuit functionality. The most severe stress on an N-channel device occurs when its gate is positively biased during irradiation. This causes positive charge in the oxide to be driven closer to the Si-SiO_2 interface where it is more effective in causing the P-type substrate surface to become inverted to N-type.

In normal operation, positive bias does not appear between the gate and substrate of P-channel devices since the substrate is already at the most positive circuit potential, V_{DD}. The most severe effect on P-channel devices during irradiation often occurs with zero gate to substrate bias. This stress creates Si-SiO_2 interface states which are capable of holding a positive charge with negative voltage applied to the gate. This increases the absolute value of V_{TP}, but is a much less deleterious effect to the circuit than the V_{TN} shift.

CMOS Process Modification

Gate Oxidation

To minimize both the radiation induced positive oxide charge and formation of Si-SiO_2 interface states, a dry rather than wet oxidation step is used. The gate oxide is thermally grown in a pure oxygen atmosphere, rather than in a steam atmosphere, as is the case in some metal gate fabrication processes. Moreover, the gate oxide is thermally grown at 1000°C, followed by a nitrogen anneal at 850°C. This cycle has been empirically found to produce oxides having a high degree of resistance to ionizing radiation effects as well as excellent pre-radiation MOS characteristics[2]. The need for thermally growing gate oxides at 1000°C in dry oxygen for optimal radiation hardness is one of the more intriguing aspects of this experimentally deduced cycle.

Metallization

A by-product of the E-beam aluminum evaporation process commonly used in commercial IC fabrication is soft X-radiation. This radiation produces the same type of positive charge in the gate oxide and interface states which a radiation hardened oxide should resist. Although these harmful effects in the gate oxide can be removed by a high temperature anneal cycle, subsequent exposure of the oxide to ionizing radiation results in a drastically less radiation resistant structure. Use of a non-E-beam metallization technique circumvents the problem of high threshold shifts due to irradiation under zero and negative gate bias associated with soft X-ray damage. For this reason, induction heated evaporation of aluminum is used to fabricate radiation hardened CMOS products.

Substrate and P-Tub Surface

The deleterious effect of ionizing radiation on V_{TN} and V_{TP} values in a CMOS device can be minimized through process modification. In anticipation of these threshold voltage shifts, radiation hardened CMOS devices are designed with the initial value of V_{TN} as high as possible and V_{TP} as close to zero as possible without sacrificing pre-radiation circuit performance. Both the substrate resistivity and the P-tub surface concentration have been modified with the initial value of V_{TN} being increased to 1.8 volts from the standard value of 1.3 volts and V_{TP} being changed from the standard −1.7 volts to −1.3 volts.

Performance Characteristics

All of the data given in Figures 5 through 10 was generated from the parts listed in Table A. Figures 5 through 8 illustrate the variation of post radiation V_{TN} and V_{TP} with dose. The distribution of the V_{TN} and V_{TP} data is found to be normal both before and after irradiation. The solid line shows the mean value of V_{TN} (or

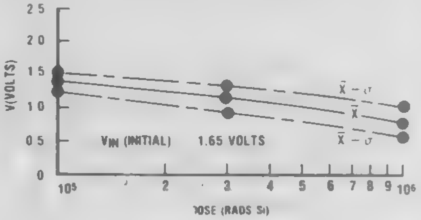

FIGURE 5. V_{TN} VS. DOSE

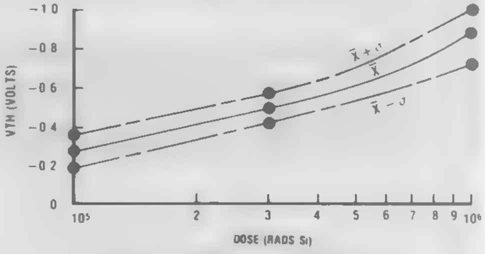

FIGURE 6: V_{TN} VS DOSE

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[2] *W.R. Dawes, Jr., G.F. Derbenwich and B.L. Gregory, "Process Technology for Radiation Hardened CMOS Integrated Circuits," IEEE Journal of Solid State Circuits, SC-11, No. 4, p. 459, August 1976.*

one standard deviation on either side of the mean. This value, for both N- and P- channel devices, remains fairly constant from the unirradiated state through 10^6 rads (Si) dosage. The values shown remain well above the 300mV V_{TN} lower limit, which, if penetrated, would lead toward N-channel depletion mode behavior and risk of losing circuit functionality and excessive supply current drain.

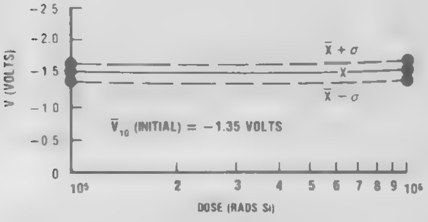


FIGURE 7. V_{TP} VS DOSE

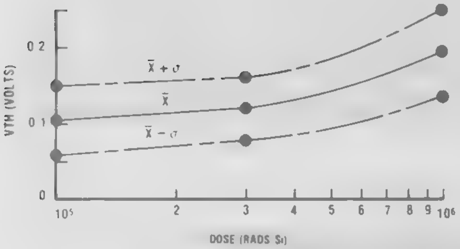


FIGURE 8: V_{TN} VS. DOSE

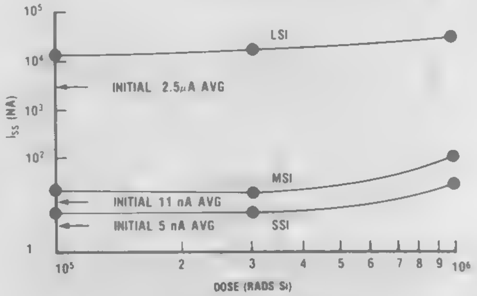


FIGURE 9: I_{SS} VS. DOSE

Figure 9 illustrates the supply quiescent current (I_{SS}) variation as a function of dose. Since I_{SS} is a function of die size, curves have been plotted for three levels of integration, SSI, MSI and LSI. In all cases, the leakage level at 10^6 rads (Si) does not increase by more than an order of magnitude from the initial value. The end point at 10^6 rads (Si) for LSI of 30μA is far below the high temperature (125°C) specification of 600μA for standard devices. The same results can be seen with MSI and SSI.

TABLE A. RADIATION EFFECTS DATA

(Graphs were obtained from the following devices which were irradiated with a Cobalt-60 source.)

DEVICE TYPE	FUNCTION	SAMPLE SIZE (AT EACH RAD LEVEL)
	SSI DEVICES	
1. CD4001	Quad 2-Input NOR	7
2. CD4011	Quad 2-Input NAND	7
3. CD4023	Triple 3-Input NAND	7
4. CD4049	Hex Buffer	7
5. CD4050	Hex Buffer	7
	MSI DEVICES	
1. CD4013	Dual "D" Flip-Flop	7
2. CD4014	8 Stage SR	7
3. CD4017	Decade Counter	7
4. CD4027	Dual "J-K" Flip-Flop	7
5. CD4029	Up/Down Counter	7
6. CD4053	Analog Multiplexer	7
7. CD4066	Quad Switch	7
	LSI DEVICES	
1. MM54C200	256-Bit RAM	7

NOTE: 91 parts irradiated at each of three radiation levels:

1×10^5 Rads (Si)
3×10^5 Rads (Si)
1×10^6 Rads (Si)

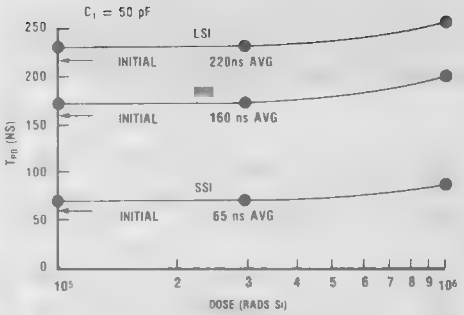


FIGURE 10: t_{PD} VS DOSE

Figure 10 illustrates circuit propagation delay, t_{PD}, as a function of dose. The plot, similar to Figure 9, is divided into three categories (LSI, MSI, SSI). The propagation delay value at 10^6 rads (Si) for all three categories increased roughly 20 - 25% from the initial value, well within desirable operating tolerances. In Figures 5 through 10, the biasing conditions during irradiation were: $V_{DD} = 10V$, $V_{IN} = 10V$, $V_{SS} = 0V$.

Hardness Assurance and Reliability

A sampling plan has been established to ensure radiation hardness to 10^5 and 10^6 rads, since ionizing radiation degrades IC performance and cannot be used for 100% screening. In addition, an intensive program to evaluate the reliability characteristics of radiation hardened CMOS circuits is underway. 476 devices of the CD4001AD-RH, CD4011AD-RH, and MM54C200-RH types have been tested and have operated for over 800,000 hours without a failure. This corresponds to a failure rate less than 0.125%/1000 hours at 125°C with a 60% confidence level.

Table B outlines the plan used to assure hardness of devices built from a given wafer lot. Sample devices are assembled in accordance with sampling plan A or B, depending on whether 10^5 or 10^6 rads (Si) hardness, respectively, is required. Sample devices are tested, irradiated, and retested, and must pass the appropriate post-radiation electrical limits outlined in Table C for the production lot to be qualified. The production units are capable of

TABLE B. HARDNESS ASSURANCE PLAN

I. Plan A	
Sample Size (Wafers)	2
Sample Size (Devices/Wafer)	3
Total Devices Irradiated	6
Accept Level	0 Rejects
Reject Level	1 Reject
II. Plan B	
Sample	Each wafer
Sample Size (Devices/Wafer)	3
Accept Level	0 Rejects per Wafer
Reject Level	1 Reject per Wafer
III. Product Flow:	
A. For 1 × 10^5 rads (Si) qualification:	
1. Qualify lot with Plan A	
2. If lot fails, qualify wafers individually with Plan B	
B. For 1 × 10^6 rads (Si) qualification:	
1. Qualify wafers individually with Plan B	

meeting MIL-M-38510 electrical test limits, when available, as well as National's RETS limits.

Extended Total Dose Rate [to 10^7 Rads (Si)]

Much of the data generated in the course of our testing indicates that the resistance of our CMOS products extends at least one order of magnitude above the 10^6 level already demonstrated. Figures 11 and 12 illustrate measured shifts from pre-irradiation values in P- and N-channel threshold voltage, V_{TP} and V_{TN}, respectively, up to total dose levels of 10^7 rads (Si). Of special interest is the change in slope of the V_{TN} versus dose characteristic at levels just above the 10^6 rads (Si).

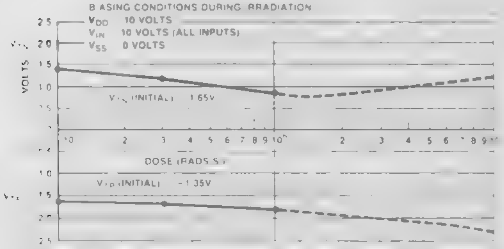


FIGURE 11: VARIATION OF V_{TN} AND V_{TP} WITH RADIATION DOSE-EXTENDED TO 10^7 RADS (Si)

At this level, negative charge from the silicon substrate arrives in the gate oxide at a rate faster than radiation-created positive charge. This causes V_{TN} to return toward its initial value as dose level is increased even further while increases in V_{TP} still remain within reasonable limits for satisfactory circuit operation.

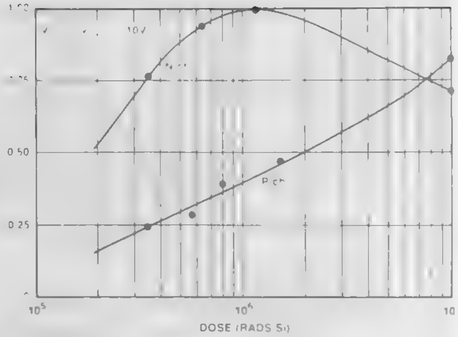


FIGURE 12: NORMALIZED V_T VS. RADIATION DOSE

Dose Rate Performance

When CMOS ICs are subjected to large bursts of ionizing radiation, hole-electron pairs are created in the silicon substrate. The resultant current flowing through the high resistivity P-and N-substrates can cause voltage differences which may impair circuit performance in one of the following ways.

One: LATCH-UP.

A CMOS circuit contains the structural elements required to form a four layered Schockley diode switching device as illustrated

TABLE C. POST-RADIATION SPECIFICATION*

PARAMETER	POST 10^5 RADS (SI)	POST 10^6 RADS (SI)
Threshold Voltage		
V_{TN}	0.45V (min)	0.20V (min)
V_{TP}	2.50V (max)	2.80V (max)
Quiescent Current		
(I_{SS}), V_{DD} = 10V		
Gates	2.0μA (max)	10.0μA (max)
Flip-Flops	5.0μA (max)	20.0μA (max)
MSI	15.0μA (max)	50.0μA (max)
LSI	50.0μA (max)	100.0μA (max)
Prop Delay, V_{DD} = 10V, C_D = 50pF	<25% degradation from pre-rad spec	<45% degradation from pre-rad spec

*Gamma irradiation from a Cobalt-60 source, worst case biasing at V_{DD} = 10 volts.

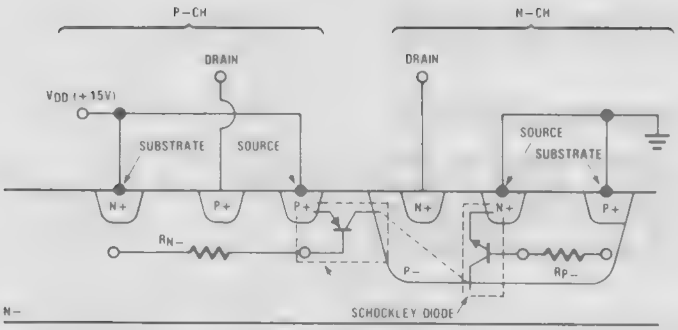


FIGURE 13 CROSS SECTION OF CMOS CIRCUIT ELEMENTS WHICH MAY LEAD TO LATCH UP DURING IONIZING RADIATION BURSTS

in Figure 13. The emitter-base junctions of the lateral PNP and vertical NPN which comprise the Schockley diode are normally prevented from becoming forward biased by the circuit metallization. Because of this, the Schockley diode will be in the off state during normal circuit operation and will pose no threat to reliable circuit performance.

Sufficiently high values of burst radiation can cause currents to flow through substrate resistances, R_{N-} and R_{P-}, to cause forward biasing of the parasitic PNP and NPN emitter-base junctions and turn on the Schockley diode. The excessive flow of supply current which accompanies turn-on of the Schockley diode has been found to occur in the range of 10^8 to 10^{10} rads (Si)/sec on many CMOS circuits.

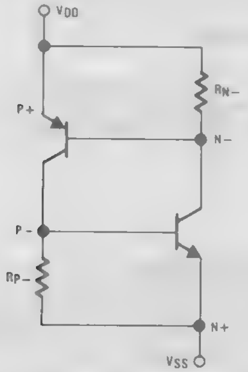


FIGURE 14: LATCH-UP EQUIVALENT CIRCUIT FOR BULK CMOS STRUCTURE

The basic circuit required for latch-up to occur is illustrated in figure 14. It consists of a parasitic bipolar NPN and PNP transistor sharing a common collector-base junction. The two requirements necessary for turn on of this device are:

1. The product of the common emitter current gains of the two devices, β_{PNP} and β_{NPN}, must satisfy the relationship $\beta_{NPN} \bullet \beta PNP \geq 1$, and
2. The emitter-base junction of the two transistors must become forward biased to about 0.6V or greater.

In normal operation, condition No. 1 will be met, but condition No. 2 will not be met, permitting latch-up free operation.

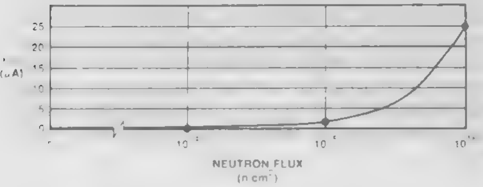
This problem can be completely eliminated by reducing to less than unity the product of the common emitter current gains of the NPN and PNP devices comprising the Shockley diode. One technique which has been successfully employed to eliminate the latch-up problem has been the use of neutron irradiation to lower minority carrier lifetime in the silicon substrate which directly affects parasitic bipolar current gains. As the values in Table D indicate,

TABLE D. LATCH-UP PERFORMANCE

DEVICE	V_{DD}	DOSE REQUIRED FOR LATCH-UP CONTROL (NON NEUTRON TREATED)	NEUTRON TREATED*	UNITS
CD4006	10V	$>9.4 \times 10^9$	$>9.4 \times 10^9$	Rads (Si)/sec
CD4011	10V	3.1×10^9	$>9.4 \times 10^9$	Rads (Si)/sec
CD4012	10V	2.0×10^9	$>2.4 \times 10^9$	Rads (Si)/sec
CD4053	10V	3.2×10^8	$>9.4 \times 10^9$	Rads (Si)/sec
MM54C200	5V	$>2.2 \times 10^{10}$	$>8.8 \times 10^{11}$	Rads (Si)/sec

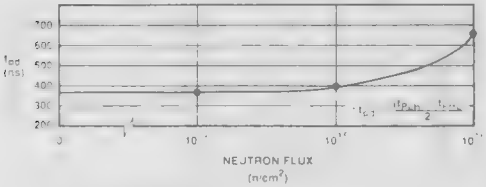
*Neutron treated parts were subjected to a neutron flux of 1×10^{14} neutrons (fast)/cm^2.

neutron treatment of parts which exhibit latch-up at 3 × 10^8 and 3 × 10^9 rads (Si)/sec resulted in latch-up free operation up to the limit of the burst simulation equipment, 10^{10} rads (Si)/sec. By treating wafers with neutron fluxes on the order of $10^{14}/cm^2$, this enhanced circuit performance is obtained without sacrificing parametric performance. This is illustrated in Figures 15 and 16, which plot supply current drain and propagation delay, respectively, versus neutron flux and show no significant degradation at the $10^{14}/cm^2$ level.



DEVICE USED MM54C200D RH
(256-BIT RAM)

FIGURE 15 DEVICE QUIESCENT SUPPLY CURRENT VS NEUTRON FLUX



DEVICE USED MM54C200D RH
(256-BIT RAM)

FIGURE 16 PROPAGATION DELAY VS NEUTRON FLUX

Another method which may be used to reduce minority carrier lifetime and achieve latch-up free operation is the use of gold doping in the wafer fabrication process in order to reduce the current gain product to below unity and thus insure latch-up free operation. This approach is presently being investigated in the National Semiconductor development laboratory.

Two: DATA-UPSET

This effect results in the loss of stored data in a circuit after being subjected to burst radiation. It is typically of most concern in circuits such as memories and shift registers, where stored data bits are not directly coupled to circuit inputs. The problem is apparently caused during ionizing burst radiation exposure when one or more of the circuit's parasitic bipolar devices becomes turned on and causes asymmetric current flows in the data storage circuit, leading to a reversal of the stored data state.

Table E shows the effect that neutron treatment of an MM54C200D/RH 256-bit static RAM has on the dose rate at which upset occurs. The effect of gain degradation of parasitic devices on data upset is not nearly as dramatic as it is in the case of latch-up. Although neutron fluxes in excess of $10^{15}/cm^2$ cause significant alterations in semiconductor material properties and circuit electrical parameters, Figures 15 and 16 indicate that the circuits tested would still meet data sheet requirements after irradiation in excess of 2 × $10^{15}/cm^2$. At this level the tolerance to data upset exhibits about a threshold improvement over untreated devices. Almost an entire order of magnitude improvements in data upset tolerance can be obtained with treatment at $10^{16}/cm^2$ if the user can tolerate the degraded propagation delay and increased supply current drain occurring at this level.

RAD Hard CMOS Reliability

Radiation hardness, however, is of no value to the system user if it is accomplished at the sacrifice of device reliability. To confirm device reliability, each of 476 units from five lots were subjected to 2,016 hours of burn-in at 125°C. The results of this testing are shown in Table F.

The two asterisked lots received a 168 hour pre burn-in prior to the operating life test. The total device hours were 804,384 which represents a

TABLE E. DATA UPSET PERFORMANCE

	DOSE RATE NEEDED TO INDUCE DATA UPSET		
NEUTRON FLUX ($N\text{-}FAST/CM^6$)	CD4006D 18-BIT SHIFT REGISTER V_{DD} = 10V	MM54C200D (MEMORY ENABLED) 256-BIT RAM. V_{DD} = 5V	UNITS
0 (control)	4.7 × 10^8	1.76 × 10^8	Rads (Si)/sec
1 × 10^{14}	4.7 × 10^8	2.00 × 10^8	Rads (Si)/sec
1 × 10^{15}	—	5.00 × 10^8	Rads (Si)/sec
1 × 10^{16}	—	1.17 × 10^9	Rads (Si)/sec

projected 0.11%/1000 hours failure rate at a 60% confidence level. This falls well within the reliability requirements of even the most stringent programs.

In addition to this initial sampling, 100% burn-in screening, as well as operating life testing, has been performed on many lots that have been produced for various customers. The results of this additional testing have continued to demonstrate that rad hard devices are as reliable as the Table F data indicates.

Radiation Hardened Linear Devices

Although most bipolar logic devices tend to be inherently hard when exposed to total-dose radiation, many bipolar linear devices will begin to degrade when exposed to relatively low levels of radiation. The causes are similar to those seen in MOS radiation exposure related failures. Linear devices, unlike most bipolar technologies, utilize lateral transistors as well as vertical transistors. Lateral transistors suffer from beta degradation as a result of the oxide and interface charges induced by high levels of radiation.

The solution to linear radiation problems, however, is quite different than what we have described above for CMOS devices. Total modification of the fabrication process is needed in order to achieve megarad hardness on linear devices. We have developed megarad versions of the LM108A and LM101A, with other devices now in development. We have extensive research and development currently underway in this area, for we feel that a broad line of rad hard linear devices is essential if systems designers are to achieve total systems hardness.

TABLE F. RAD HARD OPERATING LIFE RESULTS

DEVICE TYPE	SAMPLE SIZE	V_{DD}	REJECTS				
			168 HR.	336 HR.	504 HR.	1008 HR.	2016 HR.
CD4001AD*	115	+15V	0	0	0	0	0
CD4001AD	119	+12V	0	0	0	0	0
CD4001AD	112	+12V	0	0	0	0	0
CD4001AD	90	+12V	0	0	0	0	0
MM54C200D*	40	+12V	0	0	0	0	0
TOTAL:	476		0	0	0	0	0

*Received 168 hour burn-in prior to operating life test.

RAD Hard CMOS

Device	Series	Device	Series	Device	Series	Device	Series	Device
CD4001	A/B	CD4018	B	CD4040	A	CD4071	B	MM54C04
CD4002	A	CD4019	B	CD4041	A	CD4073	B	MM54C14
CD4006	A	CD4020	A	CD4042	B	CD4075	B	MM54C86
CD4007	A	CD4021	A	CD4043	A	CD4076	B	MM54C173
CD4008	B	CD4022	B	CD4044	A	CD4081	B	MM54C174
CD4009	A	CD4023	A/B	CD4048	B	CD4093	B	MM54C192
CD4010	A	CD4024	B	CD4049	A	CD40106	B	MM54C193
CD4011	A	CD4025	A/B	CD4050	B	CD40174	B	MM54C200
CD4012	A	CD4027	B	CD4051	B	CD40192	B	MM54C901
CD4013	B	CD4028	B	CD4052	B	CD40193	B	MM54C902
CD4014	A	CD4029	B	CD4053	B	CD4514	B	MM54C903
CD4015	A	CD4030	A	CD4066	B	CD4515	B	MM54C904
CD4016	A	CD4031	B	CD4069	A	CD4518	B	MM54C906
CD4017	B	CD4035	B	CD4070	B	CD4584	B	MM54C907

Table G. Radiation Hardened CMOS
Qualified Parts List
Devices Hard to 10^6 Rads (Si)

National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or do not wish to do so, yet need significantly better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembed boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the reapir and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher that it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliabilty cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

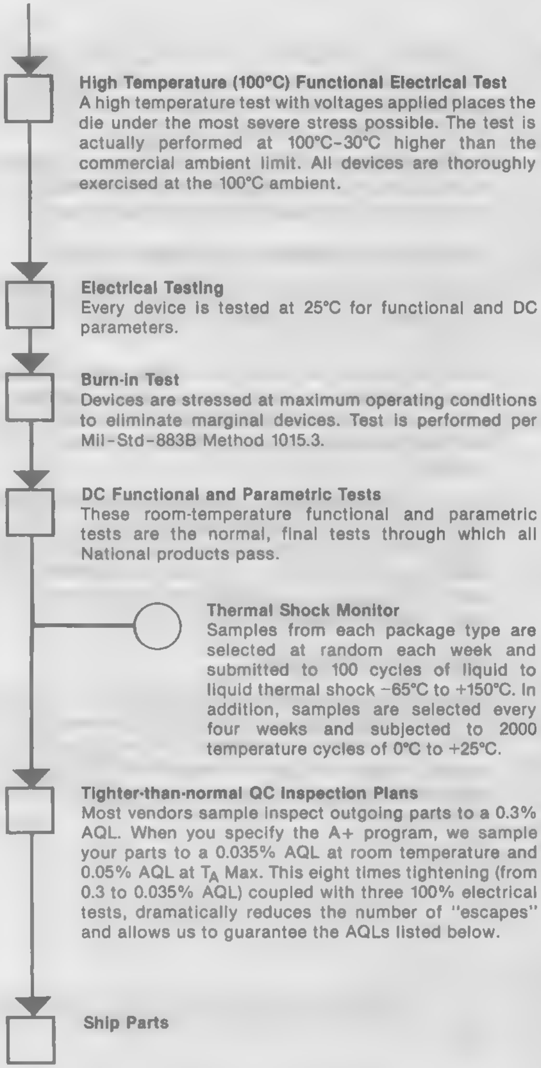
National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.



High Temperature (100°C) Functional Electrical Test
A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing
Every device is tested at 25°C for functional and DC parameters.

Burn-in Test
Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per Mil-Std-883B Method 1015.3.

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor
Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.4%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

B+ Program

B+ Program: a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality *and* the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembed boards.
- Reduces field failures.
- Reduces equipment down time.

Reliabilty Saves You Money

With the increases population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at least two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair, and rework costs have risen — and promise to continue to rise — but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be — literally — hundreds of times more than the cost of the failed IC itself.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliabilty the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

Quality Improvement

When an IC vendor specifies 100 percent final testing of its parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

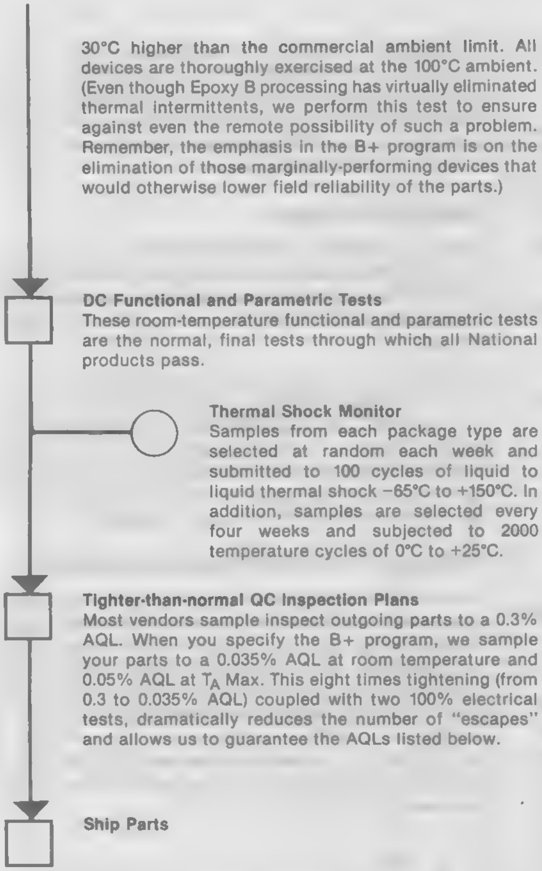
We've stated that the B+ program improves both the quality *and* the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

SEM
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test
A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C —



30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.)

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor
Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the B+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with two 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sampling plans used in our B+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.4%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

Introduction

With the entry into the integrated circuit marketplace of Complementary-Metal-Oxide Semiconductor (CMOS) technology; an electronic revolution comparable to that following the introduction of bipolar transistor technology was stimulated. The trend toward increased use of CMOS in industrial and consumer systems came about principally because of the unique properties associated with these devices. For example, P- and N-channel enhancement mode transistors are combined on the same chip, which makes possible high-speed operation, high noise immunity, and low stand-by power dissipation in the nanowatt range. Only one power supply is required, and the circuit is operated so that only one transistor is on at a time. Significant power is dissipated only during change of state. The combination of these advantages, coupled with extremely small device size and National's stable and reliable CMOS fabrication process, has contributed to certain unique applications which could not be handled by more conventional MOS technologies.

National Semiconductor first entered the MOS market in early 1968 by producing established P-channel metal gate product. By mid-1972, National had introduced its first CMOS product line. The salient points in the chronological history of CMOS logic at National are:

1. National introduces in early-1972 the CD40xxA series as its first CMOS product line. These parts were designed as a second source to the RCA CMOS products.
2. By mid-1972, a second product line, the MM74Cxxx series, is introduced. These are proprietary CMOS parts which are pin and functional equivalents of many of the most popular devices in the 74xx TTL series.
3. CMOS logic is qualified by MIL–M–38510 Program in late 1975. This program is designed to standardize the integrated circuit industry and at the same time provide the customer with the highest possible quality level for the required application.
4. Significant improvements in the majority of the CD40xxA series result in the introduction of the CD40xxB series in mid-1976. Internal buffers, acting in most cases as a pair of inverters, are added to all outputs. This results in making the output drive (in both directions) a uniform and standard value which in turn makes rise and fall times more nearly identical.
5. In early 1977, National introduces its analog-to-digital (A-to-D) converters into the series: the ADC 08xx, a Single Chip Data Acquisition System; and the ADC 3xxx, a 3½- to 3¾-digit Digital Volt Meter (DVM) chip.
6. In recognition of the necessity of CMOS logic product to withstand exposure to radiation in satellite systems and space vehicles, National in early 1977 introduces the industry's first complete line of radiation-hardened devices. Both the traditional 40xx series and National's own TTL compatible MM74Cxx series can withstand radiation exposures of 10^6 Rads.

And today, National Semiconductor offers a broad spectrum of CMOS logic devices:

- 20 in the CD4000 A series
- 85 in the MM54C/74C series
- 67 in the CD4000B series
- 13 CD45XX series
- 5 A-to-D Converters
- 57 Radiation Hardened devices.

The report which follows describes National's quality and reliability program, including test-results data for National's integrated CMOS product in Epoxy B. The basic principles of CMOS will be presented, together with National's processing philosophy, production techniques, and the methods and programs now in place to assure the end product's quality and reliability.

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Device Fabrication

CMOS wafer fabrication is designed to produce reliable, high-performance devices which require minimum handling restrictions. At National Semiconductor, these objectives are achieved through the use of advanced materials, process innovations, and rigorous process controls.

The substrate material used in the CMOS process is [1-0-0]-orientation N-type silicon rather than the commonly selected [1-1-1]-orientation type. Coupled with controlled processing, this substrate permits the fabrication of MOS transistors with threshold voltages up to half as low as that produced on [1-1-1]-orientation silicon. Lower threshold voltages allow higher-speed circuit operation with lower supply voltages. In addition, the threshold voltage distribution from run to run is much tighter, so that long-term uniformity of device characteristics is assured.

The stability of CMOS characteristics depends directly on the level of contamination in the gate oxide. National's proprietary oxidation procedure and cleaning methods are capable of producing ultra-clean oxides. In order to ensure low levels of oxide contamination in production, capacitance-voltage (C-V) process controls have been installed.

All production oxidation and evaporation systems are monitored on a regular basis using the capacitance-voltage method. An MOS capacitor is fabricated and drifted under +15V bias at 275°C for two minutes. The shift in the C-V plot is a measure of the ionic contamination in the oxide under evaluation. This method is also used for investigations of process changes and innovations. These measurements assure rapid detection and correction of production process difficulties before contaminated material can leave the wafer processing area.

An additional check on stability is performed on completed wafers. Fields of $\pm 2 \times 10^6$V/cm are applied to C-V test dots designed into the device die while the wafer is heated to 275°C for two minutes, then cooled to room temperature. The C-V shift is measured before and after heating for both bias conditions. The maximum permissible shift in threshold voltage is 0.40V with typical shifts running less than 0.15V.

Moreover, National's CMOS devices have a double input diode protection network designed to prevent catastrophic failures caused by positive- or negative-going voltage transients. This effective input protection network, coupled with excellent oxide integrity, reduces the handling restrictions required on CMOS devices. A detailed guide to the handling requirements of CMOS parts is given in the last section of this report.

The following is a pictorial representation of National's CMOS device fabrication. (Please note that the drawings are not to scale.)

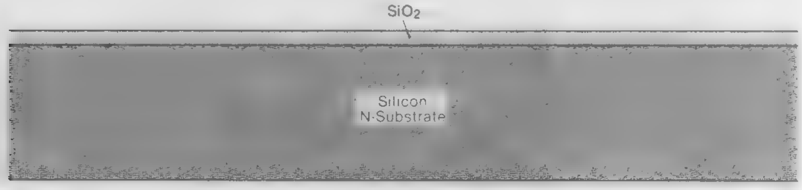


Figure 1. Initial Oxidation, Thermally Grown Silicon Dioxide Layer on Silicon Substrate Surface

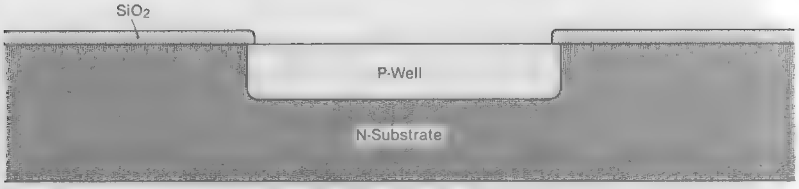


Figure 2. P-Mask & Formation of P-Well Tub in which N-Channel Devices will be Located

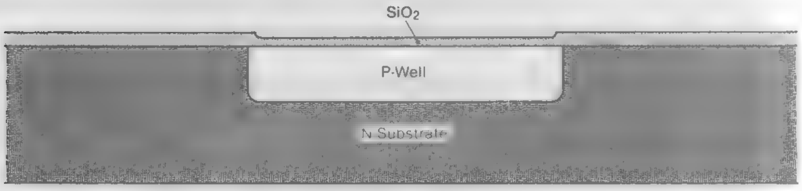


Figure 3. P-Well Oxidation, Thermally Grown Silicon Dioxide Layer over P-Well Area

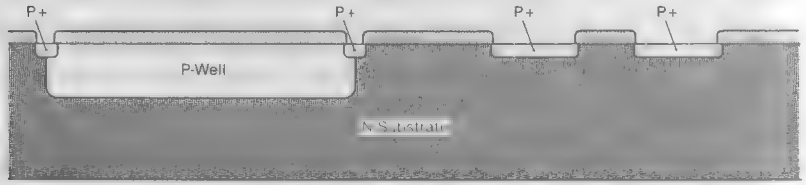


Figure 4. P+ Mask & Formation of Low Resistance P+ Type Pockets in P-Well and N-Substrate

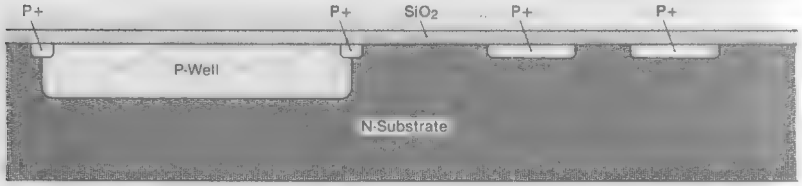


Figure 5. P+ Oxidation, Thermally Grown Silicon Dioxide Layer over P+ Type Pockets

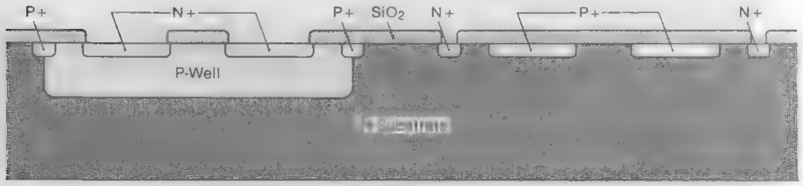


Figure 6. N+ Mask and Formation of Low Resistance N+ Type Pockets in P-Well & N-Substrate

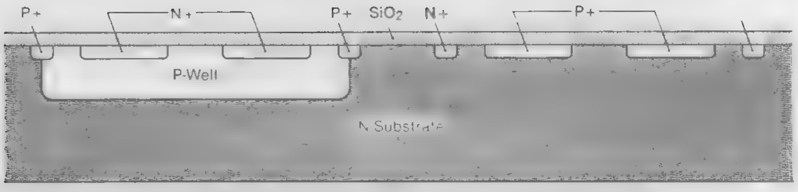


Figure 7. N+ Oxidation, Thermally Grown Silicon Dioxide Layer over N+ Type Pockets

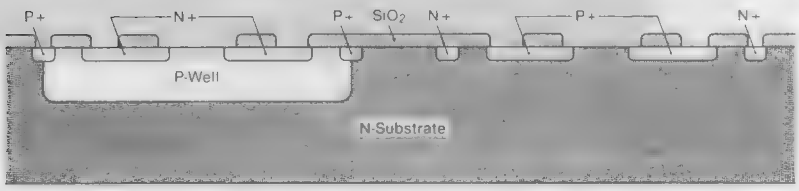


Figure 8. Composite Mask & Openings to N and P Channel Devices

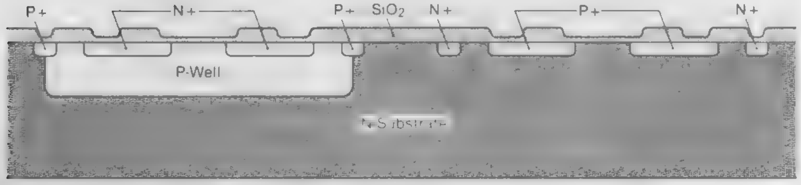


Figure 9. Gate Oxidation, Thermally Grown Silicon Dioxide Layer over N and P Channel Devices

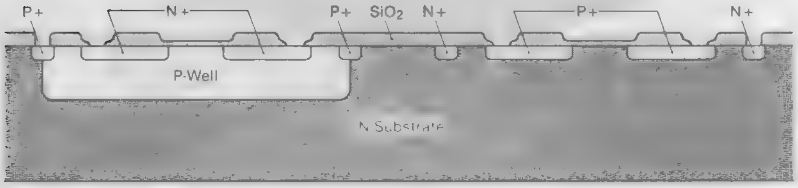


Figure 10. Contact Mask & Openings to N and P Channel Devices

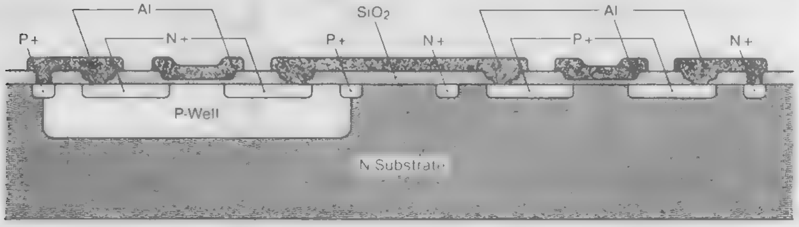


Figure 11. Metallization, Metal Mask, Resulting in Gate Metal & Metal Interconnects

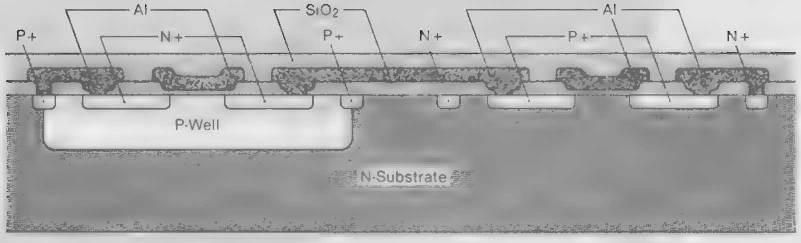


Figure 12. Passivation Vapox, Deposited Silicon Dioxide over Entire Die Surface

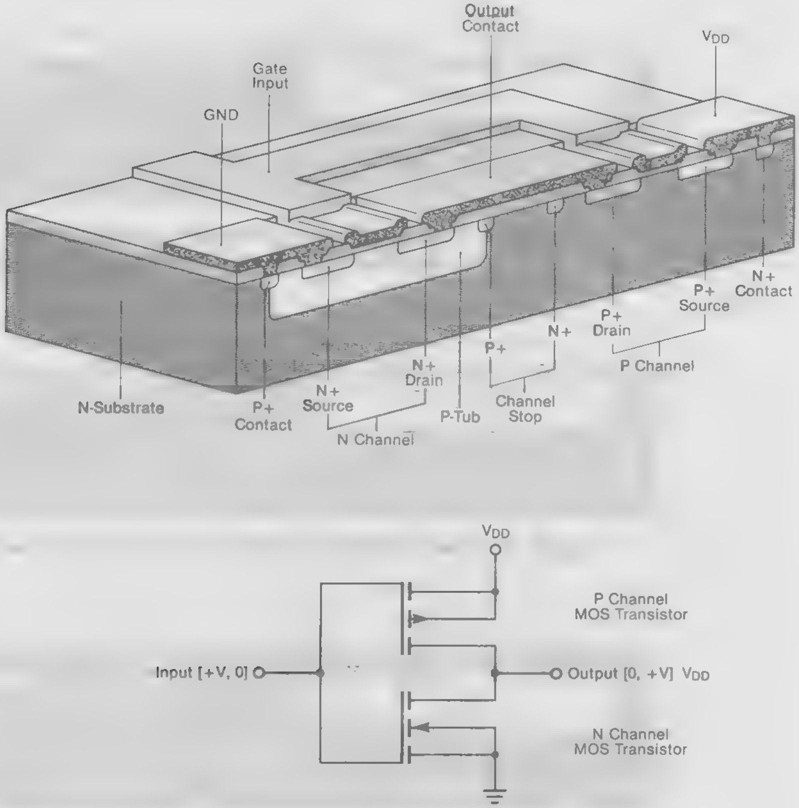


Figure 13. Basic CMOS Inverter Circuit

and internal procedures used in the manufacture of highly reliable CMOS microcircuits. No amount of testing and sorting will replace skill and extreme care in production processing.

The main task, therefore, is not only how to make a reliable product but also how to maintain the reliability level which is obtainable from a suitable design. The answer lies in meticulous control over production techniques and in painstaking process control checks and quality control gates after critical operations.

The following outline briefly describes the standard CMOS production process and indicates each of the steps in this flow at which process control and checking are undertaken by Quality Assurance engineers and technicians.

1. Incoming Raw Materials are Received

Silicon wafers, wires, frames, plastic, photo resist, chemicals, molding compounds, emulsion work plates, etc.

Quality Assurance Incoming Inspection

The raw materials are purchased from a qualified vendor and must meet stringent material procurement specifications. Samples are inspected and tested to dimensional, physical, mechanical, chemical, and environmental specifications. Each vendor must maintain a continuous history of acceptable quality shipments in order to remain on National's list of qualified vendors.

2. Wafer Processing

All operations are carried out in closely monitored clean conditions. Material waiting for subsequent operations is stored under laminar-flow hoods (Class 100, Federal Standard 209A). All wafers are visually inspected for defects under collimated light prior to initial oxidation. Wafers are rejected which fail to meet the criteria defined by written process specifications.

3. Initial Oxidation

5,000 Å of silicon dioxide are thermally grown. An optical measurement of oxide thickness is made.

4. P-Mask

This masking step is used to form the P-well in which N-channel devices are to be located.

Optical inspection is made at 400X power for characteristics such as cleanliness, continuity, and definition. Precision optical-dimensional measurements using an image-shearing microscope are made to check the accuracy of device geometry.

5. Pre-Ion-Implant Oxidation

A thin layer of silicon dioxide is thermally grown. This oxidation is primarily done to improve the uniformity of the subsequent ion implantation.

6. Ion Implantation of CMOS P-Well

Ion implantation is inherently a low-temperature process offering excellent boron-impurity control of surface doping concentrations.

Ion Implant P-Well Quality Control

The boron-ion concentration is checked by measuring V/I on a specially prepared N-type test wafer.

7. Ion Implant P-Well Drive-in and Oxidation

A drive-in cycle including thermal annealing is followed by silicon-dioxide oxidation over the P-well.

8. P+ Mask

The second mask provides source and drain regions for P-channel devices, substrate-to-ground diodes (guard bands), and V_{DD} input diodes.

Etch Inspect Quality Control

Optical and dimensional inspections as described after the first masking operation above are repeated.

9. P+ Diffusion

All P+ regions are thermally doped followed by a drive-in and oxidation. Measurements are made to determine sheet resistance, junction depth, and field oxide thickness in the P+ source and drain diffused regions. Pre-deposition V/I and oxidation thickness are held within 10% of design values, which results in tighter electrical distributions.

10. N+ Mask

The third mask provides N-type source and drain regions in P-well for N-channel devices, channel guard bands, and V_{SS} input diodes.

Etch Inspect Quality Control

Optical and dimensional inspections (as previously described) are repeated.

11. N+ Diffusion

Source and drain regions in P-well are thermally doped followed by a drive-in and oxidation. As with P+ diffusion, measurements are made to determine sheet resistance, junction depth, and the field oxide thickness in the N+ source and drain diffused regions. Again, pre-deposition V/I and oxidation thickness are held within 10% of design value so as to have tighter electrical distributions.

12. Composite Mask

The fourth mask opens the thermal oxide over the N- and P-channel gate regions in preparation for gate oxidation.

Etch Inspect Quality Control

The same post-mask optical and dimensional inspections as described previously are repeated.

13. **Gate Oxidation**

A thin layer of silicon dioxide is thermally grown as drift-free gate electrical material over the N- and P-channel gate regions.

Gate Oxidation Quality Control

Interferometer measurements are made of the oxide thickness on specially prepared test wafers. An indirect evaluation of aluminum evaporation and of the quality of the cleaning process is obtained as a consequence of a control loop procedure.

14. **Metal Contact Mask**

The fifth mask opens the thermal oxide over the source and drain tubs of N- and P-channel devices as well as over N+ and P+ contacts.

Etch Inspect Quality Control

The same optical and dimensional inspections as performed before are repeated.

15. **Metallization**

A thin film of aluminum is sputtered in a vacuum over the entire surface of the wafer.

Metallization Quality Control

Metallization thickness is controlled in each production run by sectioning, the use of interferometers, etc. A dynamic capacitance voltage plot is taken to verify the absence of sodium contamination in the metallization process.

16. **Metal Mask**

The sixth mask is used to form aluminum interconnection patterns, contacts, and bonding gates.

Etch Inspect Quality Control

Previously described optical and dimensional inspections are repeated.

17. **Alloy**

Aluminum metal interconnections to device contact regions are alloyed.

18. **Passivation Vapox**

A chemically-vapor-deposited glass (vapox) provides metal scratch protection and getters positive mobile ionic charges.

Passivation Vapox Quality Control

The percentage of phosphorous concentration in the vapox is measured by diffusion from the deposited oxide source, and double-checked by analysis of the diffused layer surface concentration on test wafers using X-ray fluorescence techniques. Also measured are defect density and etch rate.

19. **Vapox Mask**

The seventh mask opens the vapox over the aluminum bonding areas.

Etch Inspect Quality Control

Once more, an optical etch inspection is made at 400X power to check on cleanliness, continuity, and definition. Precision optical-dimensional measurements using an image-shearing microscope are made to determine the accuracy of device geometry.

Electrical Test Quality Assurance

Together with the C-V test, measurements are made of electrical parameters sensitive to slight process variations, including transistor threshold, current gain, junction reverse-breakdown voltages, and diffused region sheet resistivities. MOS capacitors on test arrays are measured for fast surface-state density (Q_{SS}), mobile ionic contamination (Q_0), and the thickness of gate oxide dielectric. These data are used to maintain tight process controls.

20. **Dynamic Capacitance Voltage Plot**

A positive 15 volts are applied to a C-V dot designed into the device die while the wafer is heated to 275°C, held at temperature for two minutes, then cooled to room temperature. C-V plots of threshold voltage on N- and P-channels are made before and after heating to determine V_t.

21. **Product Wafer Probe**

Each die receives a complete functional test to all conditions and parameters specified on the device data sheet. Supply voltages are applied over the guaranteed ranges. Dice failing to meet any of these tests are inked for subsequent removal.

Epoxy B Package Processing Flow

Sorted Wafers are Received

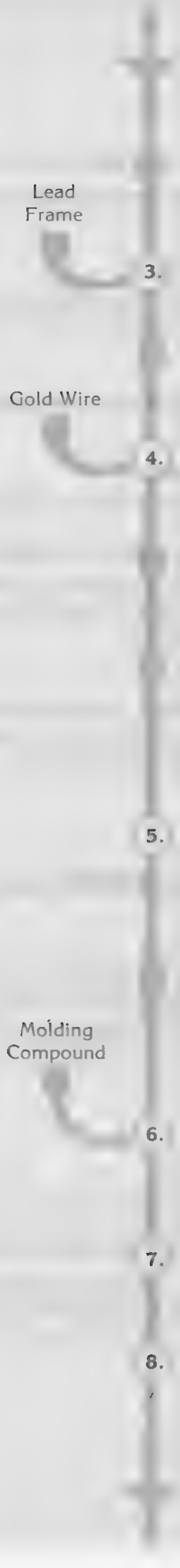
All dice on wafers have been 100% electronically tested. Electrical rejects are marked with an ink spot.

1. **Diamond-Saw, Break, and Plate Dice**

Inked dice are removed.

2. **Optical Die Sort**

100% optical microscope inspection at 100X to remove potentially unreliable dice.



Quality Control Surveillance Begins

Verification is made that the optical die sort was performed according to written specifications.

3. Die Attach

Polymer attachment of die to lead frame.

Quality Control Surveillance

Verification is made that the die-attach operation was performed according to written specifications.

4. Lead Bond

Thermocompression ball-bonding of gold wire to die and lead frame.

Quality Control Surveillance

Several times each shift, samples are checked from each machine and from each operator's work.

Quality Assurance Lead Bond Pull Test

Samples by lot from each operator are checked a minimum of twice per shift. All bonds are pulled to destruction. The force required to break the bond, and the location of the break, are recorded for process-control purposes.

5. Pre-Mold Optical Sort

100% optical microscope inspection at 30X for assembly defects. Devices are inspected for wafer processing anomalies, assembly work damage, completeness, and accuracy of assembly.

Quality Control Surveillance

Samples of each optical sorter's work are inspected to criteria which meet or exceed the applicable requirements of Mil–Std–883B, Method 2010.

6. Mold and Cure

Thermosetting plastic is transfer molded around the completed assembly. The plastic is then cured to insure mechanical and chemical stability.

7. Trim and Form Leads

Frame supports are removed and leads formed to desired configuration.

8. Tin Dip Leads (Non pre-plated frames only)

Frames which have not been plated prior to die attach (Step 3) are hot-solder dipped to provide protection against corrosion and for excellent solderability.

Quality Control Surveillance

Visual and mechanical quality are continuously monitored.

9. **Mark Package**

Devices are marked with National's part number, a date code (signifying mold week), and the National logo.

10. **Clip Rails**

Lead-frame rails are removed, leaving finished devices ready for test

11. **Electrical Test**

100% electrical test on all data-sheet parameters.

☐ **Quality Assurance Acceptance**

Each lot of finished devices is sample inspected and tested by Quality Assurance Inspectors for compliance with specifications.

12. **Pack and Ship**

Each shipment is inspected by Quality Assurance to be sure that the right devices are going in the right quantity to the right customer.

Environmental and Life Test Data of CD40XXC and MM74CXXN

As was noted in the Introduction, CMOS serves as an ideal solution for industrial and consumer (and aerospace) systems which cannot be handled by more conventional MOS technologies. In these critical applications, reliability is of major importance. The data which follow are the summations of 1979-1980 reliability tests conducted on commercial CMOS devices in Epoxy B.

Criteria

Two failure categories are considered:

1. **Degradation** — Devices which are still able to perform logical functions, but whose electrical parameters have drifted beyond published specifications.
2. **Catastrophic** — Devices with opens or shorts, or those which fail to perform logical functions because of increased leakage or a shift in any other electrical parameter.

Temperature Cycle Test Results

The air-to-air temperature cycle is conducted in accordance with Mil-Std-883B, Method 1010.2, from 0°C to 125°C, 10 minutes dwell time at temperature extremes, 2 second transfer time, 20 minutes per cycle.

Lots	Sample Size	Failures at: 1,000 Cycles	2,000 Cycles
12	2,500	0	1

Thermal Shock

The liquid-to-liquid thermal shock test is conducted in accordance with Mil-Std-883B, Method 1011.2, Test Condition C, −65°C to +150°C.

Lots	Sample Size	Failures at: 50 Cycles	100 Cycles
25	450	0	0

Autoclave (Pressure Pot)

The pressure pot test is conducted in a steam autoclave at 121°C, 15 psig, and 100% relative humidity for 96 hours.

Lots	Sample Size	No. Fail
52	1,200	5

High Temperature Storage

The high temperature storage test is conducted in accordance with Mil-Std-883B, Method 1008.1, Test Condition C, at 150°C.

Lots	Sample Size	Failures at: 168 Hrs	500 Hrs	1000 Hrs
9	210	0	0	1

Moisture Resistance

85°C, 85% relative humidity, static life conditions, biased with rated voltage.

Lots	Sample Size	Failures* at: 168 Hrs	500 Hrs	1000 Hrs
40	1,279	2	18	5

*Functional failures

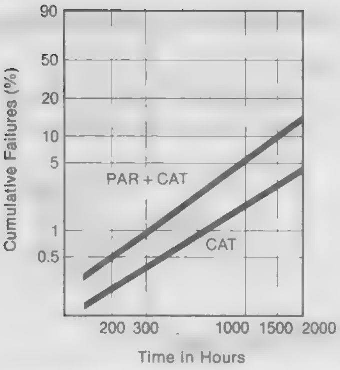


Figure 14. Failure Rate at 85°C/85% RH

High Temperature Operating Life (125°C, Bias = +15V)

Lots	Sample Size	Failures at: 168 Hrs	500 Hrs	1,000 Hrs	% Fail/ 1,000 Hrs.	MTBF Hours
40	1,472	5	4	8	1.2%	0.86×10^5
Total Test Hours: 1,472,000						
Equivalent Hours at 70°C: 125×10^6†					0.014%	6.90×10^6
Equivalent Hours at 45°C: 1562×10^6†					0.0012%	83.00×10^6

† Activation Energy = 0.7 eV

Notes:

1. The failures are data sheet limit failures.
2. Failure rate (λ), or predicted percent failure per 1,000 hours, is at 60% Confidence Level.
3. Failure rate percentage is the inverse of Mean Time Between Failures (MTBF).
4. Failure rates derived for 70°C and 45°C were obtained using acceleration factors related to actual test ambient temperatures.

The following figure shows the Field Failure Rate predicted for CMOS devices when operated at 70°C. The Infant Mortality section of the curve is shaded because Infant Mortality is strongly influenced by numerous variables such as handling, system-induced voltage transients, temperature, environment, mechanical stress, etc., and therefore varies widely.

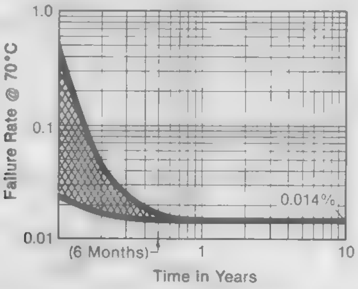
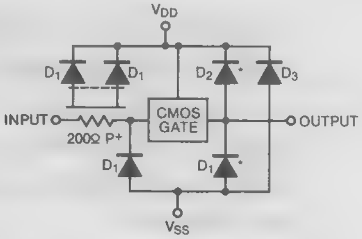


Figure 15. Field Failure Rate at 70°C

The single, most prevalent cause of "Infant Mortality" field failures in CMOS microcircuits is gate oxide damage. This can result from any transient voltage condition — electrostatic discharge (ESD), electrical noise, inductive spikes, etc. Effective input protection circuitry (see page 2 for further discussion), such as that used on National's CMOS chips, can provide effective protection provided the gate oxide itself is inherently reliable. National's standard gate oxide is designed to withstand 80 volts. As in any process, there is always some deviation from the normal. Nevertheless, it has been proven by National Reliability Engineering analyses that most devices which fail because of gate oxide damage actually have inferior gate oxide to start with — or an oxide which will rupture at voltages considerably below the "3 sigma limit" of the normal distribution.

National has improved its gate oxidation process in the areas of cleaning, masking, and controls to the point where the "3 sigma limit" is as small as possible. This guarantees that the inherent reliability of the process is preserved. Thus, the chance for failure caused by gate oxide rupture is drastically reduced. Translated to field performance, this means an absolute minimum of "Infant Mortality" failures in the operation of CMOS devices in their end-use environment.



Diode Breakdown
$D_1 = 25$ Volts
$D_2 = 60$ Volts
$D_3 = 100$ Volts
*These are Intrinsic Diodes

Handling and Test Guide

Introduction

All CMOS low-threshold devices are susceptible to damage by the electrostatic discharge (ESD) of energy through the devices. This is because the gate oxide thickness of such devices is in the range of 1,000Å to 1,100Å, which limits the maximum voltage that can be applied (to the input of the device) to 80V with a reasonable safety factor. (For a fuller description of ESD and its possible latent effects on microcircuits, see National Semiconductor's *Reliability Physics Brief, RPB–02*, July 1978, and *Reliability Physics Brief, RPB–07*, January 1980.) Although all CMOS devices have input protection networks which are effective in a large number of device-handling situations, they are not effective in 100% of the cases (please refer to specific devices in National's *CMOS Data Book*).

In order to be totally safe, proper handling procedures must be used to eliminate damage and subsequent yield loss caused by static electrical charges. It is the purpose of this application guide to outline proper handling procedures for CMOS devices.

General Handling Procedures

1. The leads of CMOS devices should be in contact with conductive material to avoid build-up of static charge. Containers used for transporting or storing CMOS components should be made of such material or lined with anti-static material. Rails for handling and shipping MOS devices should be made of electrically conductive material or be made static-free by an appropriate surface coating. In no case should CMOS devices be inserted into polystyrene foam or other high-dielectric materials. Any surface coating which is not at ground potential should not come in direct contact with device pins.

2. Devices should be packed in conductive containers, rails, or envelopes for storing. In addition, devices should be kept at ground potential and should never come in contact with non-conductive plastics.

3. All electrical equipment should be hard-wired to ground. Soldering iron tips, metal parts of fixtures and tools, and all handling systems should be grounded.

Cleaning

1. Devices should be cleaned by a solvent which will assure complete removal of foreign matter, flux, residual matter, etc., from the exterior of the package.

2. A static-neutralizing ion blower should be used when manually cleaning devices or sub-assemblies with brushes.

3. All automatic cleaning should be grounded.

4. All cleaning baskets should be grounded.

Assembly

1. Sub-assembled modules and printed circuit boards should be manufactured and handled using the same procedures as those described above for individual CMOS devices.

2. CMOS parts should be the last to be inserted into printed circuit boards or systems so as to avoid overhandling.

3. Circuit boards containing CMOS devices which are being transported between work stations and test areas should be contained in anti-static material or have all board terminals shorted together using a conductive shorting bar. Only handling trays of conductive material should be used.

4. All automatic insertion equipment, solder machines, metallic parts of conveyor systems, and soldering irons should be grounded.

Note: These precautions should be taken until the sub-assembly is inserted into the complete system in which the proper voltages are applied. Sub-assemblies should never be constructed, fixtured, stored or transported in polystyrene or any other high-dielectric materials.

General Operating Procedures

The National CMOS product line is comprised of many different device types for a variety of applications. The following operating procedures apply in a general sense to all CMOS devices, but reference to device specification sheets is still necessary to assure correct operating values.

A. Before making any physical connections or applying any external signal sources, be sure that all power supplies are off. Be sure, also, to observe proper static ground conditions.

B. Power supplies should be turned up slowly to the necessary voltages so as to avoid rapid supply changes.

C. After power supplies have been turned on, apply external input signals.

Note: Failure to perform the power-on procedure in this order can result in damaged CMOS circuitry.

D. To power down, remove input signals first, then turn power supplies off slowly.

E. If CMOS devices are operated at an elevated environmental temperature, allow devices to reach room temperature before they are powered down.

F. Do not leave inputs to any CMOS device unused. For NAND gates the unused inputs should be tied to V_{DD}; unused inputs to NOR gates should be tied to ground. Tying unused inputs to used inputs will result in an increase in source current of a NAND gate, and in an increase in sink current of a NOR gate.

Testing

1. Use grounded metallic fixtures where possible. Any surface that is not at ground potential should not come into direct contact with device pins.

2. Use a static-neutralizing ion air blower when running automatic handlers. Use conductive handling trays when transferring devices.

3. Do not insert devices or boards with power turned on.

4. Ensure that AC signals do not cause excessive current leakage.

Electrical Failure Modes Caused by Improper Handling

If proper handling techniques are not followed, it is likely that the generation of static electrical discharges will damage the CMOS devices, resulting in inoperable or degraded parts. Typical failure modes are:

1. Shorted or open gates;
2. Shorted or leaky input protection diodes;
3. Open metal paths in the device input circuitry; and
4. Degraded device characteristics, especially g (mutual transconductance or "gain").

The presence of these failure modes can be detected easily using a transistor curve tracer.

Section 8

Application Notes

CMOS, the Ideal Logic Family

National Semiconductor
Application Note 77
Stephen Calebotta

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

Well, that ideal logic family is here — almost. The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1MHz with a 50 pF load is less than 10mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, -55°C to +125°C or 74C, −40°C to +85°C. Table 1 compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

TABLE 1. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters.

FAMILY	V_{CC}	V_{IL} MAX	I_{IL} MAX	V_{IH} MIN	I_{IH} 2.4V	V_{OL} MAX	I_{OL}	V_{OH} MIN	I_{OH}	t_{pd0} TYP	t_{pd1} TYP	P_{DISS}/GATE STATIC	P_{DISS}/GATE 1 MHz, 50 pF LOAD
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	–	3.5		0.4	*360μA	2.4	*100μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	–	8.0		1.0	**10μA	9.0	**10μA	25	30	0.00003 mW	5 mW

*Assumes interfacing to low power TTL.

**Assumes interfacing to CMOS.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in Figure 2-1. It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.

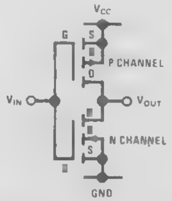


FIGURE 2-1. Basic CMOS Inverter.

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomeclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2-2 shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of V_{GS} = 15V (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for V_{DS}'s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS}'s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS}'s, there are similar curves except that the magnitude of the I_{DS}'s are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The P-channel transistor exhibits essentially identical, but complemented, characteristics.

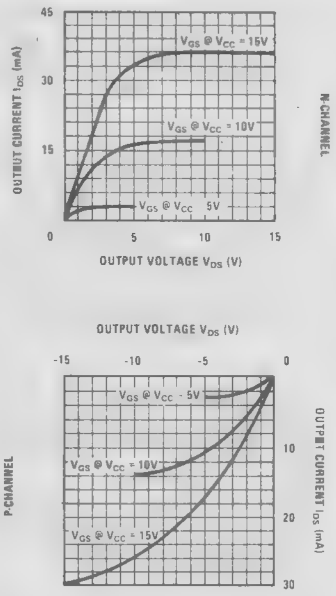


FIGURE 2-2. Logical "1" Output Voltage vs Source Current.

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 2-1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in Figure 2-3 have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system.

Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.

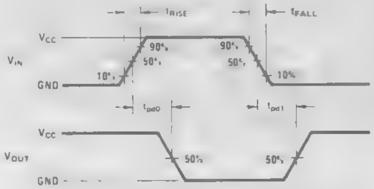
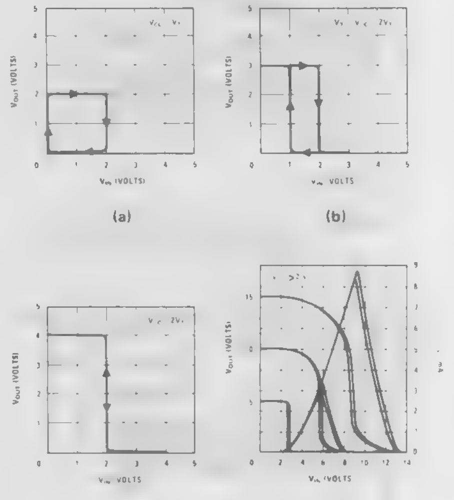


FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System.

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC}'s $> 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC}, the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidently, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

Let's look at the transfer characteristics, Figure 2-4, as they vary with V_{CC}. For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T, to be 2V. If V_{CC} is less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve Figure 2-4a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 2-4b), then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 2-4c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off (Figure 2-4d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them giving the rounded characteristic.



(a) (b)

(c) (d)

FIGURE 2-4. Transfer Characteristics vs V_{CC}.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 0.45 V_{CC} or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a 0.45 V_{CC} spurious pulse on the clock line would not cause the flop to change state.

National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within 0.1 V_{CC} volts of a proper logic level (V_{CC} or Ground), the input can be as much as 0.1 V_{CC} plus 1V away from power supply rail. Shown graphically we have:

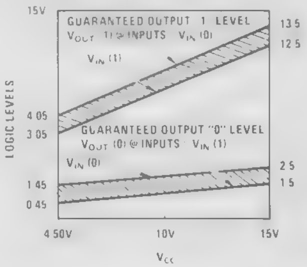


FIGURE 2-5. Guaranteed CMOS DC Margin Over Temperature as a Function of V_{CC}. CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.

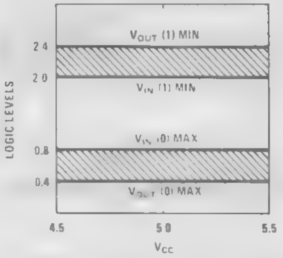


FIGURE 2-6. Guaranteed TTL DC Margin Over Temperature as a Function of V_{CC}. TTL Guarantees 0.4V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 2-4.

SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: simply stated, unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$), a floating input may drift back and forth between a "0" and "1" creating some very intriguing system problems. All unused inputs should be tied to V_{CC}, Ground or another used input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 3-1. Let inputs A & B be the unused inputs.

If we were going to tie the unused inputs to a logic level, inputs A & B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

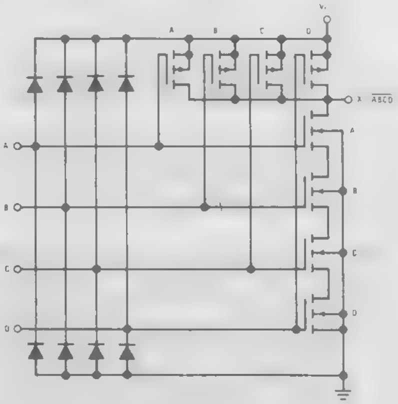


FIGURE 3-1. MM74C20 Four Input NAND Gate.

So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.

Parallel gates: depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in Figure 3-2. This insures that there are a number of parallel combinations of the series string of transistors (Figure 3-1), thereby increasing drive in that direction also.

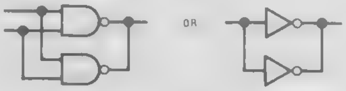
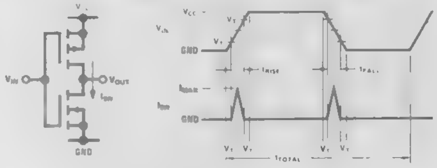


FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: there are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (part no. CD4016C). Second, over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: to minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) Figure 3-3.



VI POWER IS GIVEN BY·

$$P_{VI} = V_{CC} \times \frac{1}{2} I_{MAX} \times \text{RISE TIME TO PERIOD RATIO}$$

$$\text{RISE TIME TO PERIOD RATIO} = \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$$

$$\text{WHERE } \frac{1}{t_{TOTAL}} = \text{FREQUENCY}$$

$$P_{VI} = 1/2\,(V_{CC} - 2V_T)\, I_{CC\,MAX}\,(t_{RISE} + t_{FALL})\,\text{FREQ}$$

FIGURE 3-3. DC Transient Power.

The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See Figure 2-4d.

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the

were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at 1/2 V_{CC}. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** the CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: there are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17 to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

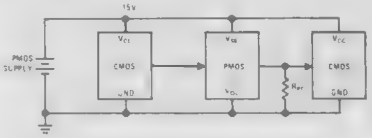
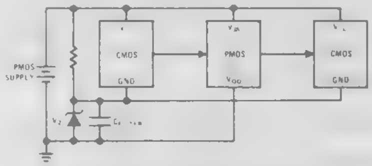


FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS.

First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, Figure 3-4.

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, Figure 3-5.

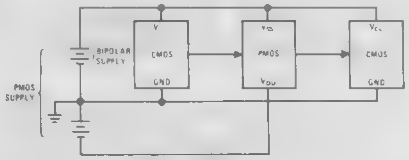


Use a bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where The P-MOS Supply is Greater Than 15V.

In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply and it interfaces directly to P-MOS, Figure 3-6.

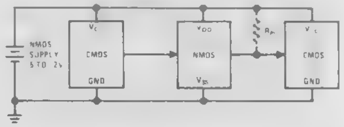


Run the CMOS from the bipolar supply and interface directly to P-MOS

FIGURE 3-6. A System With CMOS, P-MOS and Bipolar Logic.

N-Channel MOS: interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower power supply rail to about 1 to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output level will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in Figure 3-7.



Both operate off same supply with pull up resistors optional from N MOS to CMOS

FIGURE 3-7. A System With CMOS and N-MOS Only.

TTL, LPTTL, DTL: two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

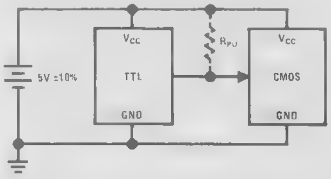
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the mil temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the mil temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in Figure 2-5, if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400μA. This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable (V_{CC} = 4.5V).

Under nominal conditions (25°C, V_{IN} = 0.4V, nominal leakage currents into CMOS and V_{CC} = 5V) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times −2mV per °C, or −4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



Pull up resistor, R_{PU}, is needed only at the lower end of the Mil temperature range

FIGURE 3-8. TTL to CMOS Interface.

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360μA (about 420μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in Figure 3-9.

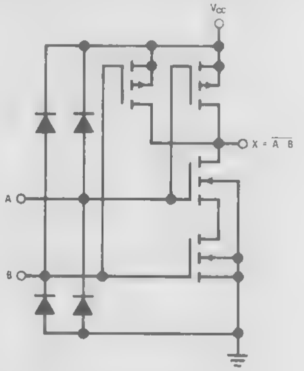


FIGURE 3-9a. MM74C00.

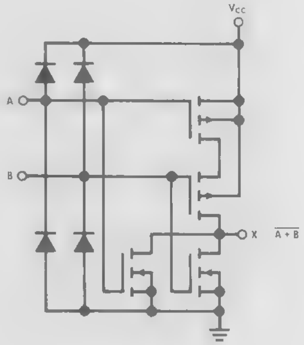


FIGURE 3-9b. MM74C02.

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360μA, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560μA over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about 800μA. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02

TIMING CONSIDERATIONS IN CMOS MSIs

There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

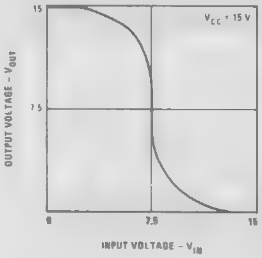


FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

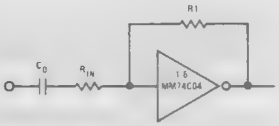


FIGURE 2. A 74CMOS Invertor Biased for Linear Mode Operation.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

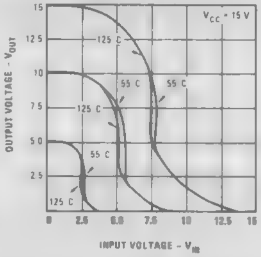


FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

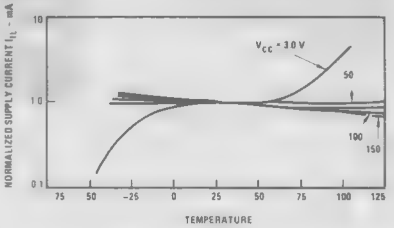


FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

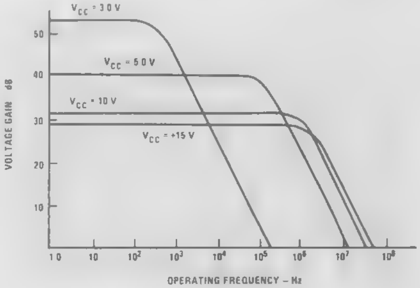


FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.

APPLICATIONS

Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

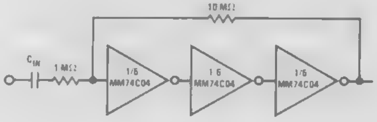


FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.

Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

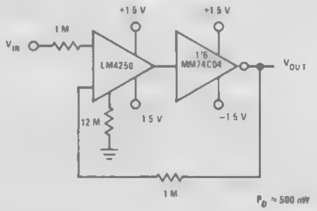


FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

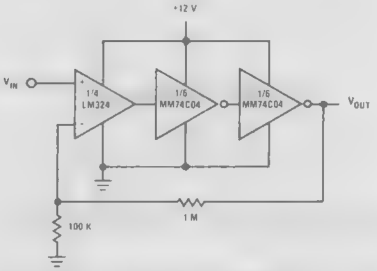


FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA from the V_{CC} supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

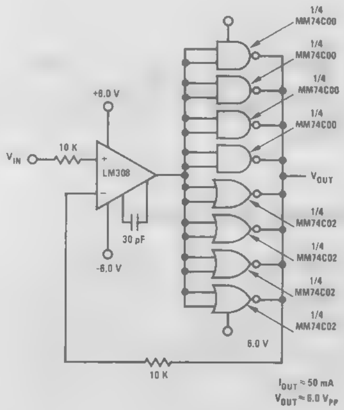


FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive.

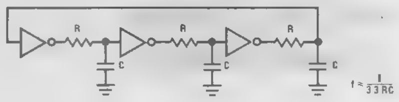
Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

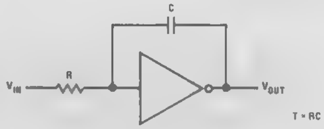
Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

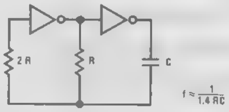
Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.



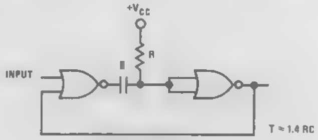
Phase Shift Oscillator Using MM74C04



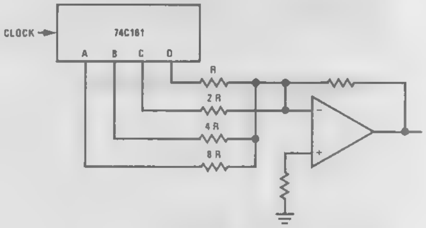
Integrator Using Any Inverting CMOS Gate



Square Wave Oscillator



One Shot



Staircase Generator

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.

54C/74C Family Characteristics

National Semiconductor
Application Note 90
Thomas P. Redfern

INTRODUCTION

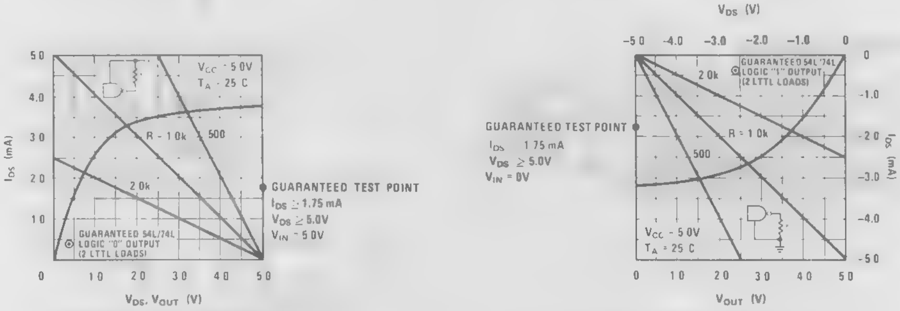
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

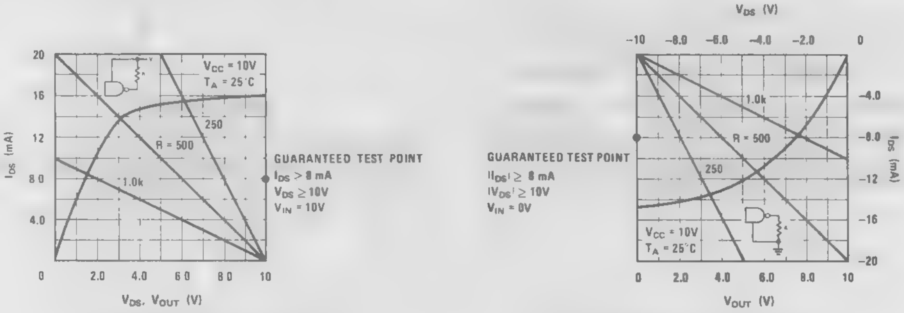
Figure 1 and Figure 2 show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to application note AN-77, "CMOS, The Ideal Logic Family." Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.



(A) Typical Output Sink Characteristic (N-Channel)

(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1



(A) Typical Output Sink Characteristic (N-Channel)

(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2

V_{CC} - 5.0V	V_{IN} = 5.0V $I_{DS} \geq 1.75$ mA $V_{DS} \geq 5.0$V	V_{IN} = 0V $\lvert I_{DS}\rvert \geq 1.75$ mA $\lvert V_{DS}\rvert \geq 5.0$V
V_{CC} - 10V	V_{IN} = 10V $I_{DS} \geq 8.0$ mA $V_{DS} \geq 10$V	V_{IN} = 0V $\lvert I_{DS}\rvert \geq 8.0$ mA $\lvert V_{DS}\rvert \geq 10$V

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. Figures 1 and 2 show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at V_{CC} = 5.0V, V_{OUT} = 1.5V (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at V_{CC} = 5.0V.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the I_{DS} = 0 axis and the output will then typically switch to either V_{CC} or ground.

NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

The transfer characteristic of Figure 3 shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.

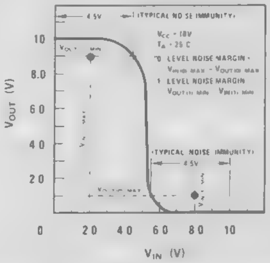


FIGURE 3. Typical Transfer Characteristic

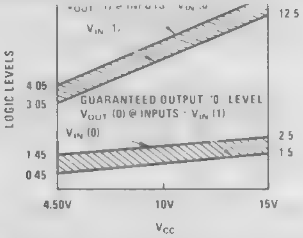


FIGURE 4. Guaranteed Noise Margin Over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. Figure 5 indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.

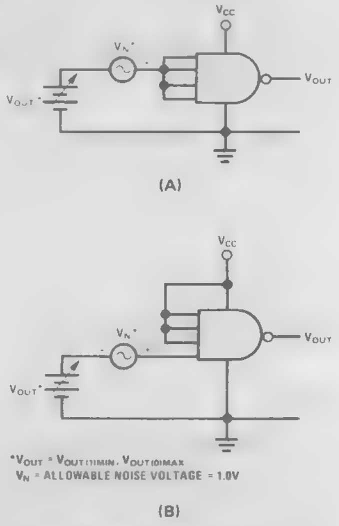

V_{CC}
V_N*
V_{OUT}
V_{OUT}*
(A)
V_{CC}
V_N*
V_{OUT}
V_{OUT}*
*V_{OUT} = $V_{OUT(1)MIN}$, $V_{OUT(0)MAX}$
V_N = ALLOWABLE NOISE VOLTAGE = 1.0V
(B)

FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in Figure 5.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current (2) transient power due to load capacitance (3) transient power due to internal capacitance and (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is $1/2\ CV^2$. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then $2\ [(1/2)\ CV_{CC}{}^2] = CV_{CC}{}^2$. Energy per unit time, or power, is then $CV_{CC}{}^2\ f$, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in application note AN-77. The expression is:

$$P_{VI} = \frac{1}{2}\ (V_{CC} - 2\ V_T)\ I_{CC\,MAX}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

$$\text{Power (no load)} = C_{PD}\ V_{CC}{}^2\ f$$

The total power consumption is then simplified to:

$$\text{Total Power} = (C_{PD} + C_L)\ V_{CC}{}^2\ f + I_{LEAK}\ V_{CC} \quad (1)$$

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further Figure 6 gives a graph of normalized power vs frequency for different power supply voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.

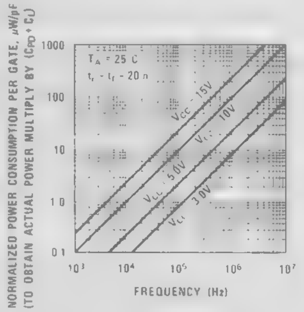


FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\mu\text{W}}{\text{pF}} \times (12\ \text{pF} + 50\ \text{pF}) = \frac{0.62\ \text{mW}}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ \text{mW} + 0.01\mu\text{A} \times 10\text{V} \cong 2.48\ \text{mW}$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}{}^2\ f$. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even through the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD}\,V_{CC}^2\,f}_{\substack{\text{no load}\\ \text{power}}} + \underbrace{C_L\,V_{CC}^2\,\frac{f}{2}}_{\substack{\text{output}\\ \text{power of}\\ \text{1st stage}}} + \underbrace{C_L\,V_{CC}^2\,\frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L\,V_{CC}^2\,\frac{f}{8}}_{\text{3rd stage}} + \underbrace{2\,C_L\,V_{CC}^2\,\frac{f}{16}}_{\substack{\text{4th stage}\\ \text{\& carry}\\ \text{output}}} + \underbrace{I_L\,V_{CC}}_{\substack{\text{leakage}\\ \text{term}}}$$

This reduces to:

$$P_{TOTAL} = (C_{PD} + C_L)\,V_{CC}^2\,f + I_L\,V_{CC}$$

From the data sheet $C_{PD} = 90$ pF and $I_L = 0.05\mu$A. Using Figure 6 total power is then:

$$P_{TOTAL} = (90\text{ pF} + 50\text{ pF}) \times \frac{100\mu\text{W}}{\text{pF}} + 0.05 \times 10^{-6}$$
$$\times\ 10\text{V} \cong 14\text{ mW}$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of Figure 6 and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF *and input rise and fall times of 20 ns.* A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem Figure 7 has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

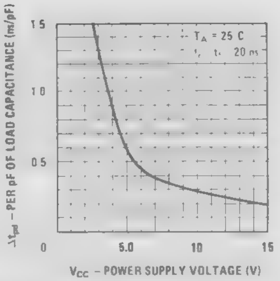


FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

$$t_{pd}\Big|_{C_L = C} = (C - 50)\text{ pF} \times \frac{\Delta t_{pd}}{\text{pF}} + t_{pd}\Big|_{C_L = 50\text{ pF}}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50\text{ pF}}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\dfrac{\Delta t_{pd}}{\text{pF}}$ = Value obtained from Figure 7.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15\text{ pF}} = (15 - 50)\text{ pF} \times 0.57\,\frac{\text{ns}}{\text{pF}} + 50\text{ ns}$$

$$= -20\text{ ns} + 50\text{ ns} = 30\text{ ns}$$

The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100\text{ pF}} = (100 - 50)\ 0.29\text{ ns} + 70\text{ ns}$$

$$= 14.5 + 70 \cong 85\text{ ns}$$

It is significant to note that this equation and Figure 7 apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller Δt_{pd}/pF.

Another point to consider in the design of a CMOS system is the affect of power supply voltage on propagation delay. Figure 8 shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.

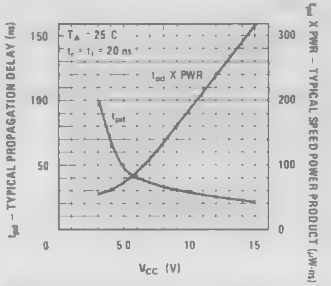


FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

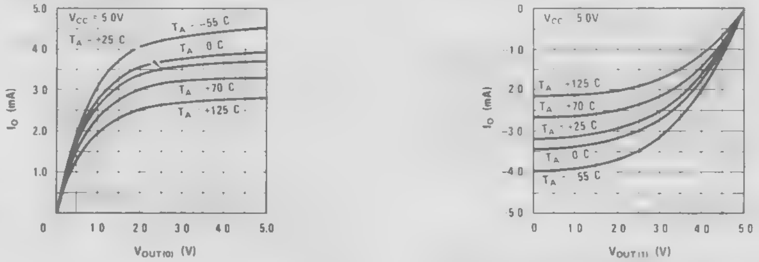
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out." Going from *V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%.* Clearly for V_{CC} > 10V a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However in general it can be seen from Figure 8 that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

TEMPERATURE CHARACTERISTICS

Figures 9 and 10 give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The affect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

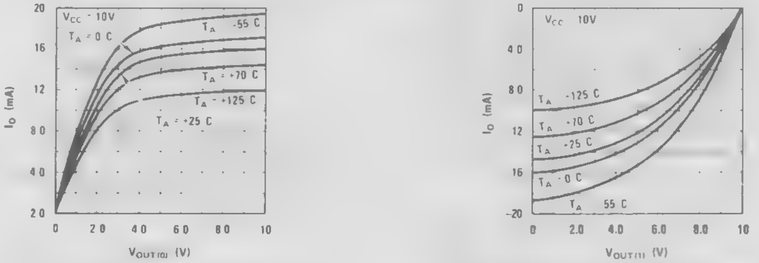
Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependance of t_{pd} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.



(A) Typical Output Drain Characteristic (N-Channel)

(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9



(A) Typical Output Drain Characteristic (N-Channel)

(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10

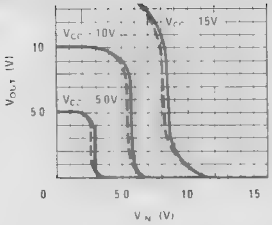


FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of Figure 9 and 10 show considerable variation with temperature. Examination of the transfer characteristics of Figure 11

dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independance of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

CMOS OSCILLATORS — AN-118

CMOS Oscillators

National Semiconductor
Application Note 118
Mike Watts

INTRODUCTION

This note describes several square wave oscillators that can be built using CMOS logic elements. These circuits offer the following advantages:

- Guaranteed startability
- Relatively good stability with respect to power supply variations
- Operation over a wide supply voltage range (3V to 15V)
- Operation over a wide frequency range from less than 1 Hz to about 15 MHz
- Low power consumption (see AN-90)
- Easy interface to other logic families and elements including TTL

Several RC oscillators and two crystal controlled oscillators are described. The stability of the RC oscillator will be sufficient for the bulk of applications; however, some applications will probably require the stability of a crystal. Some applications that require a lot of stability are:

1. Timekeeping over a long interval. A good deal of stability is required to duplicate the performance of an ordinary wrist watch (about 12 ppm). This is, of course, obtainable with a crystal. However, if the time interval is short and/or the resolution of the timekeeping device is relatively large, an RC oscillator may be adequate. For example: if a stopwatch is built with a resolution of tenths of seconds and the longest interval of interest is two minutes, then an accuracy of 1 part in 1200 (2 minutes x 60 seconds/minute x 10 tenth/second) may be acceptable since any error is less than the resolution of the device.

2. When logic elements are operated near their specified limits. It may be necessary to maintain clock frequency accuracy within very tight limits in order to avoid exceeding the limits of the logic family being used, or in which the timing relationships of clock signals in dynamic MOS memory or shift register systems must be preserved.

3. Baud rate generators for communications equipment.

4. Any system that must interface with other tightly specified systems. Particularly those that use a "handshake" technique in which Request or Acknowledge pulses must be of specific widths.

LOGICAL OSCILLATORS

Before describing any specific circuits, a few words about logical oscillators may clear up some recurring confusion.

Any odd number of inverting logic gates will oscillate if they are tied together in a ring as shown in *Figure 1*. Many beginning logic designers have discovered this (to their chagrin) by inadvertently providing such a path in their designs. However, some people are confused by the circuit in *Figure 1* because they are accustomed to seeing sinewave oscillators implemented with positive feedback, or amplifiers with non-inverting gain. Since the concept of phase shift becomes a little strained when the inverters remain in their linear region for such a short period, it is far more straightforward to analyze the circuit from the standpoint of ideal switches with finite propagation delays rather than as amplifiers with 180° phase shift. It then becomes obvious that a "1" chases itself around the ring and the network oscillates.

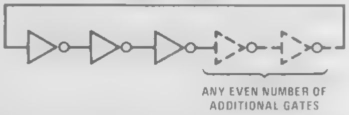


FIGURE 1. Odd Number of Inverters will Always Oscillate

The frequency of oscillation will be determined by the total propagation delay through the ring and is given by the following equation.

$$f = \frac{1}{2nTp}$$

Where:

f = frequency of oscillation
Tp = Propagation delay per gate
n = number of gates

This is not a practical oscillator, of course, but it does illustrate the maximum frequency at which such an oscillator will run. All that must be done to make this a useful oscillator is to slow it down to the desired frequency. Methods of doing this are described later.

To determine the frequency of oscillation, it is necessary to examine the propagation delay of the inverters. CMOS propagation delay depends on supply voltage and load capacitance. Several curves for propagation delay for National's 74C line of CMOS gates are reproduced in *Figure 2.* From these, the natural frequency of oscillation of an odd number of gates can be determined.

An example may be instructive.

Assume the supply voltage is 10V. Since only one input is driven by each inverter, the load capacitance on each inverter is at most about 8 pF. Examine the curve in *Figure 2c* that is drawn for V_{CC} = 10V and extrapolate it down to 8 pF. We see that the curve predicts a propagation delay of about 17 ns. We can then calculate the frequency of oscillation for three inverters using the expression mentioned above. Thus:

$$f = \frac{1}{2 \times 3 \times 17 \times 10^{-9}} = 9.8 \text{ MHz}$$

Lab work indicates this is low and that something closer to 16 MHz can be expected. This reflects the conservative nature of the curves in *Figure 2.*

Since this frequency is directly controlled by propagation delays, it will vary a great deal with temperature, supply voltage, and any external loading, as indicated by the graphs in *Figure 2.* In order to build a usefully stable oscillator it is necessary to add passive elements that determine oscillation frequency and minimize the effect of CMOS characteristics.

STABLE RC OSCILLATOR

Figure 3 illustrates a useful oscillator made with three inverters. Actually, any inverting CMOS gate or combination of gates could be used. This means left over portions of gate packages can be often used. The duty cycle will be close to 50% and will oscillate at a frequency that is given by the following expression.

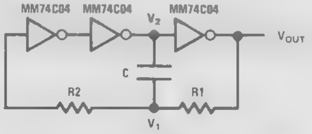


FIGURE 3. Three Gate Oscilaltor

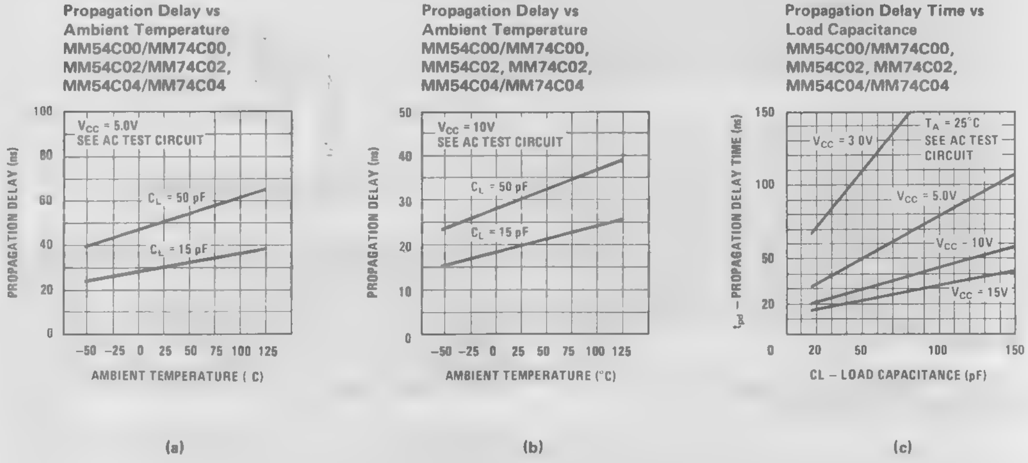
$$f \cong \frac{1}{2\,R1\,C\left(\frac{0.405\,R2}{R1 + R2} + 0.693\right)}$$

Another form of this expression is:

$$f \cong \frac{1}{2C\,(0.405\,R_{eq} + 0.693\,R1)}$$

Where:

$$R_{eq} = \frac{R1\,R2}{R1 + R2}$$



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02, MM74C02, MM54C04/MM74C04

Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02, MM74C02, MM54C04/MM74C04

(a) (b) (c)

FIGURE 2. Propagation Delay for 74C Gates

The following three special cases may be useful.

If $R1 = R2 = R$ $\quad f \cong \dfrac{0.559}{RC}$

If $R2 >\!>\!> R1$ $\quad f \cong \dfrac{0.455}{RC}$

If $R2 <\!<\!< R1$ $\quad f \cong \dfrac{0.722}{RC}$

Figure 4 illustrates the approximate output waveform and the voltage V_1 at the charging node.

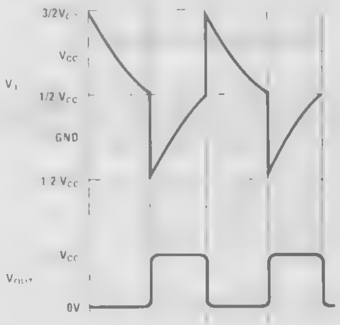


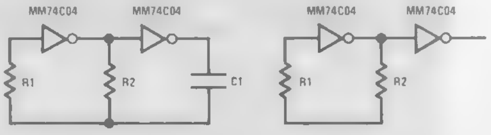
FIGURE 4. Waveforms for Oscillator in Figure 3

Note that the voltage V_2 will be clamped by input diodes when V_1 is greater than V_{CC} or more negative than ground. During this portion of the cycle current will flow through R2. At all other times the only current through R2 is a very minimal leakage term. Note also that as soon as V_1 passes through threshold (about 50% of supply) and the input to the last inverter begins to change, V_1 will also change in a direction that reinforces the switching action; i.e., providing positive feedback. This further enhances the stability and predictability of the network.

This oscillator is fairly insensitive to power supply variations due largely to the threshold tracking close to 50% of the supply voltage. Just how stable it is will be determined by the frequency of oscillation; the lower the frequency the more stability and vice versa. This is because propagation delay and the effect of threshold shifts comprise a smaller portion of the overall period. Stability will also be enhanced if R1 is made large enough to swamp any variations in the CMOS output resistance.

TWO GATE OSCILLATOR WILL NOT NECESSARILY OSCILLATE

A popular oscillator is shown in *Figure 5a.* The only undesirable feature of this oscillator is that it may not oscillate. This is readily demonstrated by letting the value of C go to zero. The network then degenerates into *Figure 5b,* which obviously will not oscillate. This illustrates that there is some value of C1 that will not force the network to oscillate. The real difference between this two gate oscillator and the three gate oscillator is that the former must be forced to oscillate by the capacitor while the three gate network will always oscillate willingly and is simply slowed down by the capacitor. The three gate network will always oscillate, regardless of the value of C1 but the two gate oscillator will not oscillate when C1 is small.



(a) (b)

FIGURE 5. Less Than Perfect Oscillator

The only advantage the two gate oscillator has over the three gate oscillator is that it uses one less inverter. This may or may not be a real concern, depending on the gate count in each user's specific application. However, the next section offers a real minimum parts count oscillator.

A SINGLE SCHMITT TRIGGER MAKES AN OSCILLATOR

Figure 6 illustrates an oscillator made from a single Schmitt trigger. Since the MM74C14 is a hex Schmitt trigger, this oscillator consumes only one sixth of a package. The remaining 5 gates can be used either as ordinary inverters like the MM74C04 or their Schmitt trigger characteristics can be used to advantage in the normal manner. Assuming these five inverters can be used elsewhere in the system, *Figure 6* must represent the ultimate in low gate count oscillators.

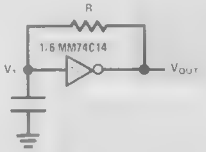


FIGURE 6. Schmitt Trigger Oscillator

Voltage V_1 is depicted in *Figure 7* and changes between the two thresholds of the Schmitt trigger. If these thresholds were constant percentages of V_{CC} over the supply voltage range, the oscillator would be insensitive to variations in V_{CC}. However, this is not the case. The thresholds of the Schmitt trigger vary enough to make the oscillator exhibit a good deal of sensitivity to V_{CC}.

Applications that do not require extreme stability or that have access to well regulated supplies should not be bothered by this sensitivity to V_{CC}. Variations in threshold can be expected to run as high as four or five percent when V_{CC} varies from 5V to 15V.

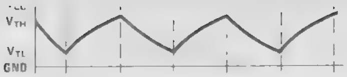


FIGURE 7. Waveforms for Schmitt Trigger Oscillator in Figure 6

A CMOS Crystal Oscillator

Figure 8 illustrates a crystal oscillator that uses only one CMOS inverter as the active element. Any odd number of inverters may be used, but the total propagation delay through the ring limits the highest frequency

CONCLUSIONS

A large number of oscillator applications can be implemented with the extremely simple, reliable, inexpensive and versatile CMOS oscillators described in this note. These oscillators consume very little power compared to most other approaches. Each of the oscillators requires less than one full package of CMOS inverters of the MM74C04 variety. Frequently such an oscillator can be built using leftover gates of the MM74C00, MM74C02, MM74C10 variety. Stability superior to that easily attainable with TTL oscillators is readily attained, particularly at lower frequencies. These oscillators are so versatile, easy to build, and inexpensive that they should find their way into many diverse designs.

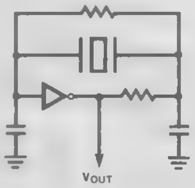


FIGURE 8. Crystal Oscillator

Using the CMOS Dual Monostable Multivibrator

National Semiconductor
Application Note 138
Thomas P. Redfern

INTRODUCTION

The MM54C221/MM74C221 is a dual CMOS monostable multivibrator. Each one-shot has three inputs (A, B and CLR) and two outputs (Q and $\bar{Q}$). The output pulse width is set by an external RC network.

The A and B inputs trigger an output pulse on a negative or positive input transition respectively. The CLR input when low resets the one-shot. Once triggered the A and B inputs have no further control on the output.

THEORY OF OPERATION

Figure 1 shows that in its stable state, the one-shot clamps C_{EXT} to ground by turning N1 ON and holds the positive comparator input at V_{CC} by turning N2 OFF. The prefix N is used to denote N-channel transistors.

The signal, G, gating N2 OFF also gates the comparator OFF thereby keeping the internal power dissipation to an absolute minimum. The only power dissipation when in the stable state is that generated by the current through R_{EXT}. The bulk of this dissipation is in R_{EXT} since the voltage drop across N1 is very small for normal ranges of R_{EXT}.

To trigger the one-shot the CLR input must be high. The gating, G, on the comparator is designed such that the comparator output is high when the one-shot is in its stable state. With the CLR input high the clear input to FF is disabled allowing the flip-flop to respond to the A or B input. A negative transition on A or a positive transition on B sets Q to a high state. This in turn gates N1 OFF, and N2 and the comparator ON.

Gating N2 ON establishes a reference of 0.63 V_{CC} on the comparator's positive input. Since the voltage on C_{EXT} can not change instantaneously V1 = 0V at this time. The comparator then will maintain its one level on the output. Gating N1 OFF allows C_{EXT} to start charging through R_{EXT} toward V_{CC} exponentially.

Assuming a perfect comparator (zero offset and infinite gain) when the voltage on C_{EXT}, V1, equals 0.63 V_{CC} the comparator output will go from a high state to a low state resetting Q to a low state. *Figure 2* is a timing diagram summarizing this sequence of events.

This diagram is idealized by assuming zero rise and fall times and zero propagation delay but it shows the basic operation of the one-shot. Also shown is the effect of taking the CLR input low. Whenever CLR goes low FF

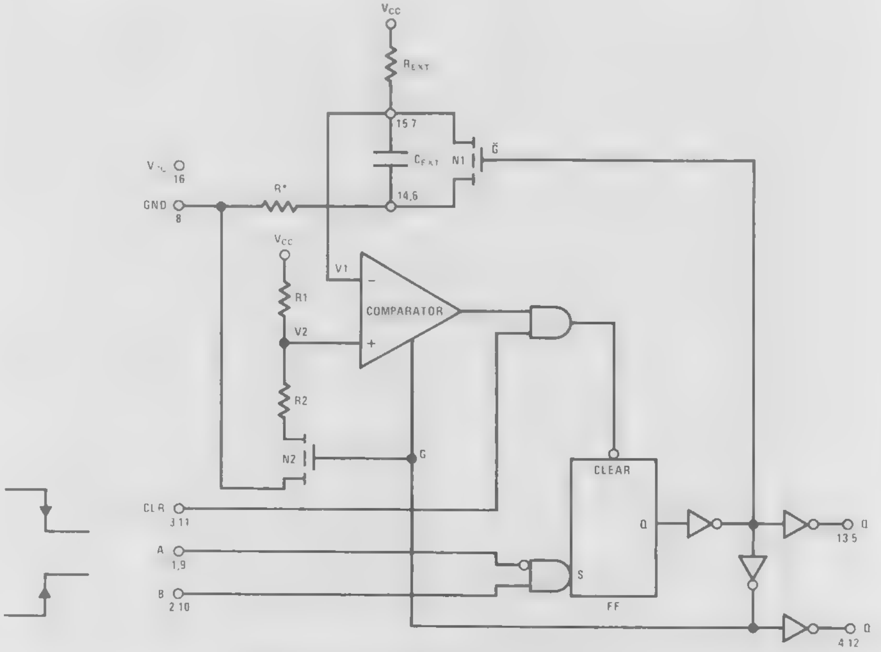


FIGURE 1. Monostable Multivibrator Logic Diagram

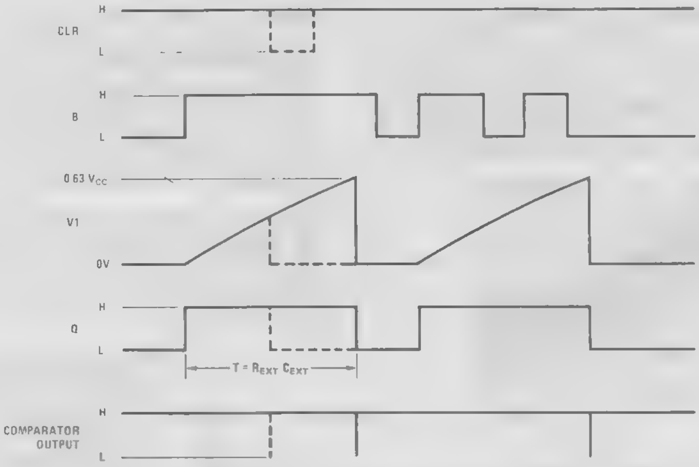


FIGURE 2. One-Shot Timing Diagram

is reset independent of all other inputs. *Figure 2* also shows that once triggered, the output is independent of any transitions on B (or A) until the cycle is complete.

The output pulse width is determined by the following equation:

$$V1 = V_{CC}\ (1 - e^{-T/R_{EXT}\,C_{EXT}}) = 0.63\ V_{CC} \qquad (1)$$

Solving for t gives:

$$T = R_{EXT}\ C_{EXT}\ \ln\ (1/0.37) = R_{EXT}\ C_{EXT} \qquad (2)$$

A word of caution should be given in regards to the ground connection of the external capacitor (C_{EXT}). It should always be connected as shown in *Figure 1* to pin 14 or 6 and never to pin 8. This is important because of the parasitic resistor R*. Because of the large discharge current through R*, if the capacitor is connected to pin 8, a four layer diode action can result causing the circuit to latch and possibly damage itself.

ACCURACY

There are many factors which influence the accuracy of the one-shot. The most important are:

a. Comparator input offset
b. Comparator gain
c. Comparator time delay
d. Voltage divider R1, R2
e. Delays in logic elements
f. ON impedance of N1 and N2
g. Leakage of N1
h. Leakage of C_{EXT}
i. Magnitude of R_{EXT} and C_{EXT}

The characteristics of C_{EXT} and R_{EXT} are, of course, not determined by the characteristics of the one-shot. In order to establish the accuracy of the one-shot, devices were tested using an external resistance of 10 kΩ and various capacitors. A resistance of 10 kΩ was chosen because the leakage and ON impedance of transistor N1 have a minimal effect on accuracy with this value of resistance.

Two values of C_{EXT} were chosen, 1000 pF and 0.1μF. These values give pulse widths of 10μs and 1000μs with R_{EXT} = 10 kΩ.

Figures 3 and 4 show the resulting distributions of pulse widths at 25°C for various power supply voltages. *Because propagation delays, at the same power supply voltage, are the same independent of pulse width, the shorter the pulse width the more the accuracy is*

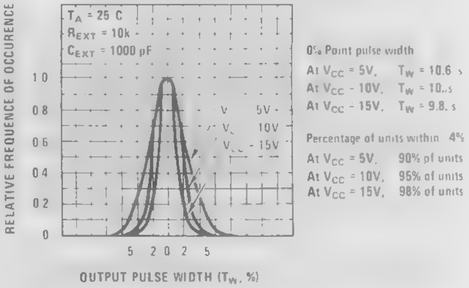


FIGURE 3. Typical Pulse Width Distribution for 10μs Pulse.

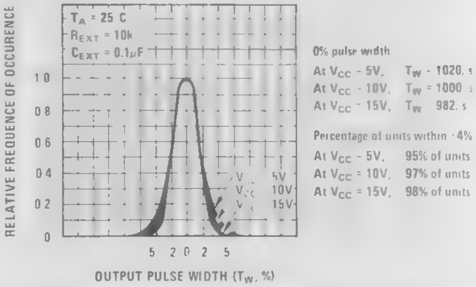


FIGURE 4. Typical Pulse Width Distribution for 1000μs Pulse.

affected by propagation delay. *Figures 3 and 4* clearly show this effect. As pointed out in application note AN-90, 54C/74C Family Characteristics, propagation delay is a function of V_{CC}. *Figure 3*, (Pulse Width = 10μs) shows much greater variation with V_{CC} than *Figure 4* (Pulse Width = 1000μs). This same information is shown in *Figures 5 and 6* in a different format. In these figures the percent deviation from the average pulse width at 10V V_{CC} is shown vs V_{CC}. In addition to the average value the 10% and 90% points are shown. These percentage points refer to the statistical distribution of pulse width error. As an example, at V_{CC} = 10V for 10μs pulse width, 90% of the devices have errors of less than +1.7% and 10% have errors less than −2.1%. In other words, 80% have errors between +1.7% and −2.1%.

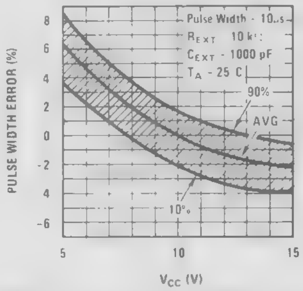


FIGURE 5. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 10μs).

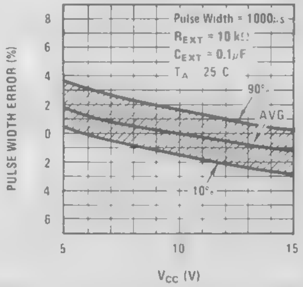


FIGURE 6. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 1000μs).

The minimum error can be obtained by operating at the maximum V_{CC}. A price must be paid for this and this price is, of course, increased power dissipation.

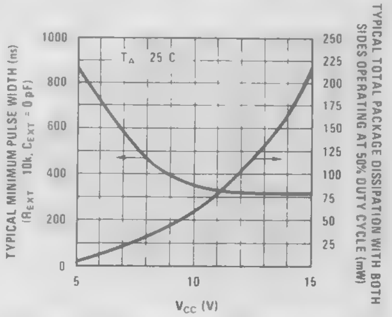


FIGURE 7. Typical Minimum Pulse Width and Power Dissipation vs V_{CC}.

Figure 7 shows typical power dissipation vs V_{CC} operating both sides of the one-shot at 50% duty cycle. Also shown in the same figure is typical minimum pulse width vs V_{CC}. The minimum pulse width is a strong function of internal propagation delays. *It is obvious from these two curves that increasing V_{CC} beyond 10V will not appreciably improve inaccuracy due to propagation delay but will greatly increase power dissipation.*

Accuracy is also a function of temperature. To determine the magnitude of its effects the one-shot was tested at temperature with the external resistance and capacitance maintained at 25°C. The resulting variation is shown in *Figures 8 and 9.*

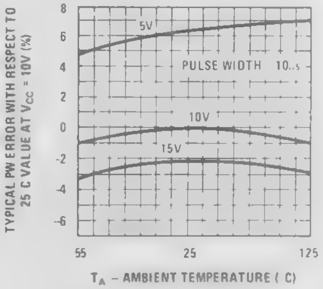


FIGURE 8. Typical Pulse Width Error vs Temperature (PW = 10μs).

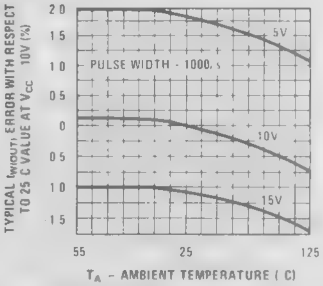


FIGURE 9. Typical Pulse Width Error vs Temperature (PW = 1000μs).

Up to this point the external timing resistor, R_{EXT}, has been held fixed at 10 kΩ. In actual applications other values may be necessary to achieve the desired pulse width. The question then arises as to what effect this will have on accuracy.

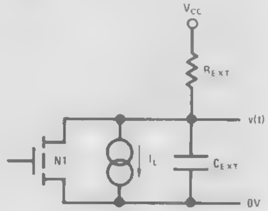


FIGURE 10.

As R_{EXT} becomes larger and larger the leakage current on transistor N1 becomes an ever increasing problem. The equivalent circuit for this leakage is shown in *Figure 10.*

Solving for t_L gives:

$$t_L = R_{EXT}\, C_{EXT}\, \ell n \left(\frac{V_{CC} - I_L\, R_{EXT}}{0.37\, V_{CC} - I_L\, R_{EXT}}\right) \qquad (3)$$

Using T as defined in Equation 2 the pulse width error is:

$$\text{PW Error} = \frac{t_L - T}{T} \times 100\%$$

Substituting Equations 2 and 3 gives:

$$\text{PW Error} = \frac{R_{EXT} C_{EXT}\, \ell n \left(\frac{V_{CC} - I_L R_{EXT}}{0.37\, V_{CC} - I_L R_{EXT}}\right) - R_{EXT} C_{EXT}\, \ell n (1/0.37)}{R_{EXT}\, C_{EXT}\, \ell n (1/0.37)}$$

PW Error is plotted in *Figure 11* for V_{CC} = 5, 10 and 15V. As expected, decreasing V_{CC} causes PW Error to increase with fixed I_L. Note that the leakage current, although here assumed to flow through N1, is general and could also be interpreted as leakage through C_{EXT}. See MM54C221/MM74C221 data sheet for leakage limits.

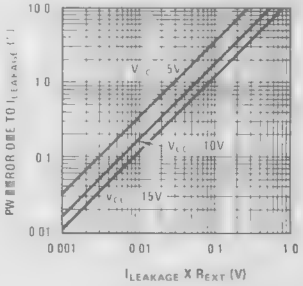


FIGURE 11. Percentage Pulse Width Error Due to Leakage.

To demonstrate the usefulness of *Figure 11* an example will be most helpful. Let us assume that N1 has a leakage of 250 x 10^{-9} amps, C_{EXT} has leakage of 150 x 10^{-9} amps, output pulse width = 0.1 seconds and V_{CC} = 5V. What R_{EXT} C_{EXT} should be used to guarantee an error due to leakage of less than 5%.

From *Figure 11* we see that to meet these conditions $R_{EXT}\, I_L < 0.14V$.

Then:

$$R_{EXT} < 0.14/(250 + 150) \times 10^{-9}$$

$$< 350\ k\Omega$$

Choosing standard component values of 250 kΩ and 0.004μF would satisfy the above conditions.

N1 becomes significant. The voltage across N1 is:

$$V_{N1} = V_{CC}\, r_{ON}/(R_{EXT} + r_{ON}) \qquad (4)$$

The output pulse width is defined by:

$$v\,(t_O) = (V_{CC} - V_{N1})\,(1 - e^{-t_O/R_{EXT}\,C_{EXT}}) + V_{N1} = 0.63\, V_{CC}$$

Solving for t_O gives:

$$t_O = R_{EXT}\, C_{EXT}\, \ell n \left(\frac{V_{CC} - V_{N1}}{0.37\, V_{CC}}\right)$$

Pulse Width Error is then:

$$\text{PW Error} = \frac{t_O - T}{T} \times 100\%$$

Substituting Equations 2 and 4 gives:

$$= \frac{R_{EXT}\, C_{EXT}\, \ell n \left(\frac{V_{CC} - V_{N1}}{0.37\, V_{CC}}\right) - R_{EXT}\, C_{EXT}\, \ell n (1/0.37)}{R_{EXT}\, C_{EXT}\, \ell n (1/0.37)}$$

This function is plotted in *Figure 12* for r_{ON} of 50Ω, 25Ω and 16.7Ω. These are the typical values of r_{ON} for a V_{CC} of 5V, 10V and 15V respectively.

As an example, assume that the pulse width error due to r_{ON} must be less than 0.5% operating at V_{CC} = 5V. The typical value of r_{ON} for V_{CC} = 5V is 50Ω. Referring to the 50Ω curve in *Figure 12*, R_{EXT} must be greater than 10 kΩ to maintain this accuracy. At V_{CC} = 10V, R_{EXT} must be greater than 5 kΩ as can be seen from the 25Ω curve in *Figure 12.*

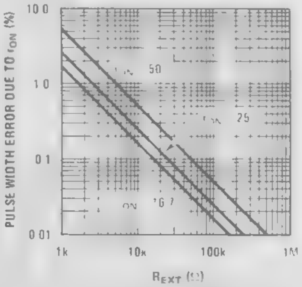
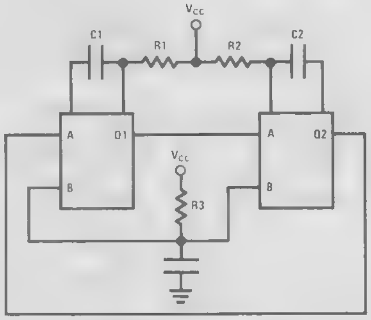


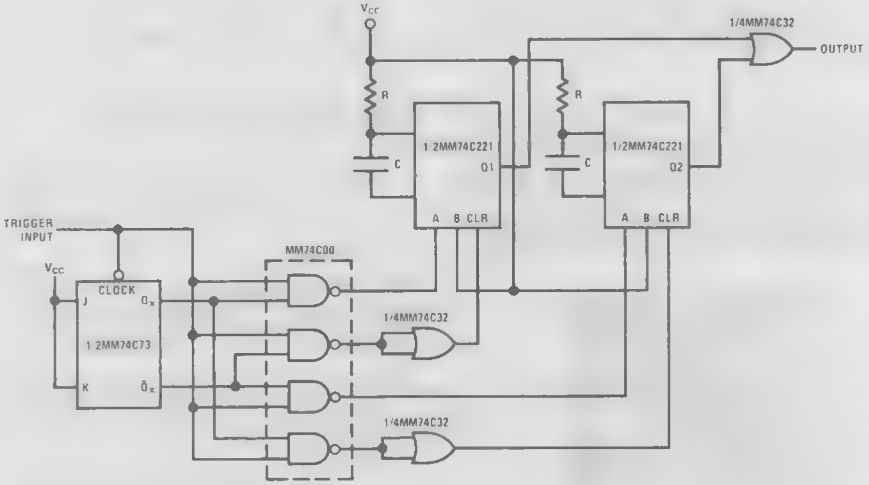
FIGURE 12. Percentage Pulse Width Error Due to Finite r_{ON} of Transistor N1 vs R_{EXT}.

Although clearly shown on the MM54C221/MM74C221 data sheet, it is worthwhile, for the sake of clarity, to point out that the parasitic capacitance between pins 7 (15) and 6 (14) is typically 15 pF. This capacitor is in parallel with C_{EXT} and must be taken into account when accuracy is critical.

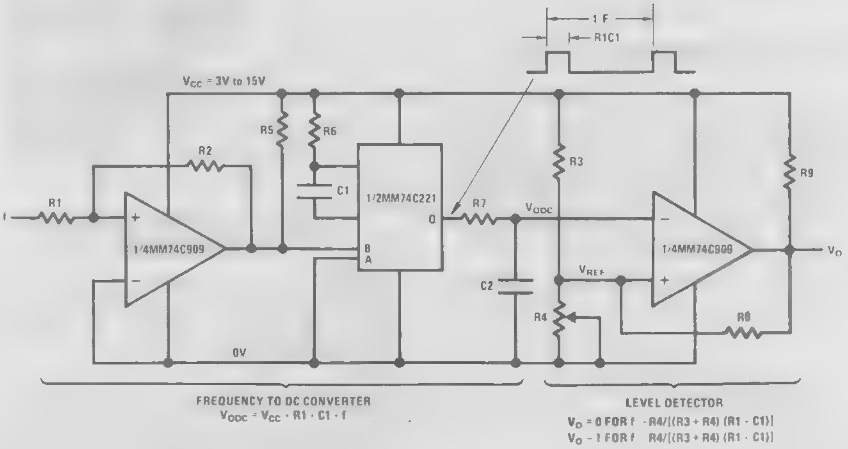
TYPICAL APPLICATIONS



Basic One-Shot Oscillator

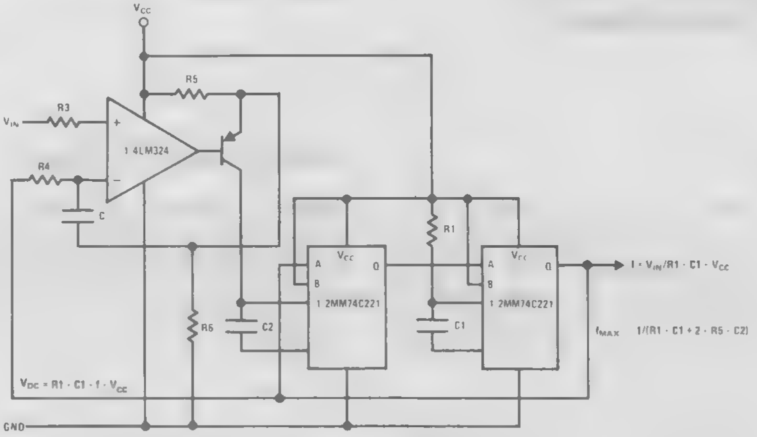


Retriggerable One-Shot


1 F
R1C1
V_{CC} = 3V to 15V
R5
R6
R2
C1
R1
f
+
−
1/4MM74C909
1/2MM74C221
B
A
Q
R7
V_{ODC}
R3
R9
C2
V_{REF}
R4
−
+
1/4MM74C909
V_O
R8
0V
FREQUENCY TO DC CONVERTER
V_{ODC} = V_{CC} · R1 · C1 · f
LEVEL DETECTOR
V_O = 0 FOR f - R4/[(R3 + R4) (R1 · C1)]
V_O - 1 FOR f R4/[(R3 + R4) (R1 · C1)]

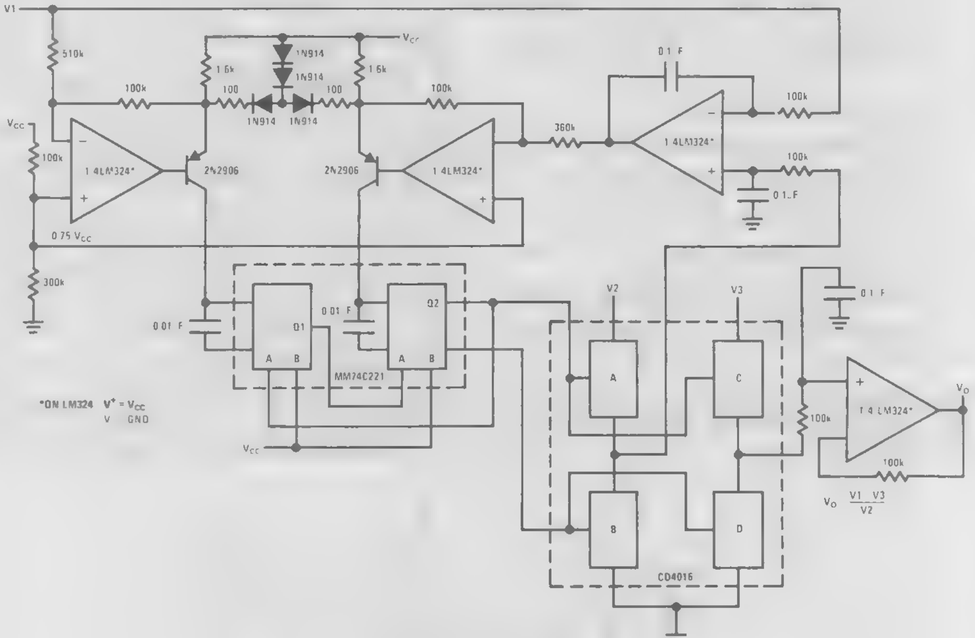
Frequency Magnitude Comparator

TYPICAL APPLICATIONS (Continued)



V_{CC}
R5
R3
V_{IN}
1/4 LM324
R4
C
R1
V_{CC}
A
B
Q
1/2 MM74C221
R6
C2
C1
$f = V_{IN}/R1 \cdot C1 \cdot V_{CC}$
$f_{MAX} = 1/(R1 \cdot C1 + 2 \cdot R5 \cdot C2)$
$V_{DC} = R1 \cdot C1 \cdot f \cdot V_{CC}$
GND

Linear VCO



Analog Multiplier/Divider

CMOS Schmitt Trigger —a Uniquely Versatile Design Component

National Semiconductor
Application Note 140
Gerald Buurma

INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
    - Thresholds are typically symmetrical to 1/2 V_{CC}
    - Outputs source and sink equal currents
    - Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC}-V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above 1/2 V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold is reached.

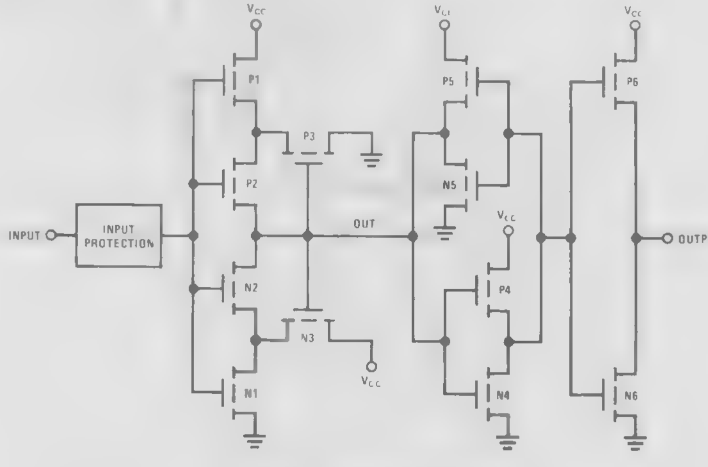


FIGURE 1. CMOS Schmitt Trigger

The typical transfer characteristics are shown in *Figure 2*; the guaranteed trip point range is shown in *Figure 3*.

WHAT HYSTERESIS CAN DO FOR YOUR

Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at V_{CC} = 10V there is the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is doen to prevent slicing level distortion. If a 4μs wide signal is sent down a transmission line a 4μs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4μs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.

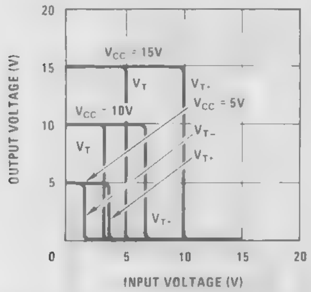


FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages.

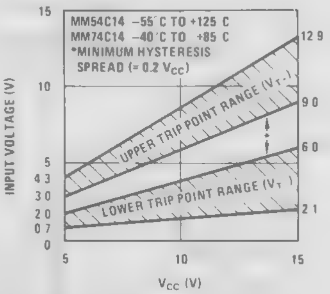
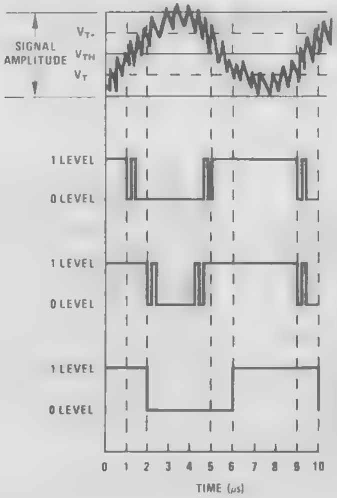


FIGURE 3. Guaranteed Trip Point Range.



a) Received signal from transmission line with thresholds at different amplitudes.

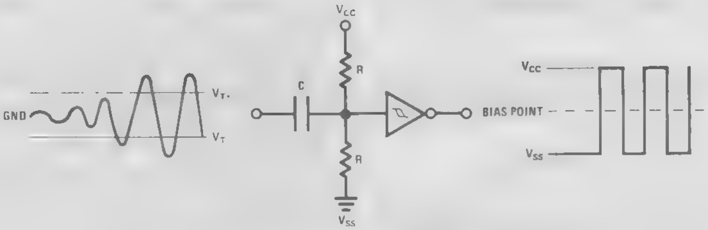
b) Recovered signal from comparator with threshold V_{TH} has multiple transitions

c) Recovered signal from comparator with positive offset on threshold, V_{T+}, positive pulse shorten, negative pulse lengthen

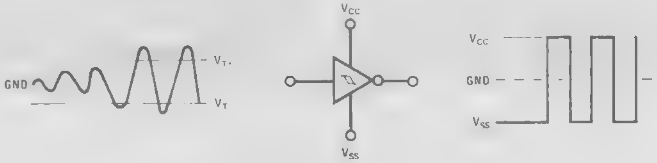
d) Recovered signal with CMOS Schmitt trigger, V_{T+} and V_{T-}. Restores true waveform

Recovered signal from Schmitt is same width as comparator with threshold at V_{TH}, and is only delayed in time.

FIGURE 4. CMOS Schmitt Trigger Ignores Noise

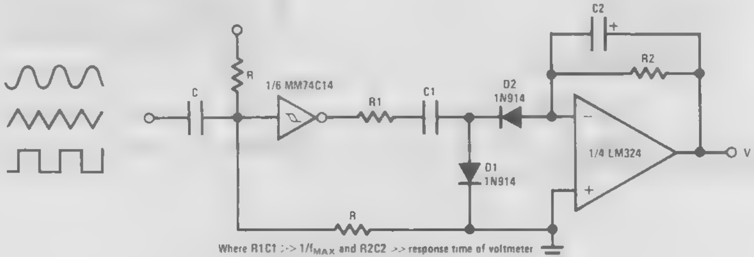


a) Capacitor impedance at lowest operating frequency should be much less than R R 1 2 R



b) By using split supply (±1 5 to ±7.5) direct interface is achieved.

FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection.



Where R1C1 >> $1/f_{MAX}$ and R2C2 >> response time of voltmeter
$V_{OUT} = fR2C1\Delta V$ where $\Delta V = V_{CC}$.

FIGURE 6. Diode Dump Tach Accepts any Input Waveform.

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a $10^{12}\Omega$ typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 >> t_{pd0} + t_{pd1}$.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

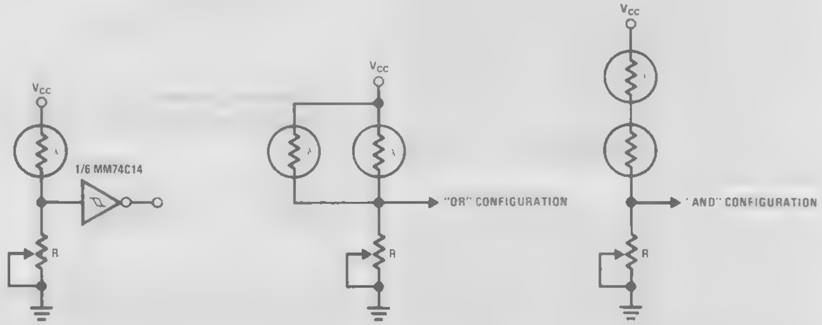
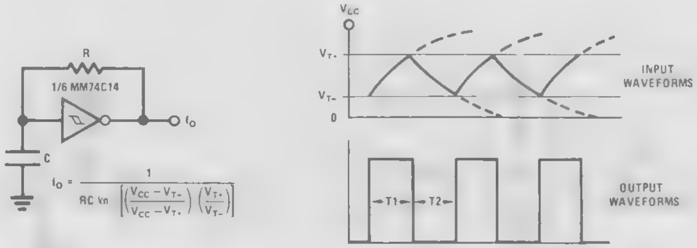
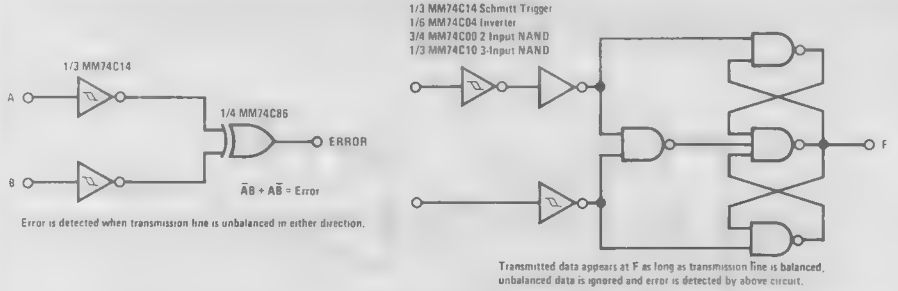


FIGURE 7. Light Activated Switch couldn't be Simpler. The Input Voltage Rises as Light Intensity Increases, when V_{T+} is Reached, the Output will go Low and Remain Low until the Intensity is Reduced Significantly.



$$f_O = \frac{1}{RC \ln \left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into Six Low Power Oscillators. Balanced Input and Output Characteristics give the Output Frequency a Typically 50% Duty Cycle.



Error is detected when transmission line is unbalanced in either direction.

Transmitted data appears at F as long as transmission line is balanced, unbalanced data is ignored and error is detected by above circuit.

a) Differential Error Detector.

b) Differential Line Receiver.

Truth Table

A	B	F
0	0	NC
0	1	0
1	0	1
1	1	NC

NC = No Change

FIGURE 9. Increase Noise Immunity by using the CMOS Schmitt Trigger to Demodulate a Balanced Transmission Line.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} +0.3V and ground −0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 5b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

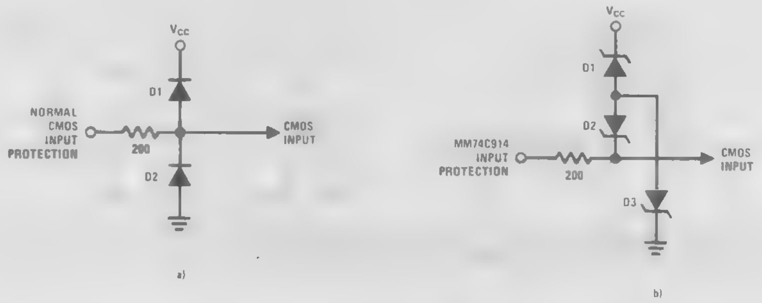
CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_s and speeding up capacitor C_s. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})\ R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to V_{IN} So,

$$\frac{d\,f_O}{d\,V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\ RC},$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN} is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.



a)

b)

FIGURE 10. Input Protection Diodes, in a) Normally Limit the Input Voltage Swing to 0.3V above V_{CC} and 0.3V below Ground. In b) D2 or D1 is Reverse Biased Allowing Input Swings of 25V above Ground or 25V below V_{CC}.

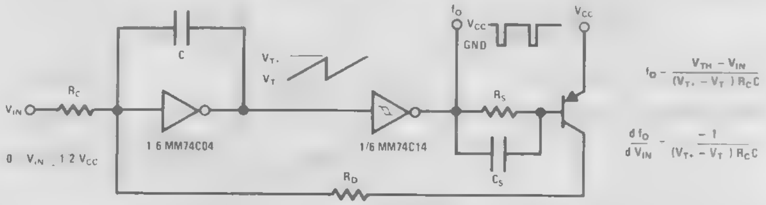

C
V_{T+}
V_T
R_C
V_{IN}
1 6 MM74C04
0 V_{IN} 1 2 V_{CC}
1/6 MM74C14
f_O
V_{CC}
GND
V_{CC}
R_S
C_S
R_D
f_O = (V_{TH} − V_{IN}) / (V_{T+} − V_T) R_CC
d f_O / d V_{IN} = − 1 / (V_{T+} − V_T) R_CC

FIGURE 11. Linear CMOS (Voltage Controlled Oscillator)

input to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{\text{SINK INVERTER}} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+}, the Schmitt output will go low sometime after the input pulse has gone low.

part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non 5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.

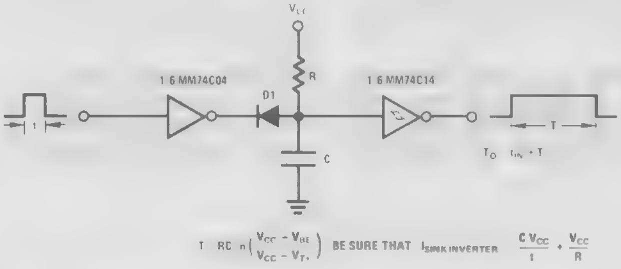

V_CC
R
1 6 MM74C04
D1
1 6 MM74C14
t
T
C
T_O t_IN + T
T RC n((V_CC − V_BE)/(V_CC − V_T+)) BE SURE THAT I_SINK INVERTER C V_CC/t + V_CC/R

FIGURE 12. Pulse Stretcher. A CMOS Inverter Discharges a Capacitor, a Blocking Diode allows Charging through R only. Schmitt Trigger Output goes Low after the RC Delay.

Designing with MM74C908, MM74C918 Dual High Voltage CMOS Drivers

National Semiconductor
Application Note 177
Jen-yen Huang

INTRODUCTION

By combining the merits of both CMOS and bipolar technologies on a single silicon chip, the MM74C908, MM74C918 provides the following distinguished features as general purpose high voltage drivers.

- Wide supply voltage range (3V to 18V)
- High noise immunity (typ 0.45 V_{CC})
- High input impedance (typ $10^{12}\Omega$)
- Extremely low standby power consumption (typ 750 nW at 15V)
- Low output "ON" resistance (typ 8Ω)
- High output drive capability ($I_{OUT} \geq 250$ mA at $V_{OUT} = V_{CC} - 3V$, and $T_j = 65°C$)
- High output "OFF" voltage

Among these, the first 4 are typical and unique characteristics of CMOS technology which are fully utilized in this circuit to achieve all the design advantages in a typical CMOS system.

The high output currents and low "ON" resistance are achieved through the use of an NPN Darlington pair at the output stage.

The MM74C908 is housed in an 8-lead epoxy dual-in-line package, which can dissipate at least 1.14W. The higher power version, MM74C918, comes in a 14-lead epoxy dual-in-line package, with power capability up to a minimum of 2.27W.

The circuitry for each of the 2 identical sections is shown in *Figure 1*.

With both inputs sitting at logical "1" level, the output of the inverter is also at logical "1", which prevents the P-channel transistor from being turned "ON"; therefore, the output is in its "OFF" state. Only a small amount of leakage current can flow.

On the other hand, when one or both of the inputs is at logical "0" level, the output of the inverter is also at logical "0", which turns on the P-channel transistor and, hence, the Darlington pair.

POWER CONSIDERATION

To assure junction temperature of 150°C or less, the on-chip power consumption must be limited to within the power handling capability of the packages. In *Figure 2*, the maximum power dissipation on-chip is shown as a function of ambient temperature for both MM74C908 and MM74C918. These curves are generated from (1) at $T_j = T_{j(MAX)} = 150°C$.

$$T_j = T_A + P_D\,\theta_{jA} \tag{1}$$

where T_j = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{jA} = thermal resistance between junction and ambient

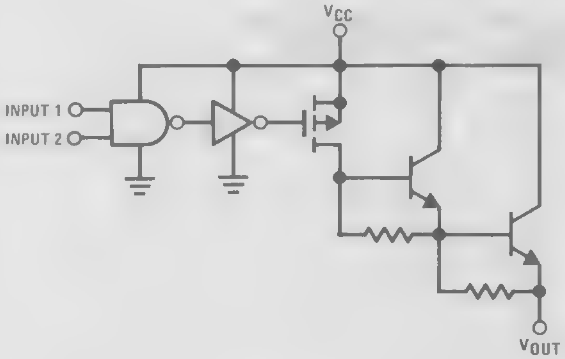


FIGURE 1

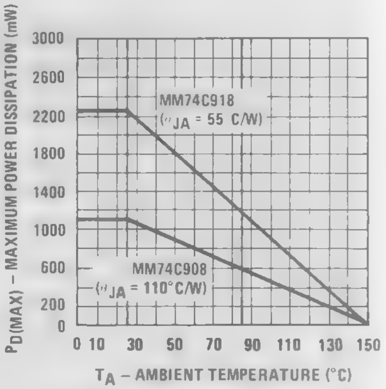


FIGURE 2. Maximum Power Dissipation vs Ambient Temperature

A general application circuit for the MM74C908, MM74C918 is as shown in *Figure 3*.

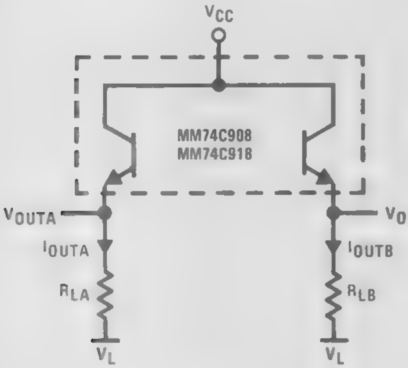


FIGURE 3

For both sections A and B;

$$I_{OUT} = \frac{V_{CC} - V_L}{R_{ON} + R_L} \qquad (2)$$

The device "ON" resistance, R_{ON}, is a function of junction temperature, T_j. The worst-case R_{ON} as a function of T_j is given in (3).

$$R_{ON} = 9\,[1 + 0.008\,(T_j - 25)] \qquad (3)$$

The total power dissipation in the device also consists of normal CMOS power terms (due to leakage current, internal capacitance, switching etc.) which are insignificant compared to the power dissipated at the output stages. Thus, the output power term defines the allowable limits of operation and is given by:

$$\begin{aligned} P_D &= P_{DA} + P_{DB} \\ &= I^2_{OUTA} \cdot R_{ON} + I^2_{OUTB} \cdot R_{ON} \end{aligned} \qquad (4)$$

Given R_{LA} and R_{LB}, (1), (2), (3), (4) can be used to calculate P_D, T_j, etc. through iteration.

For example, let $V_L = 0V$, $V_{CC} = 10V$, $R_{LA} = 100\Omega$, $R_{LB} = 50\Omega$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$.

Assume:

$R_{ON} = 12.28\Omega$

By (2):

$$I_{OUTA} = \frac{10}{12.28 + 100} = 0.089A$$

$$I_{OUTB} = \frac{10}{12.28 + 50} = 0.161A$$

By (4):

$$P_D = (0.089)^2 \cdot 12.28 + (0.161)^2 \cdot 12.28 = 0.41W$$

By (1):

$T_j = 70.5°C$

And by (3):

$R_{ON} = 12.28\Omega$

DESIGN TECHNIQUE

In a typical design, R_L must be chosen to satisfy the load requirement (e.g., a minimum current to turn on a relay) and at the same time, the power consumed in the driver package must be kept below its maximum power handling capability.

To minimize the design effort, a graphical technique is developed, which combines all the parameters in one plot, which can be used efficiently to obtain an optimal design.

Assume $T_A = 25°C$ and that both sections of the MM74C908 in *Figure 3* are operating under identical conditions. The maximum allowable package dissipation is:

$$\begin{aligned} P_D &= 2\,(V_{CC} - V_{OUT}) \times I_{OUT} \\ &= \frac{1}{110}\,(150 - T_A) = 1.14W \end{aligned} \qquad (6)$$

where $T_j = 150°C$, $\theta_{jA} = 110°C/W$ are used in (1) per the data sheet.

Thus, the maximum power allowed in each section is:

$$P_D = (V_{CC} - V_{OUT}) \times I_{OUT} = 0.57W$$

A constant power curve $P_D = 0.57W$ can then be plotted as shown in *Figure 4*. The circuit must operate below this curve. Any voltage-current combination beyond it (in the shaded region) will not guarantee T_j to be lower than 150°C.

For any given R_L, a load line (7) can be superimposed on *Figure 4*.

$$I_{OUT} = \frac{1}{R_L}\,(V_{CC} - V_L) - \frac{1}{R_L}\,(V_{CC} - V_{OUT}) \qquad (7)$$

The slope of this load line is $-1/R_L$ and it intersects with the vertical and horizontal axes at $1/R_L\,(V_{CC} - V_L)$ and $V_{CC} - V_L$ respectively.

Given V_{CC} and V_L, a minimum R_L can be obtained by drawing the load line tangent to the constant power curve. In *Figure 4*, at $V_{CC} - V_L = 5V$ the line intersects I_{OUT} axis at $I_{OUT} = 450$ mA. Thus, $R_{L(MIN)} = 5V/450$ mA $= 11.1\Omega$. Any R_L value below this will move the intersecting point up and cause a section of the load line to extend into the shaded region. Therefore, the junction temperature can exceed $T_{j(MAX)} = 150°C$ in the worst case if the circuit operates on such a section of the load line.

Whether this situation will occur or not is determined by both the value of $V_{CC} - V_L$ and the R_{ON} range of the drivers.

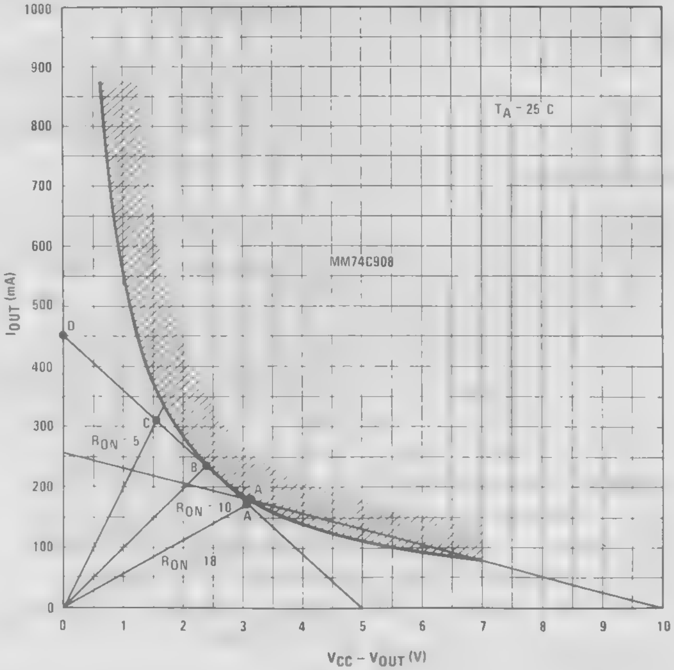


FIGURE 4

By (3), at T_j = 150°C $R_{ON(MAX)}$ = 18Ω, this is a straight line* passing through the origin with a slope of $I_{OUT}/(V_{CC} - V_{OUT})$ = 1/18 mho and intersects the load line at point A. Similarly, point B and C can be found for typical (~10Ω) and minimum (~5Ω) R_{ON} at T_j = 150°C.

For $V_{CC} - V_L$ = 5V, the tangent point falls between A and C. Hence, $R_L \geq 11.1\Omega$ calculated above must be satisfied; otherwise, part of the load line within the specified R_{ON} range will extend into the shaded region and therefore, $T_j \geq 150°C$ may occur.

For $V_{CC} - V_L$ = 10V, however, a section of the load line can go beyond the P_D = 0.57W curve without affecting the safe operation of the circuit. By inspection of *Figure 4*, the reason is clear—the load line extends into the shaded region only outside of the specified R_{ON} range (to the right of point A'). Within the R_{ON} range, the load line lies below the P_D = 0.57W curve, thus, a safe operation.

To a first approximation**, the section of the load line between A and C is the operating range for the circuit at $V_{CC} - V_L$ = 5V and R_L = 11.1Ω. Hence, the available current and voltage ranges for this circuit are 310 mA $\geq I_{OUT} \geq$ 172 mA and 3.4V $\geq V_{OUT} \geq$ 1.9V, respectively.

Thus, by simply drawing no more than 3 straight lines, one obtains all of the following immediately:

1. All the necessary design information (e.g., minimum R_L, minimum available I_{OUT} and V_{OUT}, etc.)
2. Operating characteristics of the circuit as a whole, including the effect of different R_{ON} values due to process variations, thus, a better insight into the circuit operation.
3. Most importantly, a guarantee that the circuit will be operating in the safe region, ($T_j \leq 150°C$).

For different ambient temperatures or for different power considerations, *Figure 4* can be applied by properly scaling the I_{OUT} axis. (Note that $I_{OUT} \propto T_j - T_A$ and $I_{OUT} \propto P_D$).

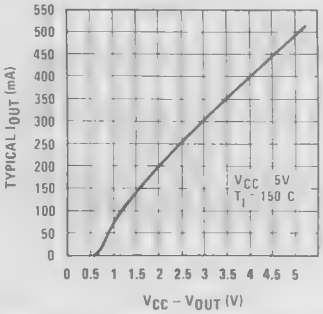


FIGURE 5. Typical I_{OUT} vs Typical V_{OUT}

*Strictly speaking, R_{ON} is a non-linear function of I_{OUT}. A typical R_{ON} characteristic at T_j = 150°C is shown in *Figure 5*. The non-linear characteristic near the origin is due to the fact that the output NPN transistor is not saturated. As soon as saturation is reached (I_{OUT} ~ 150 mA) the curve becomes a straight line which extrapolates back to the origin. For practical design purposes, it is sufficient to consider R_{ON} as a linear function of I_{OUT}.

**Note that as the operating point on the load line moves away from the P_D = 0.57W curve, (away from the tangent point in this case), the actual junction temperature drops. Therefore, at point A, for example, the device is actually running cooler than T_j = 150°C, even in the worst case. Hence, R_{ON} value drops below 18Ω and the actual operating point is slightly different from A.

Figure 4, is generated from (6) by using appropriate T_A values. The application of these curves is illustrated as follows:

Example 1

1. In *Figure 3*, assume that the two drivers in the MM74C908 package are to operate under identical conditions. Find minimum R_L at T_A = 25°C, 45°C, 65°C and 85°C for both $V_{CC} - V_L = 5V$ and $V_{CC} - V_L = 10V$.

   Then plot $R_{L(MIN)}$ vs T_A.

   a) $V_{CC} - V_L = 5V$

   By constructing the load lines tangent to the curves for T_A = 25°C, 45°C, 65°C and 85°C, $R_{L(MIN)}$ for each case can be obtained through the vertical coordinate for the intersection points as shown in *Figure 6*. These are calculated in Table I.

   Note that the same results (within graphical error) can be obtained analytically by letting $dR_L/dR_{ON} = 0$. It can be shown that

$$R_{L(MIN)} = \frac{(V_{CC} - V_L)^2}{4X \text{ (Max Power Per Driver)}} \tag{8}$$

minimum if the tangent point does not fall inside the specified R_{ON} region. The actual $R_{L(MIN)}$ can be obtained as shown in *Figure 7*. The calculations and results are given in Table II.

Note that the $R_{L(MIN)}$ values in Table II are lower than those given by (8). This corresponds to the section on each of the 4 load lines in *Figure 7* which extends beyond the power limit curve at each associated temperature. However, this section on each load line is outside the specified R_{ON} range. Within the R_{ON} range, load lines are below the power limits; therefore, safe operation is guaranteed.

The $R_{L(MIN)}$ vs T_A plot is as shown in *Figure 8*.

All the curves generated so far are restricted to $P_D \leq 0.57W$ due to our simplifying assumption that both drivers are operating identically. In *Figure 9* a few more curves are added to account for the general situation in which only the restriction $P_{DA} + P_{DB} \leq 1.14W$ is required, (i.e., P_{DA} can be different from P_{DB}). Application of *Figure 9* is illustrated as follows:

TABLE I.

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	450	375	310	240
$R_{L(MIN)} = \frac{5}{I_{OUT} @ D1, 2, 3, 4}$ (Ω)	11.1	13.3	16.1	20.8

TABLE II.

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	261	230	197	166
$R_{L(MIN)} = \frac{10}{I_{OUT} @ D1, 2, 3, 4}$ (Ω)	38.3	43.5	50.8	60.2

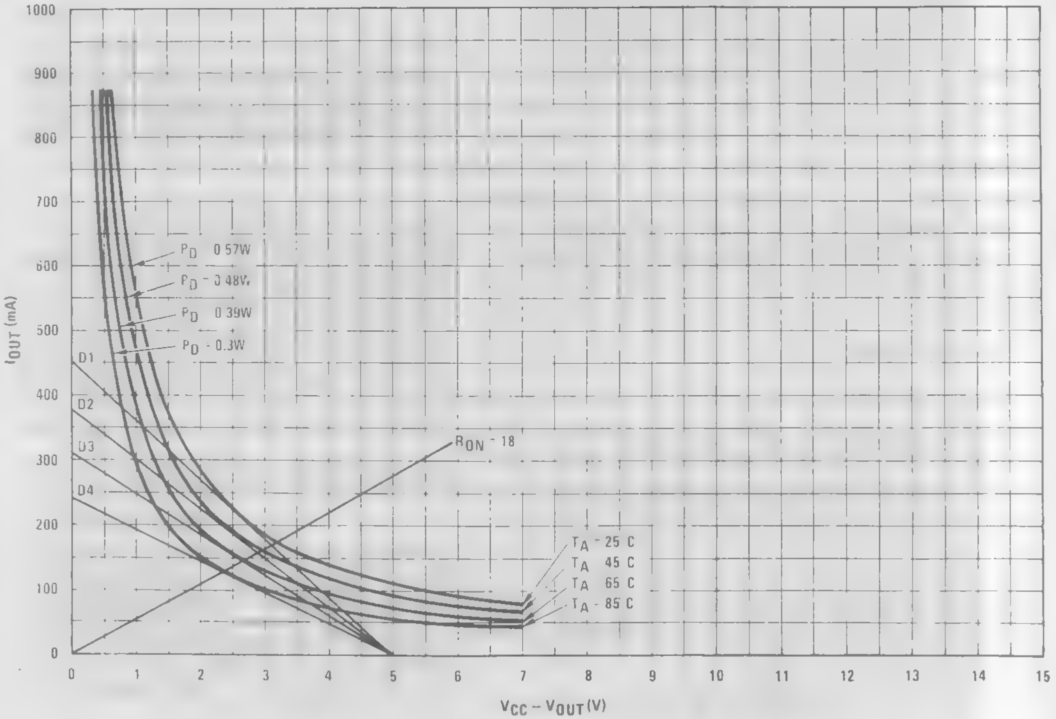


FIGURE 6

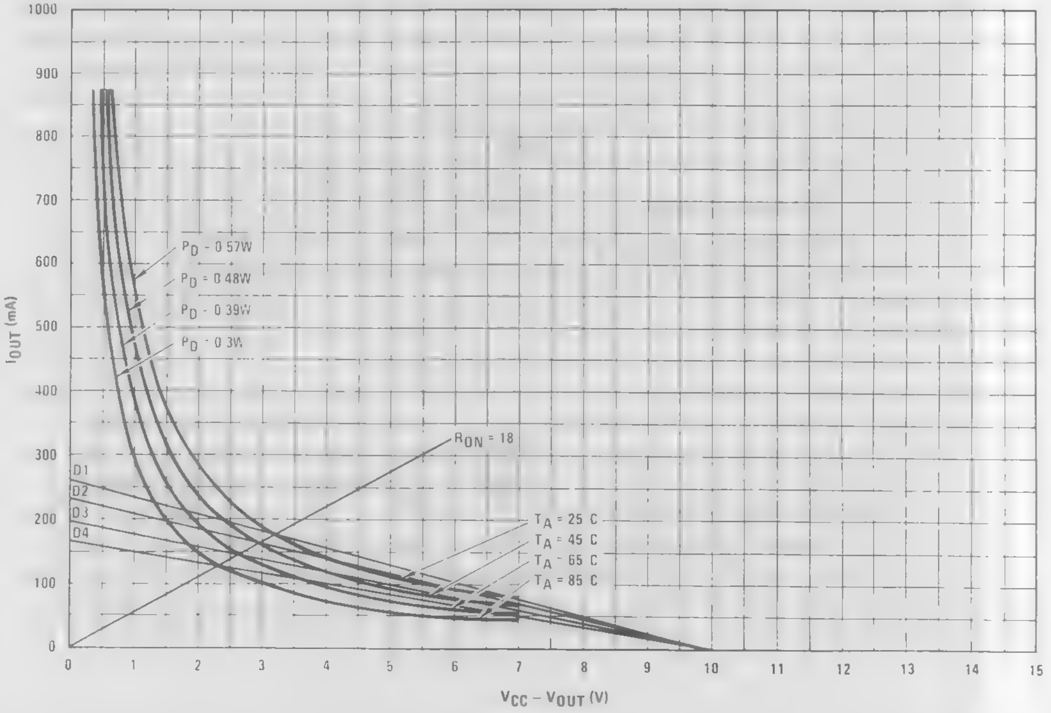


FIGURE 7

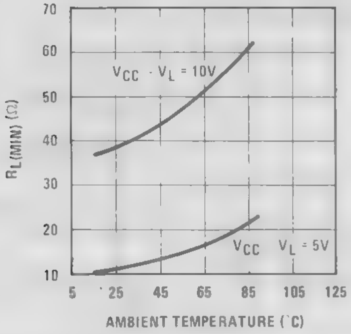


FIGURE 8

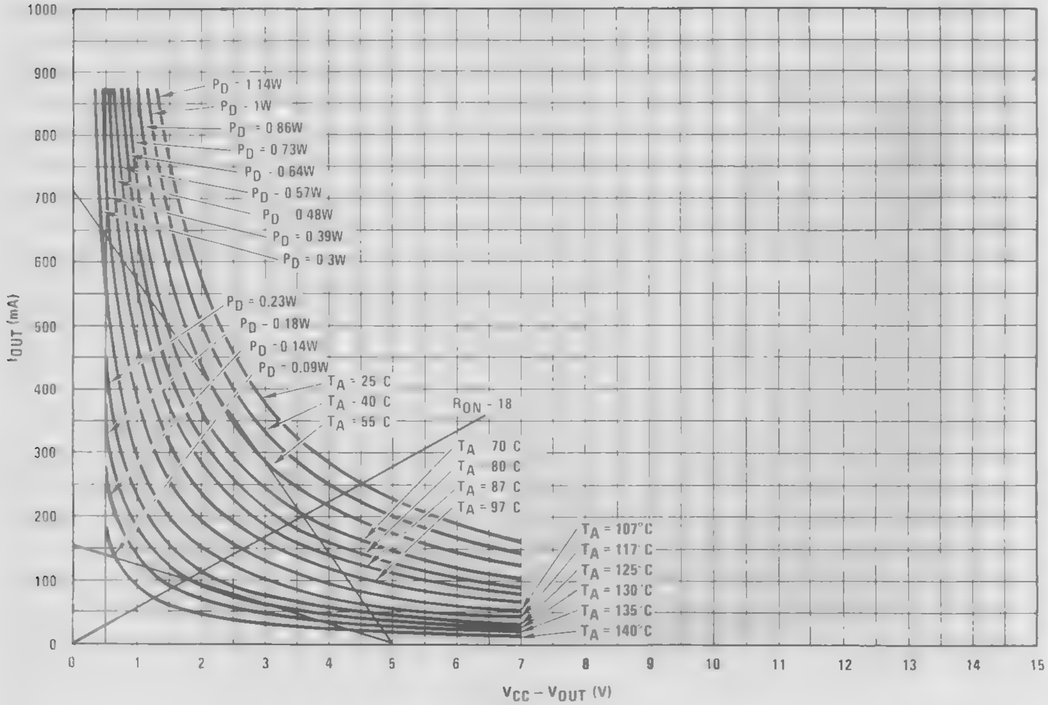


FIGURE 9

Example 2

In *Figure 3*, assume that driver A has to deliver 200 mA to its load while driver B needs only 100 mA. Design R_{LA} and R_{LB} for $V_{CC} - V_L = 5V$.

By inspection of *Figure 4*, units with high R_{ON} values will not be able to deliver 200 mA. However, since section B does not need the same amount of drive, we can reduce the power consumed in this section to compensate for the higher power (> 0.57W) required in section A.

The design procedure follows:

Section A

1. Draw a load line intersecting R_{ON} = 18Ω line at I_{OUT} = 200 mA.
2. This load line intersects the I_{OUT} axis at I_{OUT} = 710 mA and is tangent to $P_{DA} \simeq 0.9W$ curve, thus $R_{LA} \cong 5V/710\ mA = 7.1\Omega$ will guarantee both $P_{DA} \leq 0.9W$ and $I_{OUTA} \geq 200\ mA$.

Section B

1. Draw a load line intersecting R_{ON} = 18Ω line at I_{OUT} = 100 mA.
2. Similar to (2) above, it is seen immediately that $R_{LB} \cong 5V/150\ mA = 33.3\Omega$ will guarantee $I_{OUTB} \geq$ 100 mA and $P_{DB} \leq 0.18W$.

Since $P_{DA} + P_{DB} \leq 0.9 + 0.18 < 1.14W$

$R_{LA} = 7.1\Omega$
$R_{LB} = 33.3\Omega$

satisfy all the requirements in this problem.

The design in Example 2 illustrated the simple and straight-forward use of the curves and the result meets all the problem requirements. However, it should be noted that there is not much design margin left for tolerance in resistances and other circuit parameters. The reason is obvious—we are pushing at the power limit of the MM74C908 package—and the solutions are simple:

a) Increase V_{CC} supply
b) Use the higher power package MM74C918.

The design for higher V_{CC} is identical to that in Example 2 and will not be repeated here.

For the 14-lead higher power (2.27W) MM74C918, θ_{jA} = 55°C/W, this is exactly half that of the 8-lead MM74C908. Therefore, by scaling the I_{OUT} axis by a factor of 2, the same family of curves in *Figure 9* can be applied directly. This is shown in *Figure 10*. (Note that the slope of the R_{ON} = 18Ω line has been adjusted to the new scale).

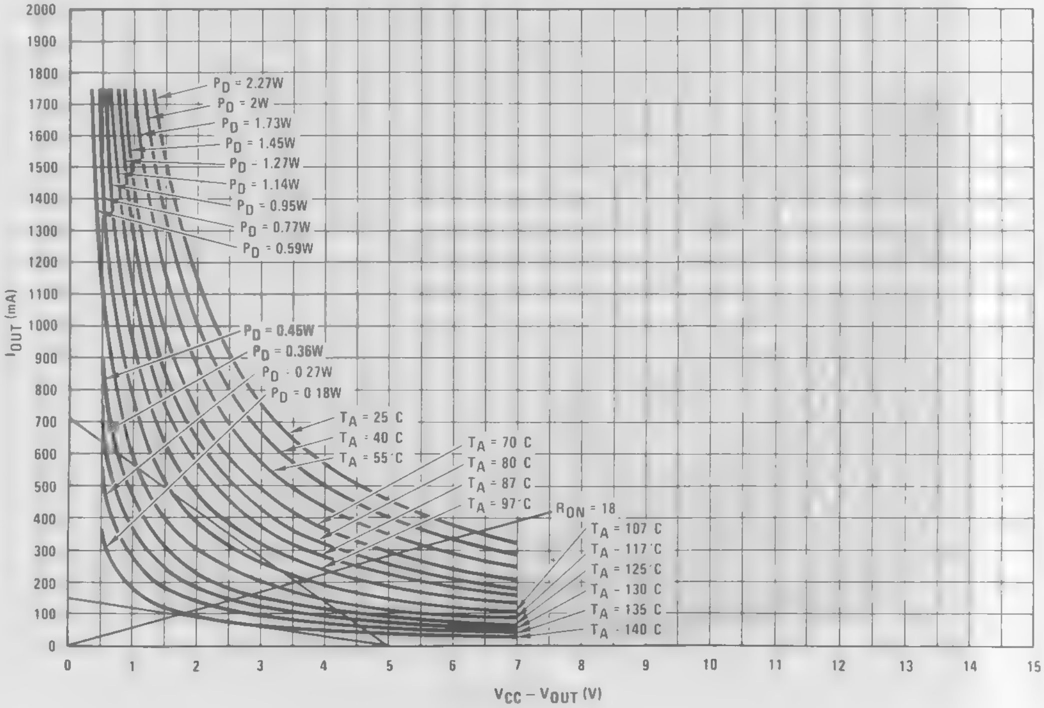


FIGURE 10

By drawing the same load lines, it is found that:

$R_{LA} \cong 5V/710\ mA = 7.1\Omega$
guarantees $P_{DA} \leq 0.9W$.

and

$R_{LB} \cong 5V/150\ mA = 33.3\Omega$
guarantees $P_{DB} \leq 0.18W$

$P_{DA} + P_{DB} \leq 1.08W$

which is way below the maximum power 2.27W available. Therefore, both R_{LA} and R_{LB} can be lowered to account for tolerance in the resistors. Consider specifically the following example:

Example 3

Assume driver A, B of the MM74C918 have to deliver 250 mA and 150 mA, respectively, to its load. Design R_{LA} and R_{LB} at $V_{CC} - V_L = 10V$.

Driver A

1. In *Figure 11*, draw the load line intersecting $R_{ON} \doteq 18\Omega$ at $I_{OUT} = 250$ mA.
2. This load line intersects the I_{OUT} axis at 450 mA. Thus, by inspection $R_{LA} \cong 10V/450\ mA \cong 22.2\Omega$ guarantees $P_{DA} \leq 1.14W$.

Driver B

1. Draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 150$ mA.
2. This load line intersects the I_{OUT} axis at 210 mA. Thus, by inspection $R_{LB} \cong 10V/210\ mA = 47.6\Omega$ guarantees $P_{DB} \leq 0.4W$.

Since $P_{DA} + P_{DB} \leq 1.14 + 0.4 = 1.8W$, while the package is capable of delivering 2.27W, both R_{LA} and R_{LB} can be lower than the above values and the circuit still operates safely. By picking the closest standard resistance values:

$R_{LA} = 20\Omega$
$R_{LB} = 43\Omega$

For 5% tolerance in these values,

$19\Omega \leq R_{LA} \leq 21\Omega$
$40.85\Omega \leq R_{LB} \leq 45.15\Omega$

Thus:

$$I_{OUTA(MIN)} \geq \frac{10V}{18\Omega + 21\Omega} = 256.4\ mA > 250\ mA$$

$$I_{OUTB(MIN)} \geq \frac{10V}{18\Omega + 45.15\Omega} = 158.3\ mA > 150\ mA$$

$$P_{DA(MAX)} \leq \left(\frac{10V}{18\Omega + 19\Omega}\right)^2 \cdot 18\Omega = 1.31W$$

$$P_{DB(MAX)} \leq \left(\frac{10V}{18\Omega + 40.85\Omega}\right)^2 \cdot 18\Omega = 9.52W$$

$$P_{DA(MAX)} + P_{DB(MAX)} \leq 1.31 + 0.52 < 2.27W$$

Therefore:

$R_{LA} = 20\Omega$ (1.5W, 5%)
$R_{LB} = 43\Omega$ (1W, 5%)

will guarantee satisfactory performance of the circuit.

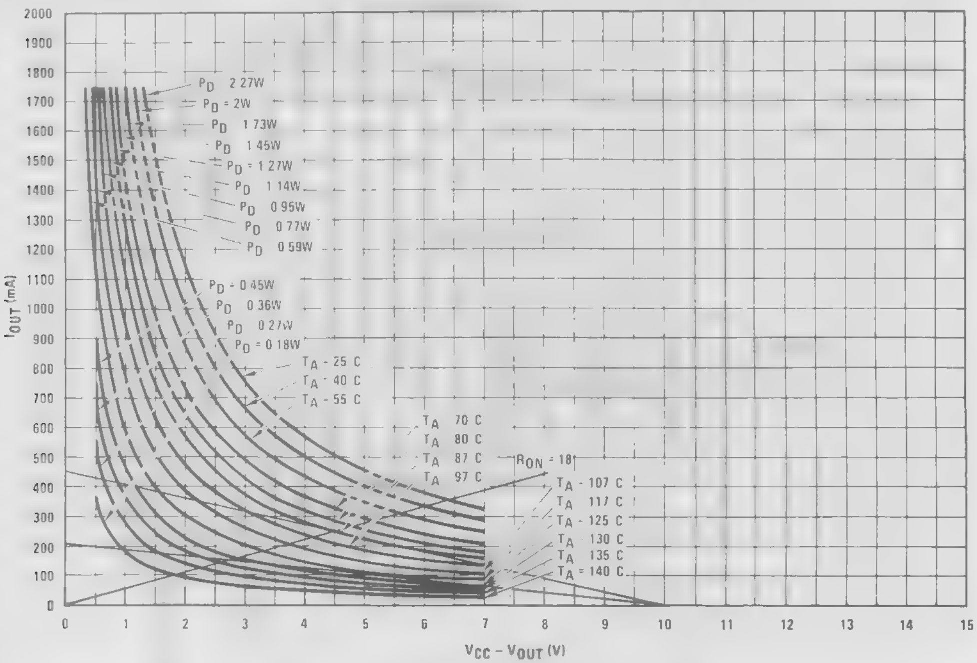


FIGURE 11

APPLICATIONS

Like most other drivers, the MM74C908, MM74C918 can be used to drive relays, lamps, speakers, etc. These are shown in *Figure 12*. (To suppress transient spikes at turn-off, a diode as shown as *Figure 12a* is recommended at the relay coil or any other inductive load.)

However, the MM74C908, MM74C918 offers a unique CMOS feature that is not available in drivers from other logic families—extremely low standby power. At V_{CC} = 15V, power dissipation per package is typically 750 nW when the outputs are not drawing current. Thus, the drivers can be sitting out on line (a telephone line, for example) drawing essentially zero current until activated—an ideal feature for many applications.

The dual feature and the NAND function of the driver design can also be used to advantage as shown in the following applications:

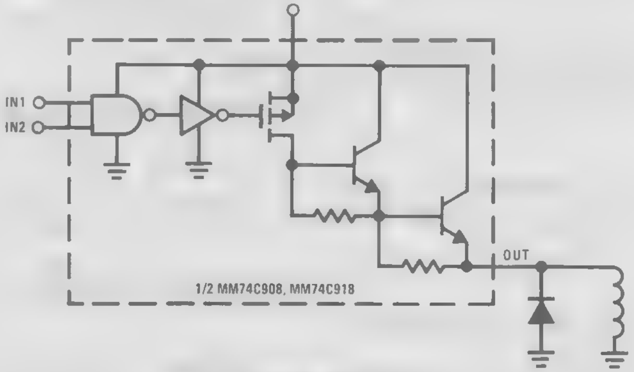


FIGURE 12a. Relay Driver

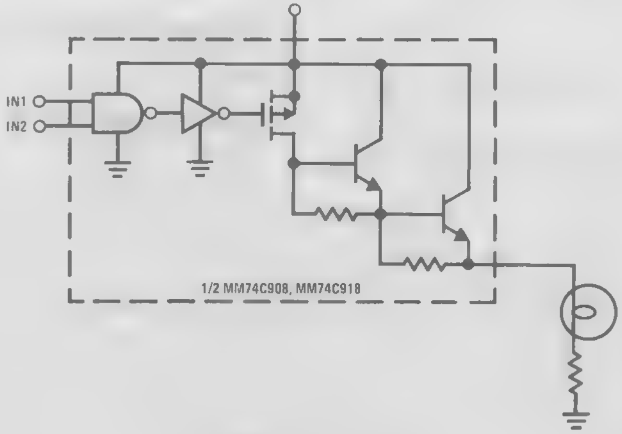


FIGURE 12b. Lamp Driver

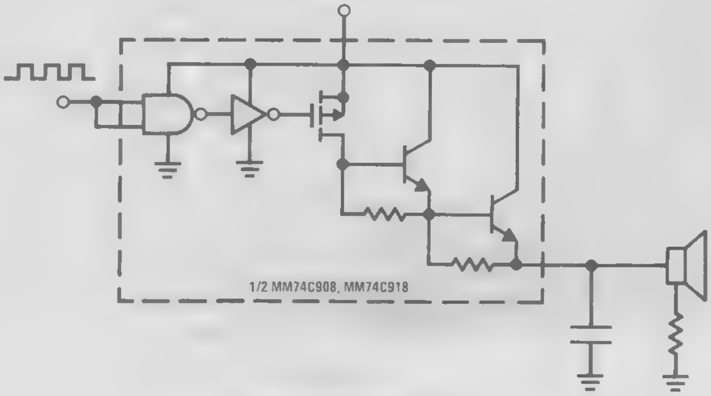


FIGURE 12c. Speaker Driver

In *Figure 13*, the 2 drivers in the package are connected as a Schmitt trigger oscillator, where R1 and R2 are used to generate hysteresis. R3 and C are the inverting feedback timing elements and R4 is the pull-down load for the first driver. Because of its current capability, the circuit can be used to drive an array of LEDs or lamps. If resistor R4 is replaced by an LED (plus a current limiting resistor), the circuit becomes a double flasher with the 2 LEDs flashing out of phase. This is shown in *Figure 14*.

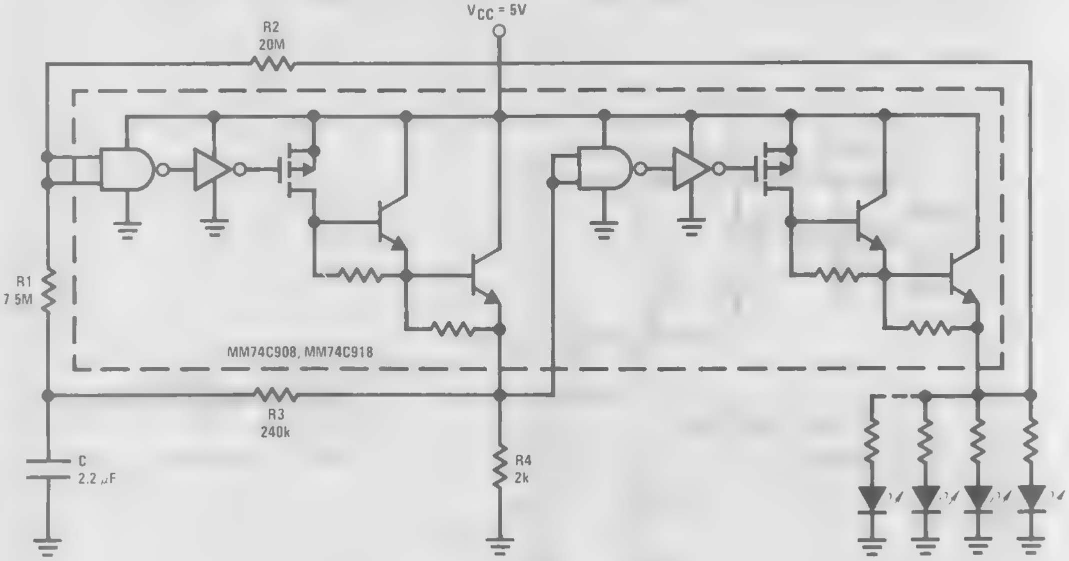


FIGURE 13. High Drive Oscillator/Flasher

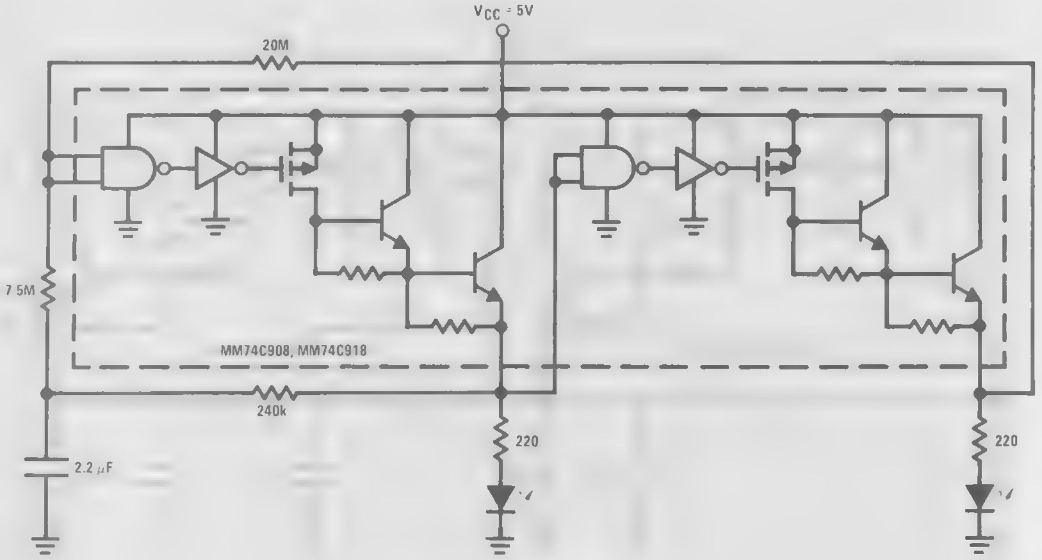


FIGURE 14. Out of Phase Double Flasher

Another oscillator circuit using only 1/2 of the package and 4 passive components is shown in *Figure 15*. Assume V_I is slightly below the input trip point, the driver is "ON" and charging both V_O and V_I until V_I reaches the trip point, V_T, when the driver starts to turn "OFF". V_O can be made much higher than V_I at this instance by adjusting the component values such that $R_fC_f >> (R_{ON}||R_L)C_L$. Since V_O is higher than V_I, V_I is still going up, although the driver is "OFF" and V_O is ramping down. The rising V_I will eventually equal to the falling V_O, and then start discharging. Then, both V_I and V_O discharge until V_I hits the trip point, V_T, again, when the driver is turned "ON", charging up V_O and subsequently V_I to complete a cycle.

This oscillator is ideal for low cost applications like the 1-package siren shown in *Figure 16*, where 1 oscillator is used as a VCO while the other is generating the voltage ramp to vary the frequency at the VCO output.

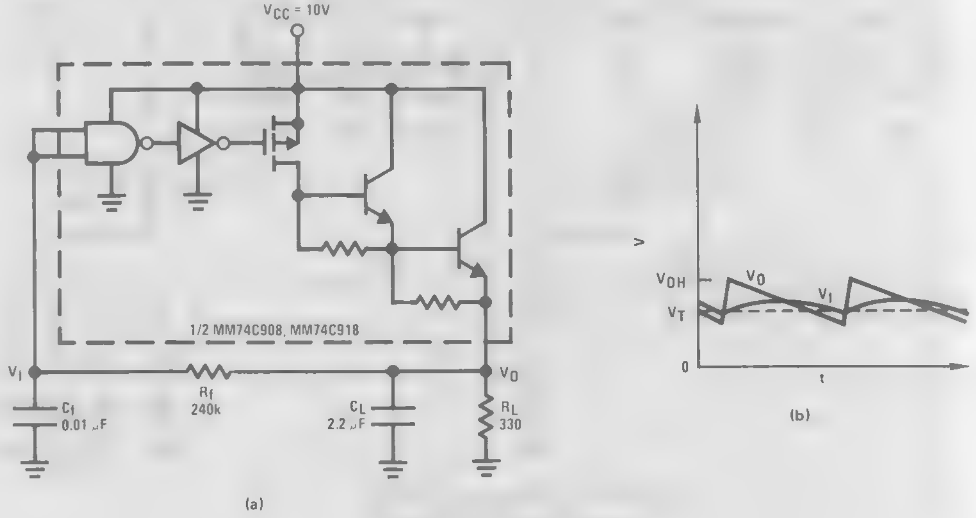


FIGURE 15. Single Driver Oscillator

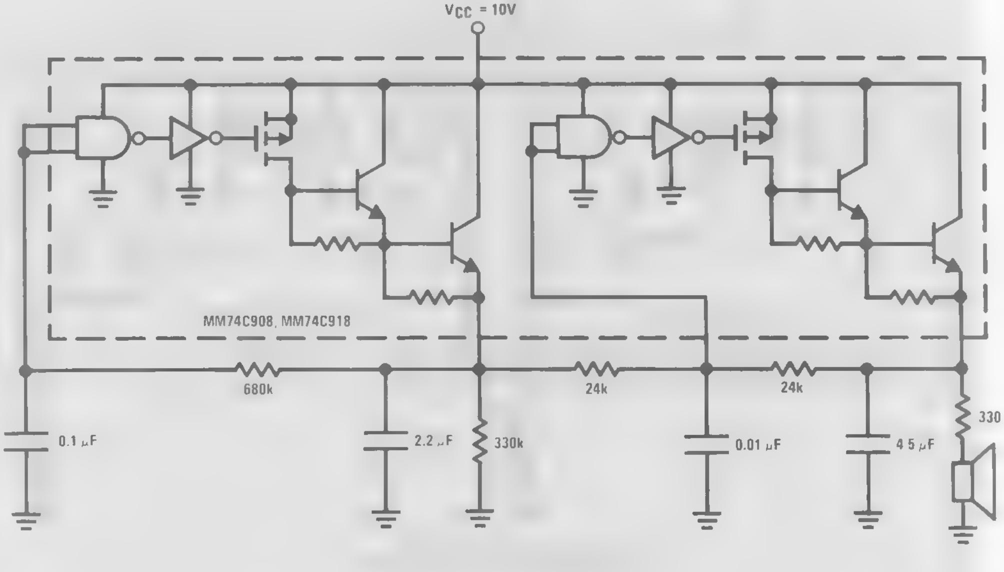


FIGURE 16. Low Cost Siren

The NAND functions at the input can also be used to reduce package count in applications where both high output drive and input NAND features are required. One such example is given in *Figure 17*.

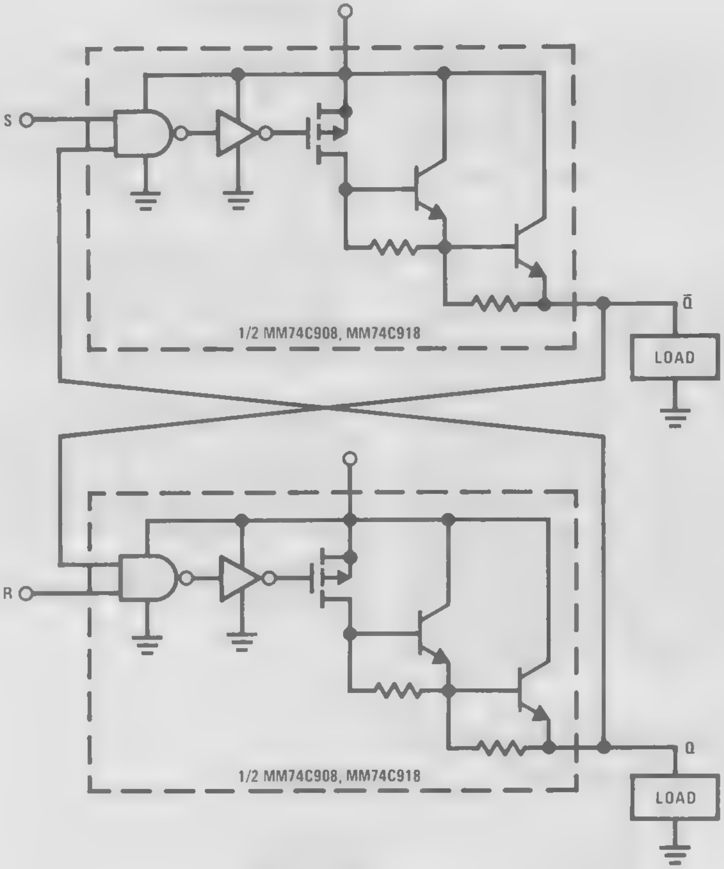


FIGURE 17. High Drive RS Latch

CMOS A/D CONVERTED CHIPS EASILY INTERFACE TO 8080A MICROPROCESSOR SYSTEMS — AN-200

CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
Application Note 200
Jake Buurma

SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters — two of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 1/2-digit DPM and ADD3701 3 3/4-digit DPM) while the other two (ADC3511 3 1/2-digit A/D and ADC3711 3 3/4-digit A/D) have addressable BCD outputs. These last two devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 1/2-digit types divide the input into 2,000 counts plus sign, while the 3 3/4-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 1/2-digit converters require 200 ms per conversion; 3 3/4-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the inputs must be floating with respect to the supply return. Without a floating supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

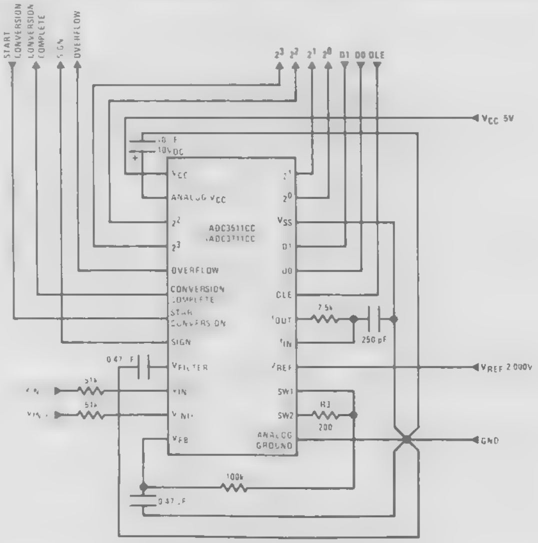


FIGURE 1. Basic A/D Converter

address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal "EEEE" plus an Overflow output.

A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

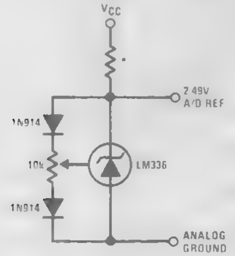
The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is

on the number of converters used.



$$^{*}R1 = \frac{2.49V}{(2N + 1)\ mA} \quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3 and 4*. *Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multichannel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a "1" is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a "1" in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of "1's" in the status word. The routine loads the address pointer to digit 4 of the selected converter. The program then calls a subroutine which goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

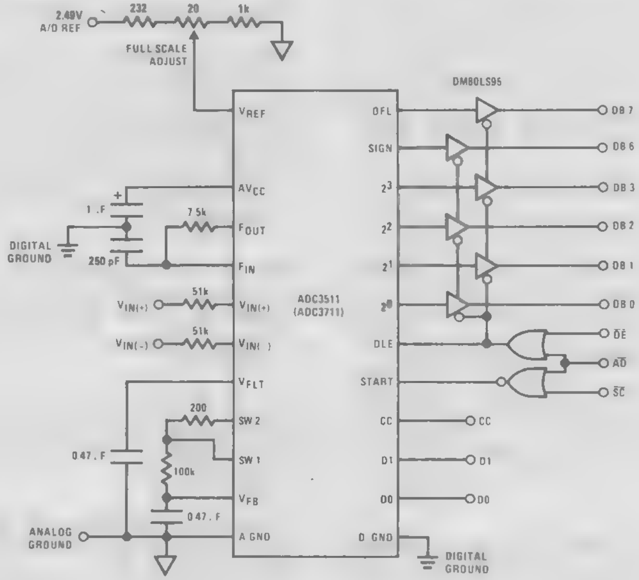


FIGURE 3. Dual Polarity A/D Requires that Inputs are Floating with Respect to the Supply. Input Range is ±1.999V.

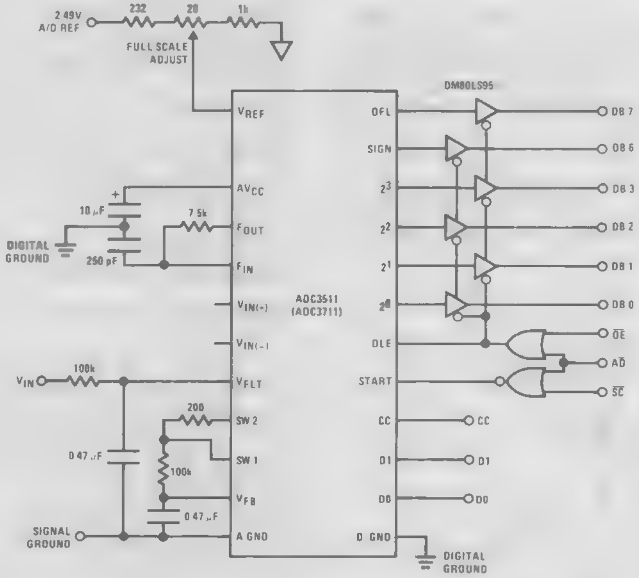


FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range is +1.999V.

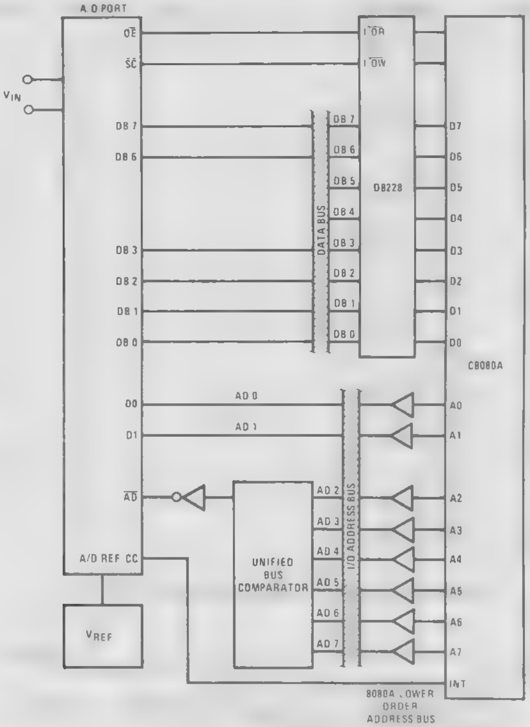


FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O

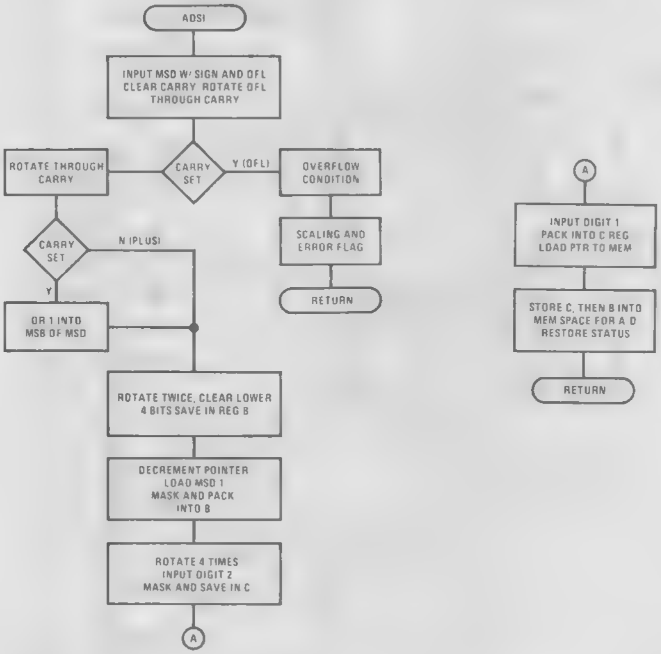

ADSI
INPUT MSD W/ SIGN AND OFL CLEAR CARRY ROTATE OFL THROUGH CARRY
CARRY SET
Y (OFL)
OVERFLOW CONDITION
SCALING AND ERROR FLAG
RETURN
ROTATE THROUGH CARRY
CARRY SET
N (PLUS)
Y
OR 1 INTO MSB OF MSD
ROTATE TWICE, CLEAR LOWER 4 BITS SAVE IN REG B
DECREMENT POINTER LOAD MSD 1 MASK AND PACK INTO B
ROTATE 4 TIMES INPUT DIGIT 2 MASK AND SAVE IN C
A
A
INPUT DIGIT 1 PACK INTO C REG LOAD PTR TO MEM
STORE C, THEN B INTO MEM SPACE FOR A D RESTORE STATUS
RETURN

FIGURE 6. Flow Chart for Single Channel A/D Converter

```
LABEL   OPCODE  OPERAND   COMMENT
ADIS:   PUSH    PSW       ; A/D interrupt
                            service
        PUSH    H         ; save
        PUSH    B         ; current status
        IN      ADD 4     ; input A/D digit 4
        IN      ADD 4     ; delay
        ORA               ; reset carry
        RAL               ; rotate OFL thru
                            carry
        JC      OFL       ; overflow condition
        RAL               ; rotate sign thru
                            carry
        JC      PLUS      ; positive input
        ORI     20H       ; OR 1 into MSB,
                            neg input
PLUS:   RAL               ; shift
        RAL               ; into position
        ANI     FO        ; mask lower bits
        MOV     BA        ; save in B
        IN      ADD 3     ; input digit 3
        IN      ADD 3     ; delay
        ANI     OF        ; mask higher bits
        OR      B         ; pack into B
        MOV     B, A      ; save in B
        IN      ADD 2     ; input digit 2
```

```
LABEL   OPCODE  OPERAND   COMMENT
        IN      ADD 2     ; delay
        RAL               ; rotate
        RAL               ; into
        RAL               ; upper
        RAL               ; 4 bits
        ANI     FO        ; mask lower bits
        MOV     C, A      ; save in C
        IN      ADD 1     ; in digit 1
        IN      ADD 1     ; delay
        ANI     OF        ; mask upper bits
        OR      C         ; pack
        MOV     C, A      ; save in C
        LXI     H, ADMS   ; load ptr to A/D
                            Mem, space
        MOV     M, C      ; save C in memory
        INX     H         ; point next
        MOV     M, B      ; save B in memory
        OUT     ADD 1     ; start new conver-
                            sion
        POP     B         ; restore
        POP     H         ; previous
        POP     PSW       ; status
        EI                ; enable interrupts
        RET               ; return to main
                            program
```

Routine 1. Single Channel Interrupt Service Routine

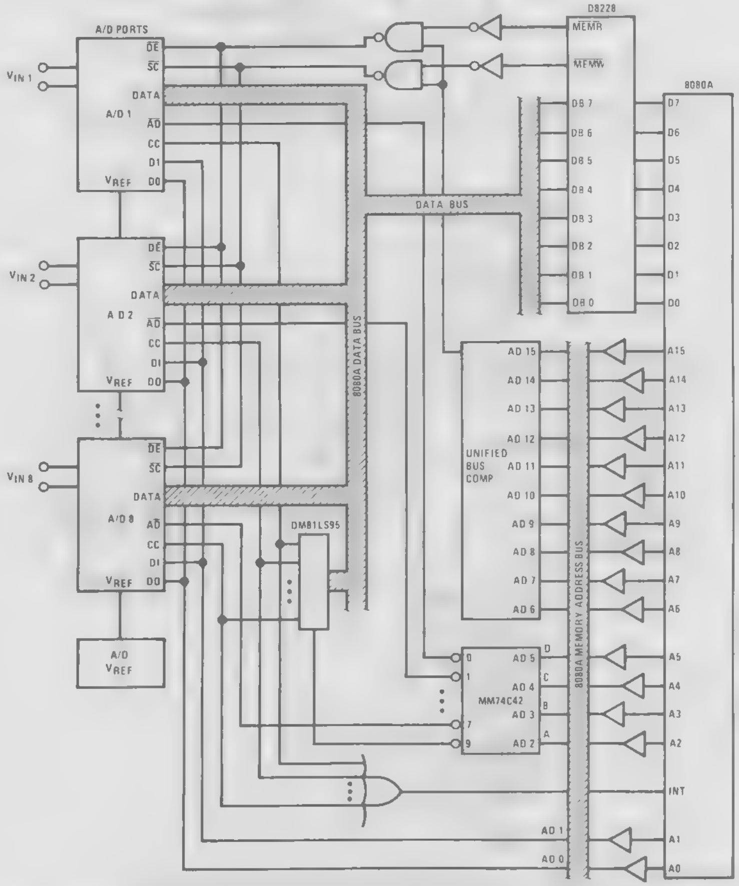


FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O

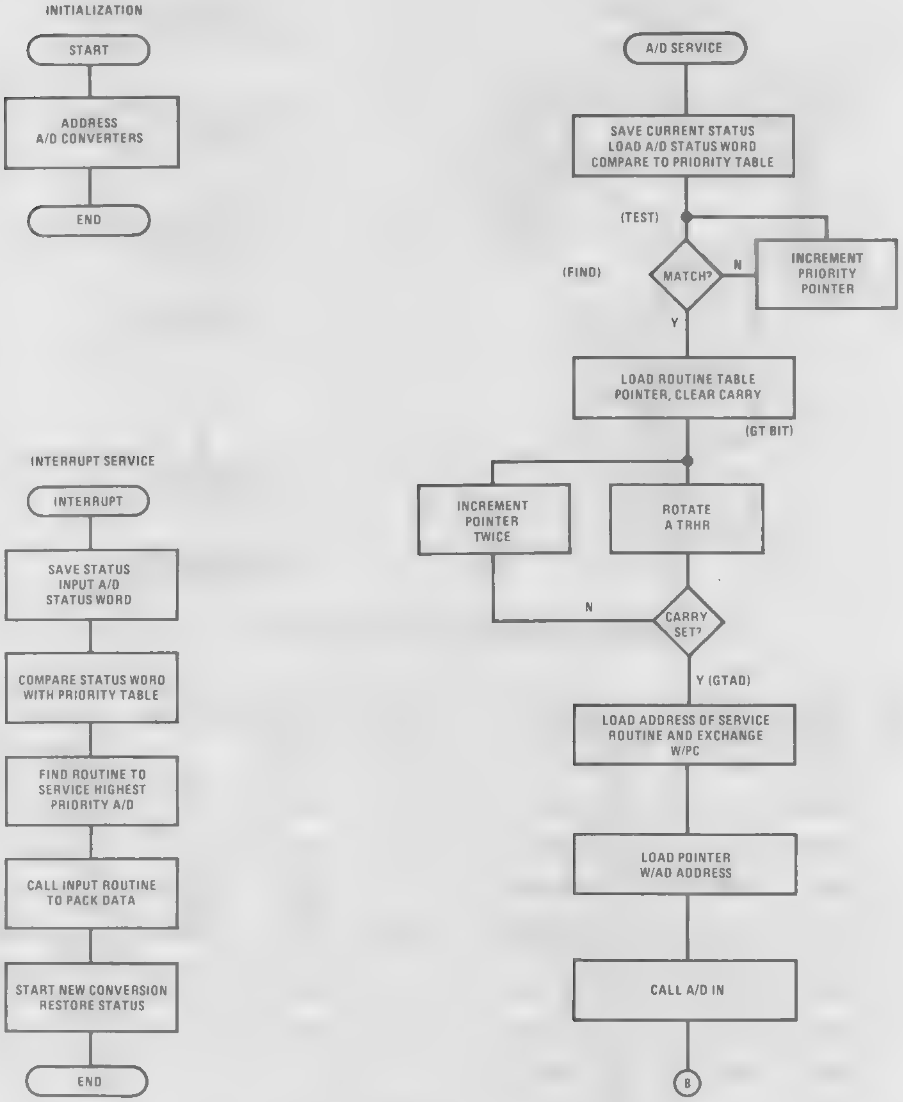

INITIALIZATION
START
ADDRESS A/D CONVERTERS
END
INTERRUPT SERVICE
INTERRUPT
SAVE STATUS INPUT A/D STATUS WORD
COMPARE STATUS WORD WITH PRIORITY TABLE
FIND ROUTINE TO SERVICE HIGHEST PRIORITY A/D
CALL INPUT ROUTINE TO PACK DATA
START NEW CONVERSION RESTORE STATUS
END
A/D SERVICE
SAVE CURRENT STATUS LOAD A/D STATUS WORD COMPARE TO PRIORITY TABLE
(TEST)
(FIND)
MATCH?
N
INCREMENT PRIORITY POINTER
Y
LOAD ROUTINE TABLE POINTER, CLEAR CARRY
(GT BIT)
INCREMENT POINTER TWICE
ROTATE A TRHR
N
CARRY SET?
Y (GTAD)
LOAD ADDRESS OF SERVICE ROUTINE AND EXCHANGE W/PC
LOAD POINTER W/AD ADDRESS
CALL A/D IN
B

FIGURE 8. Flow Charts of A/D Routines

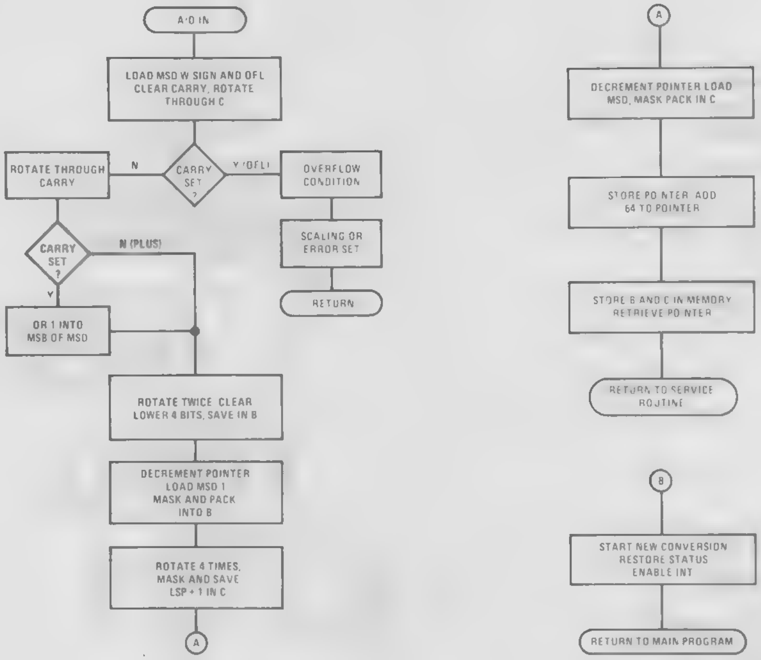

A/D IN
LOAD MSD W SIGN AND OFL CLEAR CARRY, ROTATE THROUGH C
ROTATE THROUGH CARRY
N
CARRY SET ?
Y (OFL)
OVERFLOW CONDITION
SCALING OR ERROR SET
RETURN
CARRY SET ?
N (PLUS)
Y
OR 1 INTO MSB OF MSD
ROTATE TWICE CLEAR LOWER 4 BITS, SAVE IN B
DECREMENT POINTER LOAD MSD 1 MASK AND PACK INTO B
ROTATE 4 TIMES, MASK AND SAVE LSP + 1 IN C
A
A
DECREMENT POINTER LOAD MSD, MASK PACK IN C
STORE POINTER ADD 64 TO POINTER
STORE B AND C IN MEMORY RETRIEVE POINTER
RETURN TO SERVICE ROUTINE
B
START NEW CONVERSION RESTORE STATUS ENABLE INT
RETURN TO MAIN PROGRAM

FIGURE 8. Flow Charts of A/D Routines (Continued)

```
LABEL   OPCODE  OPERAND    COMMENT
IAD     PUSH    PSW        ; interrupt from A/D
        PUSH    H          ; save H & L on
                             stack
        PUSH    B          ; save B & C on
                             stack
        PUSH    D          ; save D & E on
                             stack
        LXI     H, ADWD    ; pickup A/D status
                             word
        MOV     6, M       ; move word into B
        LXI     H, PRTBL   ; pickup priority tbl
                             pointer
TEST:   MOV     A, B       ; place status word
                             in accum.
        ANA     M          ; mask with priority
                             table
        JNZ     FIND       ; match jump to
                             Find
        INX     H          ; point to lower
                             priority
        JMP     TEST       ; try again
FIND:   LXI     H, RTBL    ; pickup routine tbl
                             pointer
        ORA     A          ; reset carry
GTBIT:  RAR                ; rotate thru carry
        JC      GTAD       ; bit was found
        INX     H          ; point to
        INX     H          ; next routine
        JMP     GTBIT      ; try again
GTAD:   MOV     E, M       ; move first byte
                             into E
        INX     H          ; point to next byte
        MOV     D, M       ; move second byte
                             into D

LABEL   OPCODE  OPERAND    COMMENT
        XCGH               ; exchange DE, HL
        PCHL               ; jump to input
                             routine
INAD1:  LXI     H, AD1     ; pickup pointer to
                             A D 1
        CALL    ADIN       ; call common input
                             routine
        MOV     M, A       ; start new conversion
        JMP     DONE       ; all done
INAD2:  LXI     H, AD2     ; pickup pointer to
                             A/D 2
        CALL    ADIN       ; call input routine
        MOV     M, A       ; start new conver-
                             sion
        JMP     DONE       ; all done

DONE:   POP     D          ; restore D
        POP     B          ; restore B
        POP     H          ; restore H
        POP     PSW        ; restore PSW
        EI                 ; enable interrupts
        RET                ; return to main
                             program
PRTBL:  DB      04H        ; 0000C100 AD3
                             highest priority
        DB      03H        ; 00000011 AD2 &
                             AD1 next priority
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

```
LABEL    OPCODE   OPERAND    COMMENT
PRTBL:   DB       10H        ; 00010000 AD5
                               lowest priority
RTBL:    DW       1000H      ; routine for A/D 1
         DW       100CH      ; routine for A/D 2
         .
         .
         .
         DW       1060H      ; routine for A/D 8
ADIN:    MOV      A, M       ; input MSD plus
                               OFL & SIGN
         MOV      A, M       ; delay
         ORA      A          ; reset carry
         RAL                 ; rotate left thru
                               carry, OFL
         JC       OFL        ; jump to overflow
                               if set
         RAL                 ; rotate left thru
                               carry, sign
         JC       PLUS       ; jump to plus if set
         OR1      20H        ; OR1 into BCD,
                               MSB for minus
PLUS:    RAL
         RAL
         ANI      FO         ; mask lower order
                               bits
         MOV      B, A       ; save in B
         DCR      H          ; point to MSD-1
         MOV      A, M       ; input MSD-1
         MOV      A, M       ; delay
         ANI      OF         ; mask higher 4 bits
         OR       B          ; pack MSD and MSD-1
```

```
LABEL    OPCODE   OPERAND    COMMENT
         MOV      B, A       ; save in B
         DCR      H          ; point to LSD + 1
         MOV      A, M       ; input LSD + 1
         MOV      A, M       ; delay
         RAL                 ; rotate
         RAL                 ; into
         RAL                 ; upper
         RAL                 ; 4 bits
         ANI      FO         ; mask lower bits
         MOV      C, A       ; save in C
         DCR      H          ; point to LSD
         MOV      A, M       ; input LSD
         MOV      A, M       ; delay
         ANI      OF         ; mask upper bits
         OR       C          ; pack
         MOV      C, A       ; save in C
         SHLD     TEMP       ; store HL in temp
         MOV      A, L       ; move L in accum.
         ACI      64         ; generate lower
                               address
         MOV      L, A       ; above memory
                               mapped
         MOV      A, H       ; converter addresses
         ACI      0          ; include carry
         MOV      H, A       ; to upper bits
         MOV      M, C       ; store C
         INX      H          ; then
         MOV      M, B       ; store B
         LHLD     TEMP       ; retrieve HL
         RET                 ; return
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority (Continued)

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the memR strobes, then with a memW strobe to start a new conversion. The next highest priority converter should then receive its addresses and memR strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

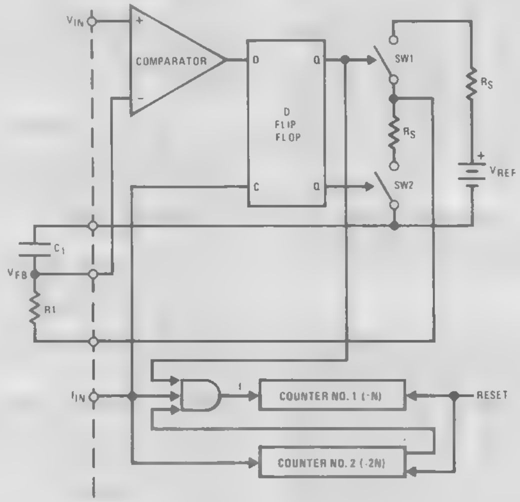
The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.
For the ADC3711 N = 4000.



$$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$$

$$f = \text{(duty cycle)} \times f_{IN}$$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

ELECTRICAL CHARACTERISTICS

ADC3511CC, ADC3711CC $4.75 \leq V_{CC} \leq 5.25V$; $-40°C \leq T_A$ +85°C, f_c = 5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	(Note 3)				
		V_{IN} = 0–2V Full-Scale	0.05	0.025	0.05	% of Full-Scale
		V_{IN} = 0–200 mV Full-Scale				
	Organization Error		-1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	-0.5	1.0	3.0	mV
	Rollover Error		-0		0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	T_A = 25°C	-5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for 'Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = 1/2 counts and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

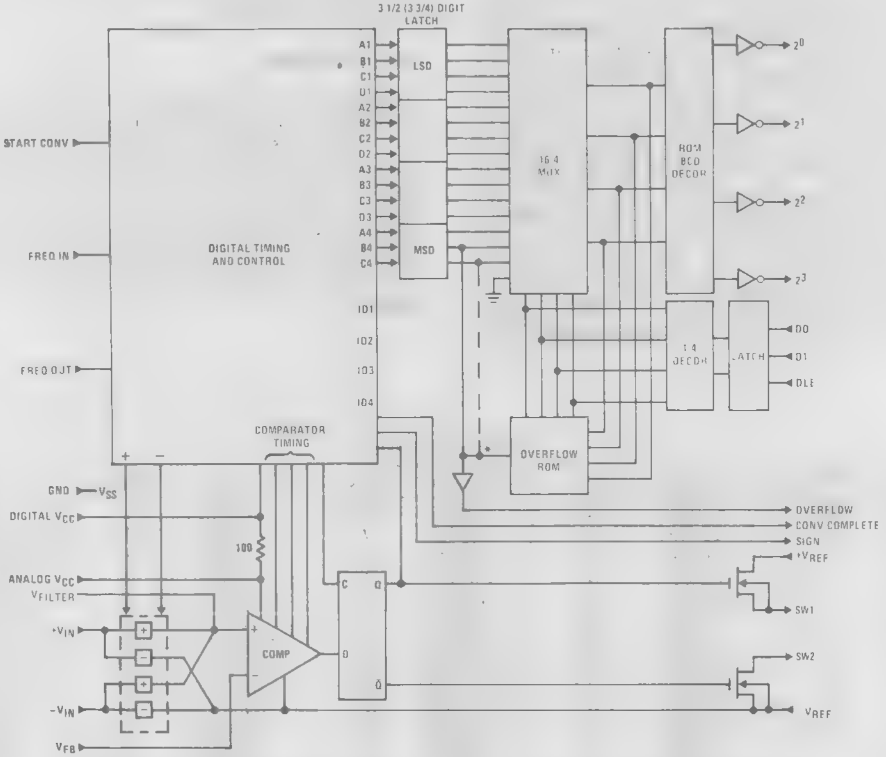


FIGURE A2. ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D) Block Diagram

For many years, military, aerospace and satellite programs have depended on bipolar transistor and integrated circuit technology in the fabrication of airborne systems. Development of bipolar technology is an outgrowth, in part, of avionics and space applications needs. Despite their relatively high immunity or resistance to high levels of both constant and burst radiation in the form of gamma rays, x-rays, cosmic rays, and so on, bipolar devices have one drawback: high power consumption, which adds to the payload of spacecraft and missiles.

In recent years, development of sophisticated space, satellite and military systems, and mission requirements has fostered an active search for a radiation hardened circuit technology that consumes less power and offers a higher degree of circuit integration on a single silicon chip. Development of metal oxide semiconductor (MOS) devices, particularly the complementary MOS (CMOS) type, seemed to promise just such an alternative. But standard CMOS devices, even those qualified to MIL-STD-38510 or JAN standards, are sensitive to relatively low radiation levels. To date, mass producible radiation hardened or resistant CMOS devices have been able to withstand only 10^5 rads (Si), while many space, satellite and missile systems require circuitry resistance levels at least ten times higher, about 10^6 rads (Si), at a minimum. Now, the problem appears to be solved. A complete line of one megarad (10^6) CMOS logic products using a mass producible radiation hardening fabrication process has been developed, the result of a two-year research effort. Devices ranging in complexity from simple gates to large scale integrated (LSI) random access memories have been hardened to radiation doses of more than 10^6 rads of constant level gamma radiation (table 1). There are 47 circuits presently available with at least 21 more to be qualified by the end of 1978. To achieve this level of radiation resistance in a mass production CMOS process, major modifications were made in the basic commercial process, relating to gate oxidation, substrate and P-tub surface concentrations, and metallization.

Bipolar vs CMOS

The inherently higher radiation resistance of bipolar over CMOS devices results from a basic difference in their structures. Bipolar devices are vertical structures. The basic elements — emitter, collector, and base — are laid down vertically, layer upon layer, by diffusion. Current flows through the bulk silicon, some distance below the silicon-silicon dioxide interface. Thus, there is some inherent protection from the interface effects of ionizing radiation in bipolar devices.

RAD Hard CMOS

Device	Series	Device	Series	Device	Series	Device	Series	Device
CD4001	A/B	CD4019	B	CD4042	B	D4075	B	MM54C04
CD4002	A	CD4020	A	CD4043	A	CD4076	B	MM54C14
CD4006	A	CD4021	A	CD4044	A	CD4081	B	MM54C86
CD4007	A	CD4022	B	CD4048	B	CD4093	B	MM54C173
CD4008	B	CD4023	A/B	CD4049	A	CD4099	B	MM54C174
CD4009	A	CD4024	B	CD4050	B	CD40106	B	MM54C192
CD4010	A	CD4025	A/B	CD4051	B	CD40174	B	MM54C193
CD4011	A	CD4027	B	CD4052	B	CD40192	B	MM54C200
CD4012	A	CD4028	B	CD4053	B	CD40193	B	MM54C901
CD4013	B	CD4029	B	CD4066	B	CD4514	B	MM54C902
CD4014	A	CD4030	A	CD4069	A	CD4515	B	MM54C903
CD4015	A	CD4031	B	CD4070	B	CD4518	B	MM54C904
CD4016	A	CD4035	B	CD4073	B	CD4520	B	MM54C906
CD4017	B	CD4040	A	CD4071	B	CD4584	B	MM54C907
CD4018	B			CD4041	A			

Table 1. Radiation Hardened CMOS Devices, Hard to 10^6 Rads (Si)

CMOS devices are surface effect devices. The equivalent operating elements, gate, source and drain, are at the surface, and the flow of current occurs horizontally across the device, very close to the silicon-silicon dioxide interface. Changes in interface parameters created by gamma or x-radiation will have a first order effect on MOS transistor performance, in contrast to a second order effect on a bipolar device. Thus the basic physics of CMOS transistor structures need to be addressed to minimize ionizing radiation effects without substantially impacting performance.

CMOS Transistor Structure

Complementary MOS, or CMOS, combines two types of MOS devices, P-channel and N-channel structures, as a functioning unit. The lower power dissipation and high stability resulting from this complementary combination is particularly attractive in the design of portable, battery powered, electronic units, or for applications where a battery provides standby power.

MOS structures, both N- and P-types, perform in two modes, enhancement and depletion. In a P-channel enhancement mode MOS device, for example, the gate controls the current flow between the source and drain. In this device, when a negative voltage is applied to the gate with respect to the source, a field is set up across the gate dielectric, producing a positively charged conductive path, a channel, between the source and the drain. This is known as an enhancement mode device because zero gate to source voltage turns off the device. In the alternative mode, depletion, current flows despite the gate voltage being zero, because sufficient field is still present within the gate to induce a conductive path between the device source and drain regions. The N-channel MOS transistor is similar to the P-channel alternative, except that positive voltage applied to the gate with respect to source induces a negatively charged conductive path between source and drain to turn the device on.

Conventional CMOS logic circuits are produced with only enhancement mode N- and P-channel devices. The process is designed to give turn on (threshold) voltage values for both types of devices which insure proper circuit performance. Figure 1 illustrates the cross section of a CMOS structure connected in a simple inverter configuration. To form the standard metal gate CMOS structure, a lightly doped P-tub is formed by diffusion into an N-type substrate with the tub becoming the substrate for the N-channel transistor. The N+ and P+ impurities are diffused into the P-tub and N-substrate to become the N- and P-channel transistors, source and drain regions, respectively. These diffusions also serve as contacting regions to the positively biased N-substrate and the normally grounded P-tub regions (V_{DD} and V_{SS} respectively).

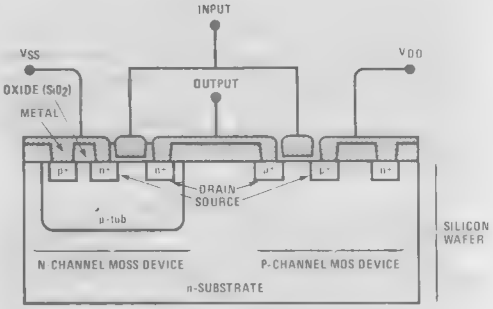


Figure 1. Cross Section of a CMOS Transistor Structure Connected in a Simple Inverter Configuration

A gate oxide is grown such that a thin film of dielectric oxide material bridges the source/drain regions over the entire circuit. Finally, contact apertures are etched to the source/drain regions and an aluminum film evaporated and etched to form gate electrodes, contacts to device terminals, and interconnection conductor lines.

Effects of Ionizing Radiation

A CMOS transistor's radiation resistance is primarily determined by formation of the gate structures in both P-channel and N-channel devices. The gate structures are used to turn the MOS devices on or off; that is, to start or stop a flow of current from the source to the drain. Ionizing radiation induces unwanted positive charge into the gate oxide structure, resulting in lowering the threshold voltage of actual circuit devices and parasitic field oxide devices by values of as much as 30V or more. In establishing a radiation hardened CMOS process, it is necessary to incorporate processing steps which minimize these radiation induced shifts in critical locations of the IC structure.

The impact of radiation induced oxide charge on operating CMOS devices is to decrease both the N-channel threshold voltage, V_{TN}, and the P-channel threshold voltage, V_{TP}. The most serious problem occurs when sufficient reduction in V_{TN} occurs to cause the N-channel device to go from enhancement to depletion mode operation. This results in excessive power supply current drain and loss of circuit functionality. The most severe stress on an N-channel device occurs when its gate is positively biased during irradiation. This causes positive charge in the oxide to be driven closer to the Si-SiO_2 interface where it is more effective in causing the P-type substrate surface to become inverted to N-type.

In normal operation, positive bias does not appear between the gate and substrate of P-channel devices since the substrate is already at the most positive circuit potential, V_{DD}. The most severe effect on P-channel devices during irradiation often occurs with zero gate to substrate bias. This stress creates Si-SiO_2 interface states which are capable of holding a positive charge with negative voltage applied to the gate. This increases the absolute value of V_{TP}, but is a much less deleterious effect on the circuit than the V_{TN} shift.

CMOS Process Modification

Gate Oxidation: To minimize both the radiation induced positive oxide charge and formation of Si-SiO_2 interface states, a dry rather than wet oxidation step is used. The gate oxide is thermally grown in a pure oxygen ambient, rather than in a water ambient, as is the case in some metal gate fabrication processes. Moreover, the gate oxide is thermally grown at 1000°C, followed by a nitrogen anneal at 850°C. This cycle has been empirically found to produce oxides having a high degree of resistance to ionizing radiation effects as well as excellent pre-radiation MOS characteristics.* Why this is so is not known exactly, and is still being studied. The need for thermally growing gate oxides at 1000°C in dry oxygen for optimal radiation hardness is one of the more intriguing aspects of this experimentally deduced cycle.

Metallization: A by-product of the E-beam aluminum evaporation process commonly used in commercial IC fabrication is soft x-radiation. This radiation produces the same type of positive charge in the gate oxide and interface states which a radiation hardened oxide should resist. Although these harmful effects in the gate oxide can be removed by a high temperature anneal cycle, subsequent exposure of the oxide to ionizing radiation results in a drastically less radiation resistant structure. Use of a non-E-beam metallization technique circumvents the problem of high threshold shifts due to irradiation under zero and negative gate bias associated with soft x-ray damage. For this reason, induction heated evaporation of aluminum is used to fabricate radiation hardened CMOS products.

Substrate and P-tub Surface Concentration: The impact of ionizing radiation on V_{TN} and V_{TP} values in a CMOS device is resolved through process modification. In anticipation of these threshold voltage shifts, radiation hardened CMOS devices are designed with the initial value of V_{TN} as high as possible and V_{TP} as close to zero as possible without sacrificing pre-radiation circuit performance. Both the substrate resistivity and the P-tub surface concentration have been modified with the initial value of V_{TN} being increased to 1.8 volts from the standard value of 1.3 volts and V_{TP} being changed from the standard −1.7 volts to −1.3 volts.

Performance Characteristics

Figures 2 and 3 illustrate the variation of post radiation V_{TN} and V_{TP} with dose. The distribution of the V_{TN} and V_{TP} data is found normal both before and after irradiation. The solid line shows the mean value of V_{TN} (or V_{TP}), and the dashed lines indicate the one standard deviation, σ, value on either side of the mean. This value, for both N- and P-channel devices, remains fairly constant with dose from the unirradiated case through 10^6 rad (Si). The values shown remain well above the 300mV V_{TN} lower limit, which, if penetrated, would lead toward N-channel depletion mode behavior and risk of losing circuit functionality and excessive supply current drain.

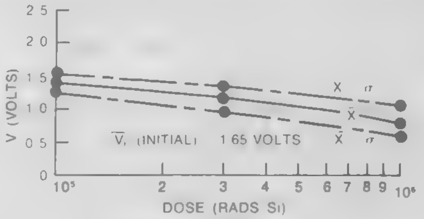


Figure 2. V_{TN} vs Dose

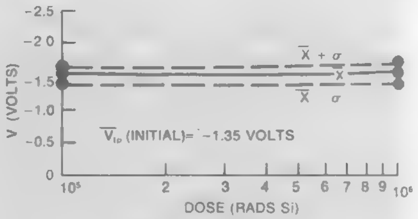


Figure 3. V_{TP} vs Dose

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*W.R. Dawes, Jr., G.F. Derbenwich and B.L. Gregory, "Process Technology for Radiation Hardened CMOS Integrated Circuits," *IEEE Journal of Solid State Circuits*, Sc-11, No. 4, p. 459, August 1976.

Figure 4 illustrates the supply quiescent current, I_{SS}, variation as a function of dose. Since I_{SS} is a function of die size, curves have been plotted for three levels of integration, SSI, MSI and LSI. In all cases, the leakage level at 10^6 rad (Si) does not increase by more than an order of magnitude from the initial value. The end point at 10^6 rad (Si) for LSI of 30µA is far below the high temperature (125°C) specification of 600µA. The same conclusion can be drawn for MSI and SSI.

Figure 5 illustrates circuit propagation delay, t_{PD}, as a function of dose. The plot, similar to figure 4, is divided into three categories (LSI, MSI, SSI). The propagation delay value at 10^6 rads (Si) for all three categories increased roughly 20-25% from the initial value, well within desirable operating tolerances. In figures 2 through 5, the biasing conditions during irradiation were: V_{DD} = 10V, V_{IN} = 10V, and V_{SS} = 0V.

Hardness Assurance and Reliability

A sampling plan has been established to ensure radiation hardness to 10^5 and 10^6 rads, since ionizing radiation degrades IC performance and cannot be used for 100% screening. In addition, an intensive program to evaluate the reliability characteristics of radiation hardened CMOS circuits is underway. 476 devices of the CD4001 AD/RH, CD4011 AD/RH, and MM54C200D/RH types have been tested and have operated for over 800,000 hours without a failure. This corresponds to a failure rate less than or equal to 0.125%/1000 hours at 125°C with a 60% confidence level.

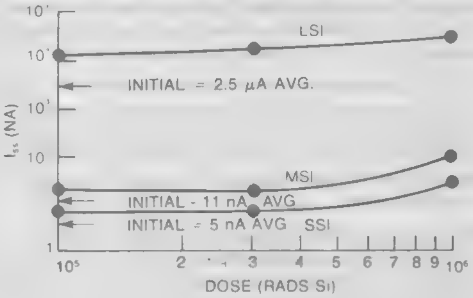


Figure 4. I_{SS} vs Dose

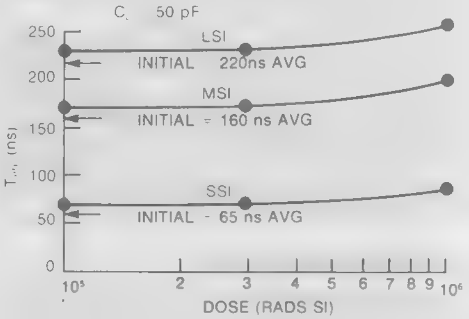


Figure 5. t_{PD} vs Dose

Using the ADC0808/ADC0809 8-Bit µP Compatible A/D Converters with 8-Channel Analog Multiplexer

National Semiconductor
Application Note 247
Larry Wakeman
September 1980

INTRODUCTION

The ADC0808/ADC0809 Data Acquisition Devices (DAD) implement on a single chip most of the elements of the standard data acquisition system. They contain an 8-bit A/D converter, 8-channel multiplexer with an address input latch, and associated control logic. These devices provide most of the logic to interface to a variety of microprocessors with the addition of a minimum number of parts.

These circuits are implemented using a standard metal-gate CMOS process. This process is particularly suitable to applications where both analog and digital functions must be implemented on the same chip.

These two converters, the ADC0808 and ADC0809, are functionally identical except that the ADC0808 has a total unadjusted error of ± 1/2 LSB and the ADC0809 has an unadjusted error of ± 1 LSB. They are also related to their big brothers, the ADC0816 and ADC0817 expandable 16 channel converters. All four converters will typically do a conversion in ~100 µs when using a 640 kHz clock, but can convert a single input in as little as ~50 µs.

1.0 FUNCTIONAL DESCRIPTION

The ADC0808/ADC0809, shown in *Figure 1*, can be functionally divided into 2 basic subcircuits. These two subcircuits are an analog multiplexer and an A/D converter. The multiplexer uses 8 standard CMOS analog switches to provide for up to 8 analog inputs. The switches are selectively turned on, depending on the data latched into a 3-bit multiplexer address register.

The second function block, the successive approximation A/D converter, transforms the analog output of the multiplexer to an 8-bit digital word. The output of the multiplexer goes to one of two comparator inputs. The other input is derived from a 256R resistor ladder, which is tapped by a MOSFET transistor switch tree. The converter control logic controls the switch tree, funneling a particular tap voltage to the comparator. Based on the result of this comparison, the control logic and the successive approximation register (SAR) will decide whether the next tap to be selected should be higher or lower than the present tap on the resistor ladder. This algorithm is executed 8 times per conversion, once every 8 clock periods, yielding a total conversion time of 64 clock periods.

When the conversion cycle is complete the resulting data is loaded into the TRI-STATE® output latch. The data in the output latch can then be read by the host system any time before the end of the next conversion. The TRI-STATE capability of the latch allows easy interface to bus oriented systems.

The operation of these converters by a microprocessor or some control logic is very simple. The controlling device first selects the desired input channel. To do this, a 3-bit channel address is placed on the A, B, C input pins; and the ALE input is pulsed positively, clocking the address into the multiplexer address register. To begin the conversion, the START pin is pulsed. On the rising edge of this pulse the internal registers are cleared and on the falling edge the start conversion is initiated.

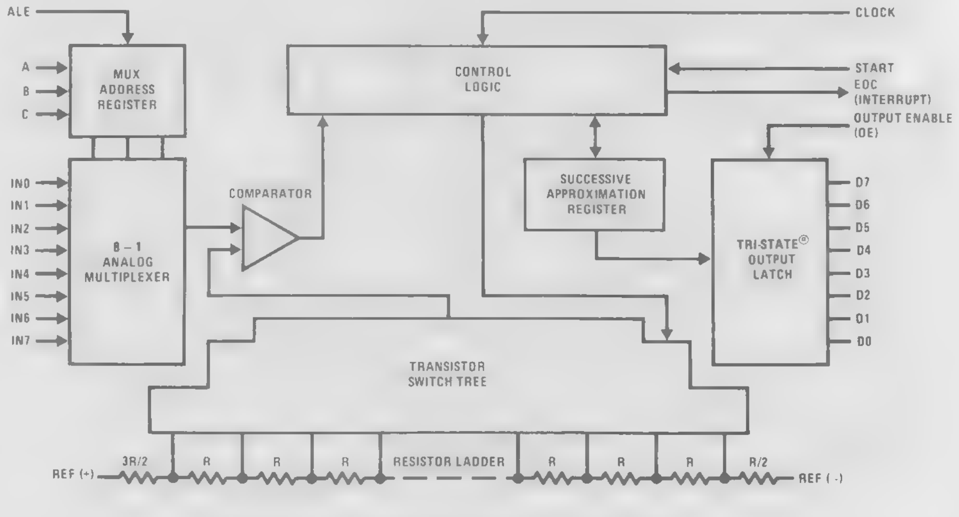


FIGURE 1. ADC0808/ADC0809 Functional Block Diagram

TRI-STATE® is a registered trademark of National Semiconductor Corp

As mentioned earlier, there are 8 clock periods per approximation. Even though there is no conversion in progress the ADC0808/ADC0809 is still internally cycling through these 8 clock periods. A start pulse can occur any time during this cycle but the conversion will not actually begin until the converter internally cycles to the beginning of the next 8 clock period sequence. As long as the start pin is held high no conversion begins, but when the start pin is taken low the conversion will start within 8 clock periods.

The EOC output is triggered on the rising edge of the start pulse. It, too, is controlled by the 8 clock period cycle, so it will go low within 8 clock periods of the rising edge of the start pulse. One can see that it is entirely possible for EOC to go low before the conversion starts internally, but this is not important, since the positive transition of EOC, which occurs at the end of a conversion, is what the control logic is looking for.

Once EOC does go high this signals the interface logic that the data resulting from the conversion is ready to be read. The output enable (OE) is then raised high. This enables the TRI-STATE outputs, allowing the data to be read. *Figure 2* shows the timing diagram.

2.0 ANALOG INPUTS

2.1 Ratiometric Inputs

The arrangement of the REF(+) and REF(−) inputs is intended to enable easy design of ratiometric converter systems. The REF inputs are located at either end of the 256R resistor ladder and by proper choice of the input voltages several applications can be easily implemented.

Figure 3 shows a typical input connection for ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full-scale value. In other words, the tranducer's absolute output value is of no particular concern but the ratio of the output to the full-scale is of great importance. For example, the potentiometric displacement transducers of *Figure 3* have this feature. When the wiper is at midscale, the output voltage is $V_O = V_F \times$ (Wiper Displacement) $= V_F \times 0.5$. This enables the use of much less accurate and less expensive references. The important consideration for this reference is noise. The reference must be "glitch free" because a voltage spike during a conversion cycle could cause conversion inaccuracies.

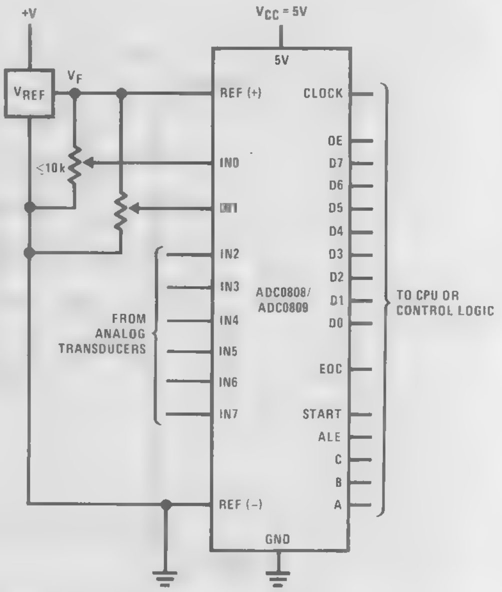


FIGURE 3. Ratiometric Converter with Separate Reference

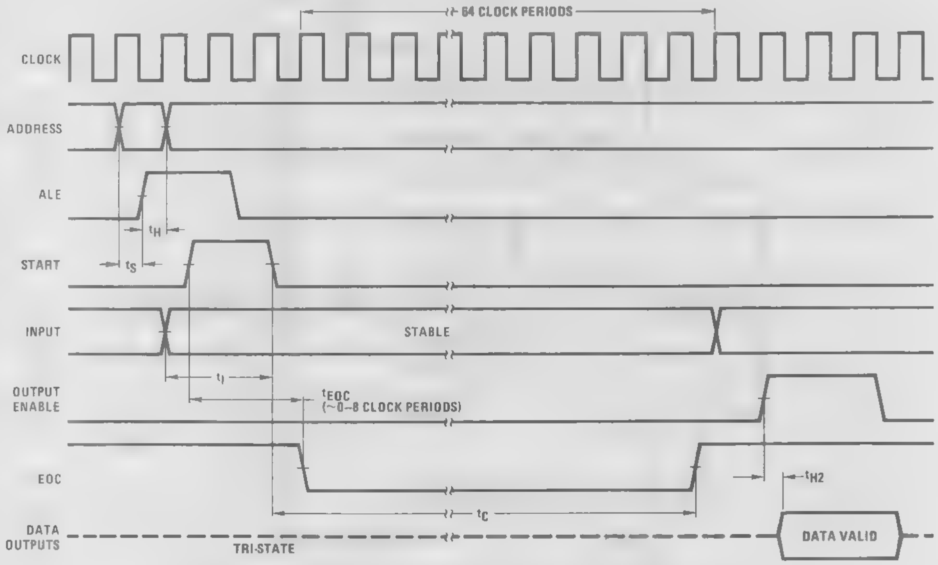


FIGURE 2. ADC0808/ADC0809 Timing Diagram

Since highly accurate references aren't required it is possible to use the system power supply as a reference, as shown in *Figure 4*. If the power supply is to be used in this manner supply noise must be kept to a minimum to preserve conversion accuracy. If possible the supply should be well bypassed and separate reference and supply PC board traces, originating as close as possible to the power supply or regulator, should be used. This is illustrated in *Figure 4*.

External accessibility of both ends of the resistor ladder enables several variations on these basic connections, and are shown in *Figures 5 and 6*. The magnitude of the reference voltage, $V_{REF} = REF(+) - REF(-)$, can be varied from about ~0.5V to V_{CC}, but the center voltage must be maintained within ±0.1V of $V_{CC}/2$. This constraint is due to the design of the transistor switch tree, which could malfunction if the offset from center scale becomes excessive. Variation of the reference voltage can sometimes eliminate the need for external gain blocks to scale the input voltage to a full-scale range of 5V.

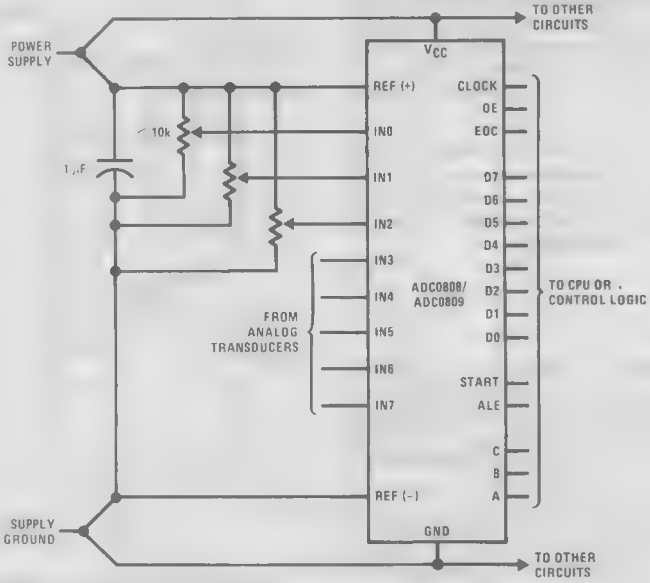


FIGURE 4. Ratiometric Converter with Power Supply Reference

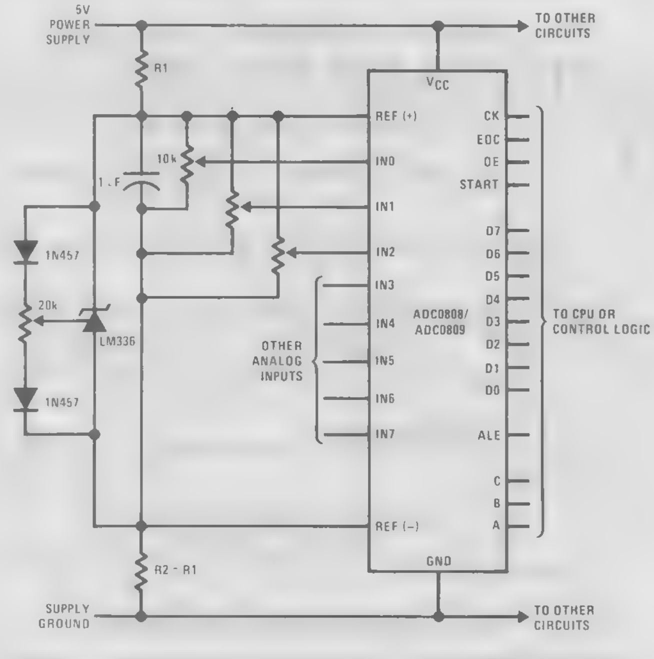


FIGURE 5. Mid-Supply Centered Reference using LM336 2.5V Reference

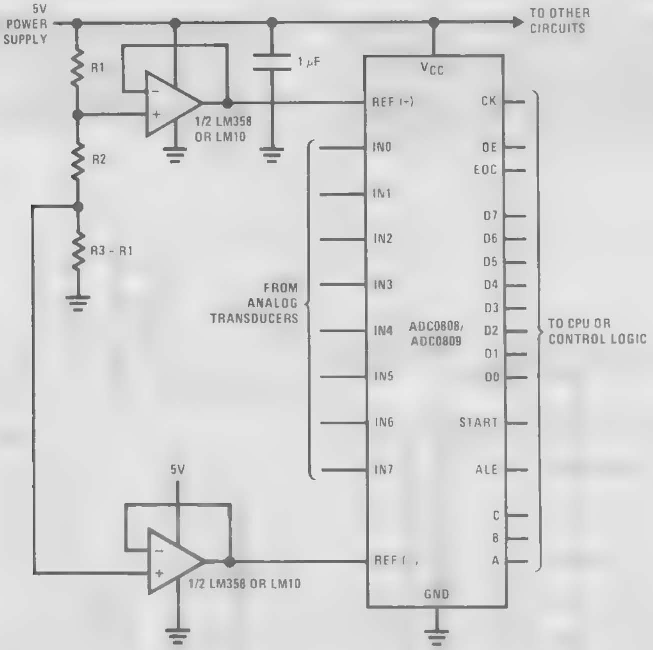


FIGURE 6. Mid-Supply Centered Reference using Buffered Resistors

Figure 5 shows a center referencing technique, using two equal resistors to symmetrically offset an LM336 2.5V reference, from both supplies. The offset from either supply is:

$$V_{OFF} = \frac{V_{CC} - V_{REF}}{2} = 1.25V$$

These resistors should be chosen so that they limit current through the LM336 to a reasonable value, say 5 mA. The total resistor current is:

$$I_R = I_{REF} + I_{LADDER} + I_{TRAN}$$

where I_{LADDER} is the 256R ladder current, I_{TRAN} is the current through all the transducers, and I_{REF} is the current through the reference. R1 and R2 should be well matched and track each other over temperature.

For odd values of reference voltage, the reference could be replaced by a resistor, but due to loading and temperature problems, these resistors should be buffered to the REF(+) and REF(−) inputs, *Figure 6*. The power supply must be well bypassed as supply glitches would otherwise be passed to the reference inputs. The reference voltage magnitude is:

$$V_{REF} = V_{DD} \left(\frac{R2}{2R1 + R2}\right) \quad R3 = R1$$

There are several op amps that can be used for buffering this ladder. Without adding another supply, an LM358 could be used if the REF(+) input is not to be set above 3.5V. The LM10 can swing closer to the positive supply and can be used if a higher, $V_{REF(+)}$ voltage is needed.

As the REF(+) to REF(−) voltage decreases the incremental voltage step size decreases. At 5V one LSB represents ~20 mV, but at 1V, one LSB represents ~4 mV. As the reference voltage decreases, system noise will become more significant so greater precaution should be enforced at lower voltages to compensate for system noise; i.e., adequate supply and reference bypassing, and physical as well as electrical isolation of the inputs.

2.2 Absolute Analog Inputs

The ADC0808/ADC0809 may have been designed to easily utilize ratiometric transducers, but this does not preclude the use of non-ratiometric inputs. A second type of input is the absolute input. This is one which is independent of the reference. This implies that its *absolute* numerical voltage value is very critical, and to accurately measure this voltage the accuracy of the reference voltage becomes equally critical. The previous designs can be modified to accommodate absolute input signals by using a more accurate reference. In *Figure 4* the power supply reference could be replaced by an LM336-5.0 reference. R1 and R2 of *Figure 6*, and R1 and R3 of *Figure 7* may have to be made more accurately equal.

In some small systems it is possible to use the precision reference as the power supply as shown in *Figure 7*. An unregulated supply voltage >5V is required, but the LM336-5.0 functions as both a regulator and reference. The dropping resistor R must be chosen so that, for the whole range of supply currents needed by the system, the LM336-5.0 will stay in regulation. As in *Figure 4* separate supply and reference traces should be used to maintain a noiseless supply.

If the system requires more power, an op amp can be used as shown in *Figure 8* to isolate the reference and boost the supply current capabilities. Here again, a single unregulated supply is required.

2.3 Differential Inputs

Differential measurements can be obtained by playing a little software trick. This simply involves sequentially converting two channels then subtracting the two results. For example, if the difference voltage between channel 1 and 2 is required, merely convert channel 1 and read the result. Then convert channel 2, input the result, and subtract it from the first result. *(See Figure 9.)* When using this procedure, both input signals must be stable throughout both conversion times or the end result will be incorrect. One way to get around this is to use two sample/holds which are sampled at the same time.

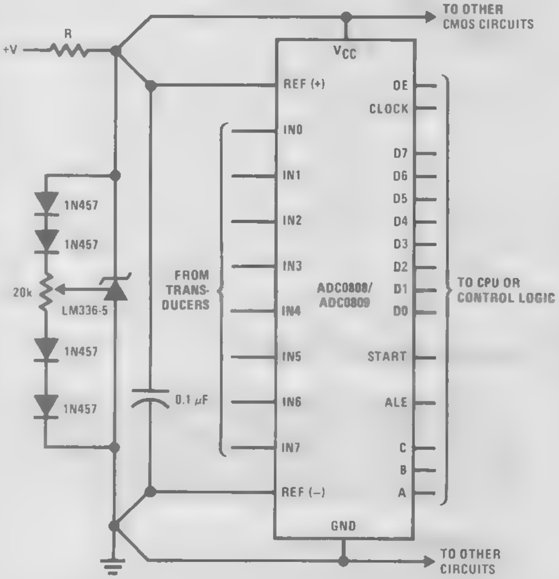


FIGURE 7. Precision Reference used as a Power Supply

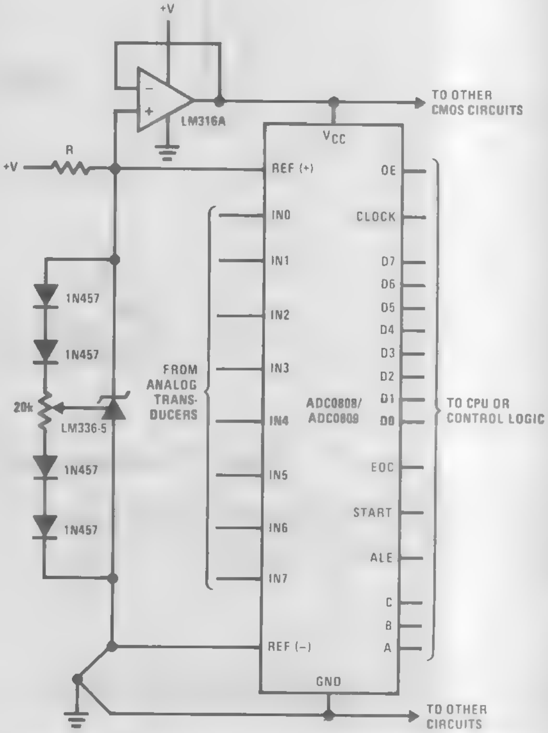


FIGURE 8. Precision Reference Buffered for Power Supply

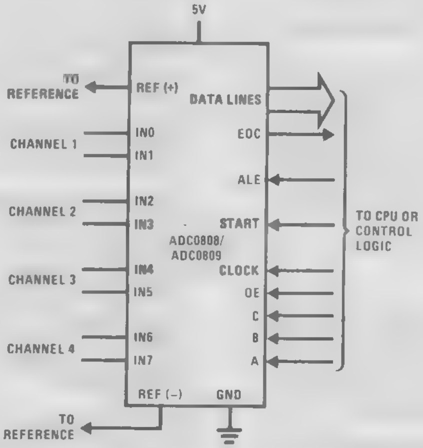


FIGURE 9. Software Controlled Differential Converter

A second method is to use two chips to convert a differential channel, *Figure 10*. Typically each channel 1 would be connected to opposite sides of the differential input. Both converters are started simultaneously. When both converters' EOC outputs go high the output of the AND gate will go high indicating that the data is ready to be read.

The circuit in *Figure 10* can be slightly modified to provide increased data throughput by using two converters in a parallel data acquisition scheme. *Figure 11* shows this circuit in which all the input channels are connected in pairs through LF398 monolithic sample/holds. Under normal operation a sample/hold is accessed through an MM74C42 which will pulse an MM74C221, generating a sample pulse. After a sample/hold is done sampling the signal, the appropriate channel is started. If this process is alternated between two converters the sample rate can be doubled.

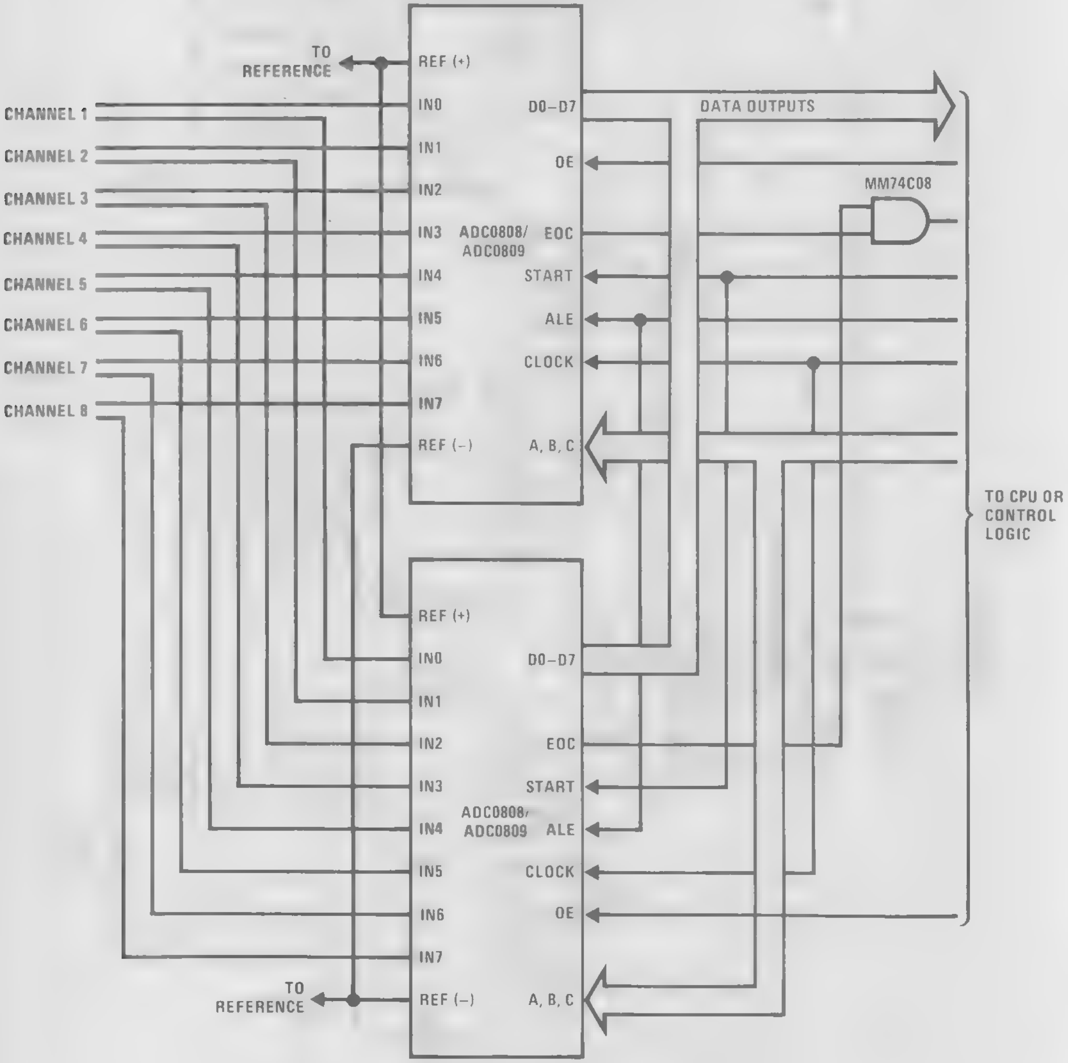


FIGURE 10. Dual Converter Differential Circuit

2.4 Analog Input Considerations

Analog inputs into the ADC0808/ADC0809 can handle any input signal that is maintained within the supply limits, but some careful consideration must be given to the output impedance of the transducer or buffer. Using transducers with large source impedances can cause errors due to comparator input currents.

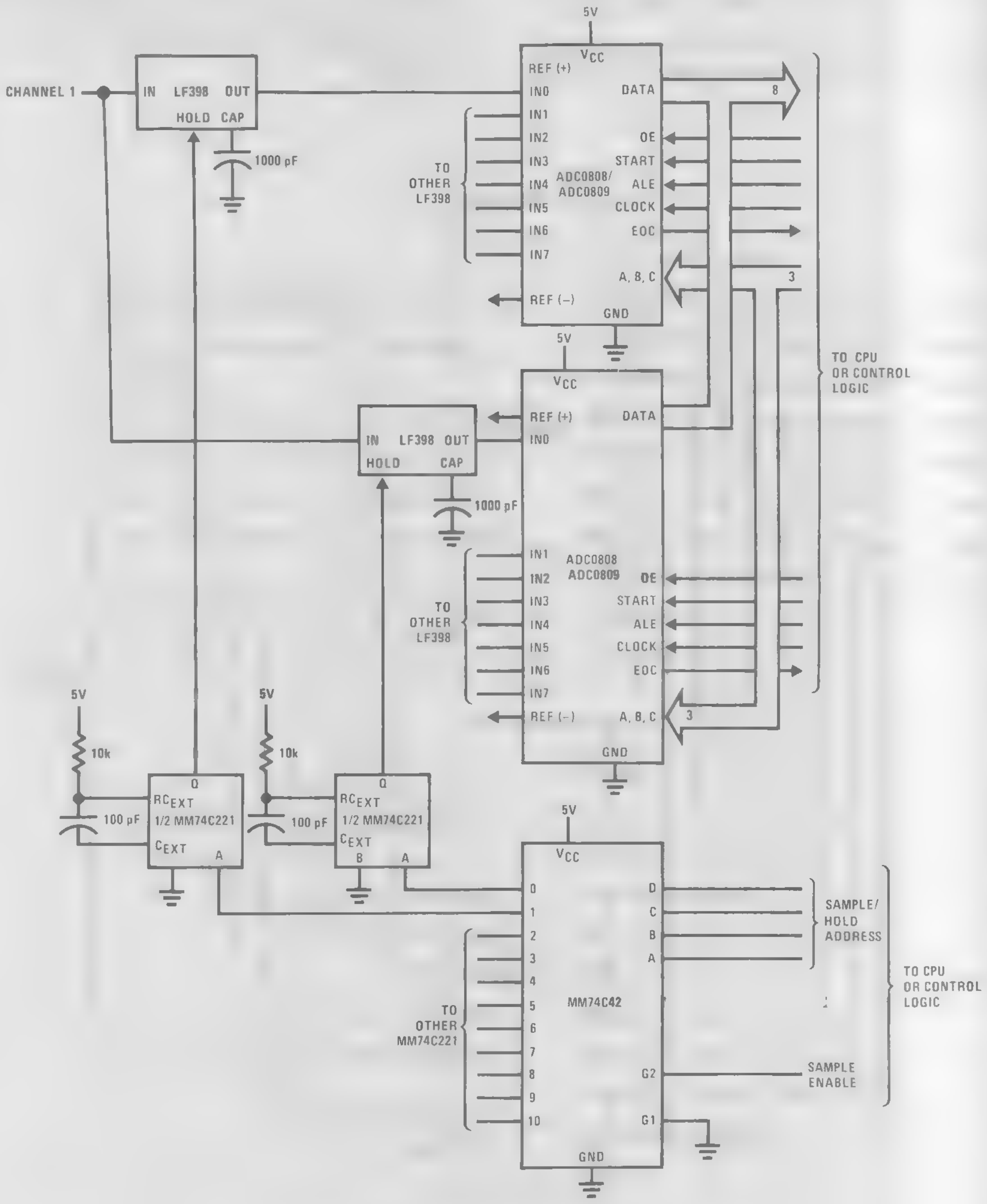


FIGURE 11. Parallel Data Acquisition with Sample/Holds

charged up to the input voltage. It then samples the ladder and discharges the capacitor. The net charge difference is determined by a modified inverter chain and results in a 1 or 0 state at the output.

Eight samples are made per conversion, resulting in eight spikes of varying magnitude on the input.

If the source resistance is large, it adds to the RC time constant of the switched capacitor which will inhibit the input from settling properly, causing errors. As one might expect, the maximum source resistance allowable for accurate conversions is inversely proportional to clock frequency. This resistance should be ≤ 1 kΩ at 1.2 MHz and ≤ 2 kΩ at 640 kHz. If a potentiometer-type ratiometric transducer is used it should be ≤ 5 kΩ at 1.2 MHz and ≤ 10 kΩ at 640 kHz.

If large source impedances are unavoidable (≥ 2 kΩ at 640 kHz), the transient errors can be reduced by placing a bypass capacitor ≥ 0.1 μF from the analog inputs to ground. This will reduce the spikes to a small average current which will cause some error as well, but this can be much less than the error otherwise incurred. The maximum voltage error for a potentiometer input with a bypass capacitor added is:

$$V_{ERR} \approx \left[\frac{R_{POT}}{5}(I_{IN})\frac{Ck}{640\text{ kHz}}\right]V$$

where R_{POT} = total potentiometer resistance; I_{IN} = maximum input current at 640 kHz, 2 μA; and Ck = clock frequency.

For standard buffer source impedance the maximum error is:

$$V_{ERR} = \left[I_{IN}R_S\left(\frac{Ck}{640\text{ kHz}}\right)\right]V$$

where R_S = buffer source resistance; I_{IN} = the maximum input current at 640 kHz, 2 μA; and Ck = clock frequency.

3.0 MICROPROCESSOR INTERFACING

The ADC0808/ADC0809 converters were designed to interface to most standard microprocessors with very little external logic, but there are a few general requirements which must be considered to ensure proper converter operation.

systems extra buffering may be necessary. The EOC output is not quite as powerful as the data outputs, but normally it is not bussed like the data outputs.

The converter inputs are standard CMOS compatible inputs. When TTL outputs are connected to any of the digital inputs a pull-up resistor should be tied from the TTL output to V_{CC}, ~ 5 kΩ. This will ensure that the TTL will pull-up above 3.5V.

Usually the converter clock will be derived from the microprocessor system clock. Some slower microprocessor clocks can be used directly, but at worst a few divider stages may be necessary to divide microprocessor clock frequencies above 1.2 MHz to a usable value.

The timing of the START and ALE pulses relative to channel selection and signal stability can be critical. The simplest approach to microprocessor interfaces usually ties START and ALE together. When these lines are strobed the address is strobed into the address register and the conversion is started. The propagation delay from ALE to the comparator input of the selected input signal is about ~3.0 μs (input source resistance << 1 kΩ). If the start pulse is very short the comparator can sample the analog input before it is stable. When using a slow clock ≤500 kHz the sample period of the comparator input is long enough to allow this delay to settle out.

If the ADC0808/ADC0809 clock is >500 kHz, a delay between the START and ALE pulses is required. There are three basic methods to accomplish this. The first possibility is to design the microprocessor interface so that the START and ALE inputs are separately accessible. This is simple if some extra address decoding is available. Separate accessibility of the START and ALE pins allows the microprocessor, via software, to set the delay time between the START and ALE pulses.

If extra decoding is not available, then START and ALE could be tied together. To obtain the proper delay, the microprocessor would cause START/ALE to be strobed twice by executing the load and start instruction twice. The first time this instruction is executed, the new channel address is loaded and the conversion is started. The second execution of this instruction will reload the same channel address and restart the conversion. But since the multiplexer address register contents are unchanged the selected analog input will have already settled by the time the second instruction is issued. Actual implementations of these ideas are shown in following sections.

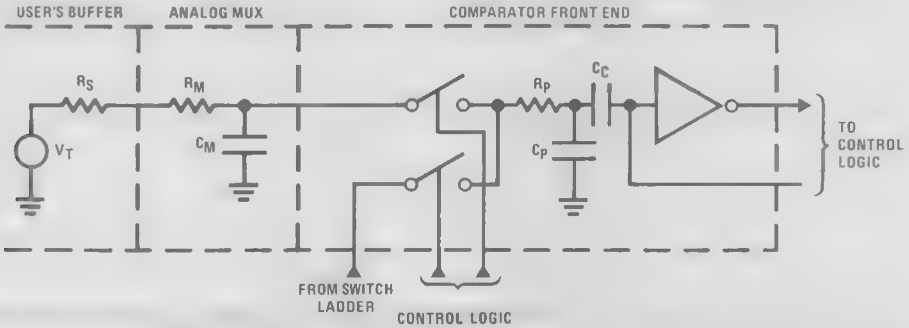


FIGURE 12. Analog Multiplexer and Comparator Input Model

A third possibility when ALE and START are tied together is to stretch the microprocessor derived ALE/START pulse by inserting a one-shot at these inputs and creating a positive pulse $>3\ \mu s$. Since ALE loads the multiplexer register on the positive going edge of the pulse and START begins the conversion on the falling edge, the width of the pulse sets the ALE to START delay time.

Most microprocessor interfaces would be designed such that a START pulse is issued by a memory or I/O write instruction, although a memory or I/O read can be used. The ALE strobe on the other hand, requires a write by the CPU when A, B, and C are connected to the data bus, and could use a read instruction if A, B, and C are connected to the address bus, but the software could get confusing. The logic to derive the OE strobe must be connected to the microprocessor so that a memory or I/O read instruction will cause OE to be pulsed. A read is required since the ADC0808/ADC0809 data must be read.

3.1 Interfacing to the INS8080

The simplest interface would contain no address decoding, which may seem unreasonable; but if the system ports are I/O mapped, up to 8 of them can be connected to the CPU with no decoding. Each of the 8 I/O address lines would serve as a simple port enable line which would be gated with read and write strobes to select a particular port. This scheme is shown in *Figure 13.* A7 is the address line used and, whenever it is zero and an I/O read or write is low, the port is accessed. This implementation shows A, B, C connected to D0, D1, D2 causing the information on the data bus to select the channel, but A, B, and C could be connected to the address bus, with a loss of only 3 ports. Both decoding schemes are tabulated in *Figure 14.* (Remember A, B, C inputs are only valid when selecting a channel to convert, and are not used to read data.)

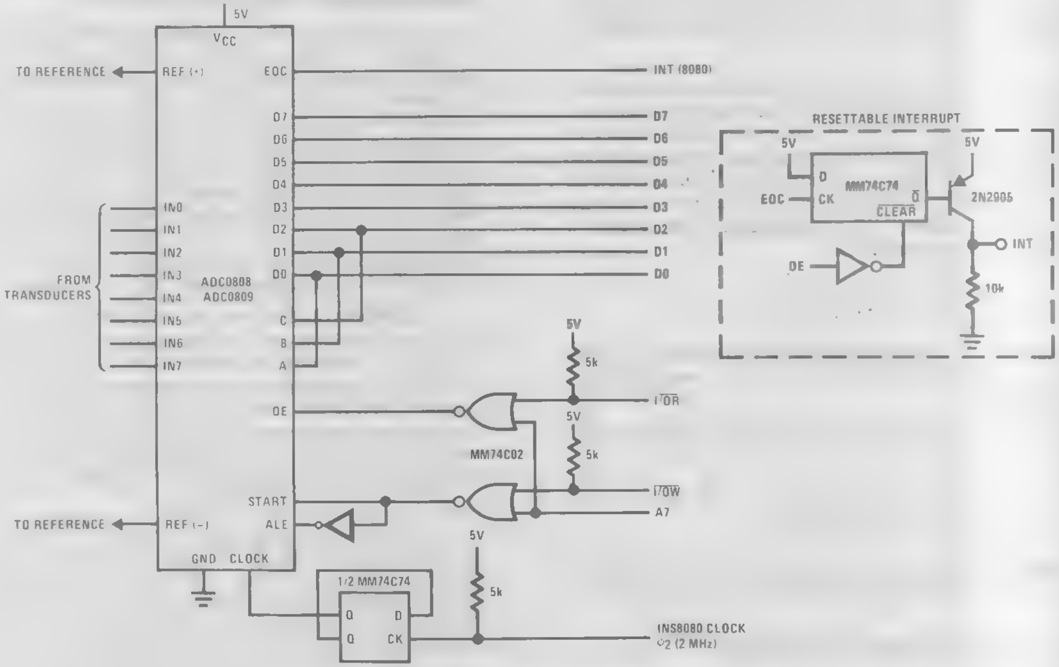


FIGURE 13. Minimum INS8080/INS8224/INS8228 Interface

A7	A6	A5	A4	A3	A2	A1	A0	D2	D1	D0	Output Port Description
1	1	1	1	1	1	1	0	X	X	X	Spare Port
1	1	1	1	1	1	0	1	X	X	X	Spare Port
1	1	1	1	1	0	1	1	X	X	X	Spare Port
1	1	1	1	0	1	1	1	X	X	X	Spare Port
1	1	1	0	1	1	1	1	X	X	X	Spare Port
1	1	0	1	1	1	1	1	X	X	X	Spare Port
1	0	1	1	1	1	1	1	X	X	X	Spare Port
0	1	1	1	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	1	1	1	Channel 7 Port

FIGURE 14a. Write Address Decoding for INS8080 Output Ports (A, B, C Connected to D0, D1, D2)

A7	A6	A5	A4	A3	A2	A1	A0	Output Port Description
0	1	1	1	1	0	0	0	Channel 0 Port
0	1	1	1	1	0	0	1	Channel 1 Port
0	1	1	1	1	0	1	0	Channel 2 Port
0	1	1	1	1	0	1	1	Channel 3 Port
0	1	1	1	1	1	0	0	Channel 4 Port
0	1	1	1	1	1	0	1	Channel 5 Port
0	1	1	1	1	1	1	0	Channel 6 Port
0	1	1	1	1	1	1	1	Channel 7 Port
1	1	1	1	0	X	X	X	Spare Port
1	1	1	0	1	X	X	X	Spare Port
1	1	0	1	1	X	X	X	Spare Port
1	0	1	1	1	X	X	X	Spare Port

X = don't care

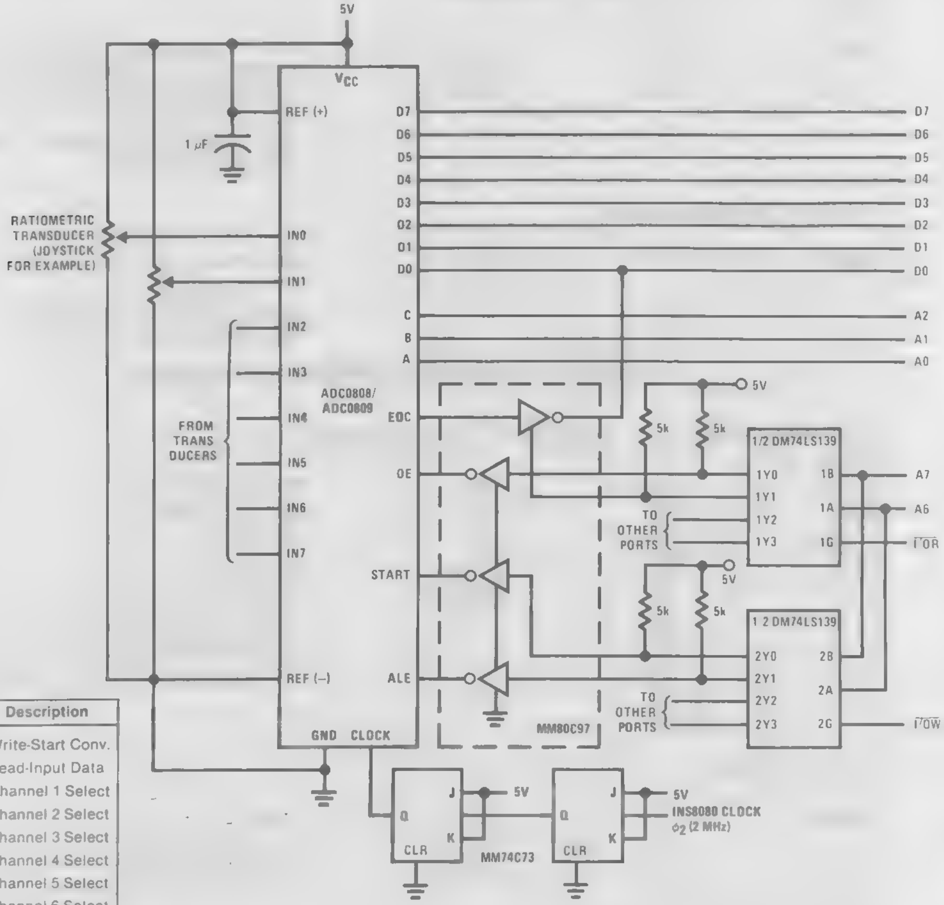
FIGURE 14b. Modified Write Address Decoding for INS8080 Output Ports (A, B, C Connected to A0, A1, A2)

Two LSTTL NOR gates are used to generate to the ADC0808/ADC0809 read/write strobes. When the INS8080 writes to the ADC0808/ADC0809 the ALE and START inputs are strobed, loading and starting the conversion. When the CPU reads the ADC0808/ADC0809 the OE input is taken high, and the data outputs are enabled.

Figure 13 implements a simple interrupt concept where EOC is tied directly to the INS8080 interrupt input. When the INS8228 is used and the INTA pin is tied high through a 1 kΩ resistor, the interrupt will cause a restart, RST, instruction to be executed, which will then cause a jump to a restart vector and execution of the interrupt routine. If a very simple multi-interrupt system is desired, a wire OR'ed configuration employing resettable latches as shown in *Figure 13's* inset can be used. In this simple design the MM74C74 is reset when the ADC0808/ADC0809 data is read. If more complicated interrupt structures are required, then an interrupt controller is usually the best solution.

The I/O port address structure for *Figure 13's* implementation is shown in *Figure 14a*. If the A, B, C inputs are tied to A0, A1, A2 inputs the port structure is as shown in *Figure 14b*. The later method makes each channel look like a separate port address whereas, if A, B, C are tied to the data bus the ADC0808/ADC0809 looks like one start conversion port address, whose channel is selected by the 3-bit status word written to it on the data bus.

Figure 15 shows a slightly more complex interface, where the address is partially decoded by a DM74LS139, dual 2-4 line decoder which creates the read and write strobes to operate the converter. This design interfaces to the processor in a polled type of interface. An MM80C97 TRI-STATE® buffer is used to buffer the EOC line to the data bus, as well as provide the correct level for the START, ALE, and OE pulses. The converter clock is a divided INS8080 system clock.



Address A7-A0	Description
0 0 X X X X X X	Write-Start Conv.
0 0 X X X X X X	Read-Input Data
0 1 X X X 0 0 0	Channel 1 Select
0 1 X X X 0 0 1	Channel 2 Select
0 1 X X X 0 1 0	Channel 3 Select
0 1 X X X 0 1 1	Channel 4 Select
0 1 X X X 1 0 0	Channel 5 Select
0 1 X X X 1 0 1	Channel 6 Select
0 1 X X X 1 1 0	Channel 7 Select
0 1 X X X 1 1 1	Channel 8 Select
0 1 X X X X X X	Read-Input $\overline{\text{EOC}}$

FIGURE 15. INS8080/INS8224/INS8228 Interface using Partial Decoding

Typically, the software to use *Figure 15* would first select the desired channel by writing the channel address to the ALE port address, 01XXXCBA, where X = don't care, and CBA is the channel address. Next the conversion is started by writing to the START address, 00XXXXXX. Now the processor must wait a few instruction cycles to allow EOC to fall. Once EOC falls, its status can be checked by reading the EOC line, address 01XXXXXX. When the EOC line is detected high again (a low on DO), the data can be read by accessing the OE port, address 00XXXXXX. As in the previous example the A, B, C inputs can be tied to D0, D1, D2 rather than A0, A1, A2, so that the information on the data bus selects the channel to be converted. *Figure 15* can be connected in an interrupt mode by incorporating the interrupt flip-flop of *Figure 13.*

A few typical utility routines to operate the ADC0808/ADC0809 application in *Figure 13* are shown in *Figure 16a*. These routines assume that the resettable interrupt flip-flop is used. *Figure 16b* illustrates some typical polled I/O routines for *Figure 15*. Notice that in *Figure 16a* the OUT START1 instruction is executed twice to allow the analog input signal to settle as discussed earlier.

```
;
; START CONVERSION (A, B, C CONNECTED TO D0, D1, D2)
;
 CHANN1          EQU          7
 START1          EQU          7FH
 DATA            EQU          7FH
;
 START:          LDA          CHANN1          ; LOAD CHANNEL ADDRESS INTO ACE
                 OUT          START1          ; STORE IT TO ADC0808/ADC0809 AND START
                 OUT          START1          ; RESTART ADC0808/ADC0809 TO ACCOUNT FOR
                                              ; MULTIPLEXER DELAY
                 EI                           ; ENABLE INTERRUPTS IF NOT ALREADY
                 —            —               ; PROCESS PROGRAM

; INTERRUPT HANDLER ROUTINE
;
 INTRP:          IN           DATA            ; READ DATA AND RESET INTERRUPT
                 —            —               ; PROCESS DATA
                 EI                           ; ENABLE INTERRUPTS IF DESIRED
                 RET                          ; RETURN TO MAIN PROGRAM
```

FIGURE 16a. Typical 8080 Resettable Interrupt I/O Routines

```
;
; START CONVERSION (A, B, C CONNECTED TO A0, A2, A3) AND POLL EOC
; (FIGURE 15)
 SELECT          EQU          40H             ; SELECT CHANNEL 0
 START           EQU          00H             ; START CONVERTER
 EOCIN           EQU          40H             ; READ EOC
 DATA            EQU          00H             ; READ DATA
 START:          OUT          SELECT          ; SELECT CHANNEL
                 OUT          START           ; START CONVERSION
                 NOP                          ; INSERT INSTRUCTIONS TO WAIT 0-8
                 NOP                          ; CLOCK PERIODS OF ADC0808/ADC0809 CLOCK
                 NOP                          ; FOR EOC TO DROP (8 NOPs MINIMUM)
                 NOP
                 NOP

; READ AND TEST EOC
;
 STATUS:         IN           EOCIN           ; INPUT EOC BIT
                 ANI          01H             ; MASK OUT OTHER BITS
                 JZ           READY           ; IF INPUT BIT IS ZERO JUMP READY
                 —            —               ; ELSE CONTINUE EXECUTING PROGRAM
; OR
; CONTINUOUS POLLING ROUTINE

 STAT 2:         IN           EOCIN           ; INPUT EOC STATUS BIT
                 ANI          01H             ; MASK OUT ALL BITS BUT D0
                 JNZ          STAT 2          ; JUMP TO TRY AGAIN IF NOT READY
 READY:          IN           DATA            ; IF READY INPUT DATA
                 —            —               ; CONTINUE EXECUTING PROGRAM
```

FIGURE 16b. Typical 8080 Polled I/O Routines for ADC0808/ADC0809

The application in *Figure 17* uses a 6-bit bus comparator and a few gates to decode a read and write strobe. Viewed from the CPU this interface looks like a bidirectional data port whose address is set by the logic levels on the T_n inputs of the DM8131 comparator. When data is written to the ADC0808/ADC0809 the 3 least significant bits on the address bus define the channel to be converted. The rest of the bits are decoded to provide the START and ALE strobes. When the conversion is completed EOC sets the interrupt flip-flop, and when the data is read the interrupt is reset.

Both the decoder and the bus comparator methods of address decoding have their own advantages. Bus comparators will more completely decode addresses but are capable of only a limited number of port strobes. Decoders, on the other hand, provide less decoding but more port strobes. There is a trade off for minimum parts systems as far as which route to go, and it will depend on the CPU and type of system.

3.2 Interfacing to the 6800

The ADC0808/ADC0809 easily interface to more than one microprocessor. The 6800 can also be used to control the converter. The 6800 has no separate I/O address space so all I/O transfers must be memory mapped. In general more address decoding logic is required to ensure that the I/O ports don't overlap existing memory. For small systems a partial address decoding scheme is shown in *Figure 18*. Generally, if several ports are desired, a small block of memory would be set aside, as is accomplished by the DM8131. *Figure 18* also illustrates a typical 6800 interrupt scheme using a flip-flop and open collector transistor. The interrupt is reset when the data is read. If more ports are needed, a decoder could be added as shown in *Figure 19*. *Figure 19* also illustrates a polled I/O mode using TRI-STATE® buffer to gate EOC onto the data bus. As with the INS8080 the A, B, C inputs of the ADC0808/ADC0809 can be connected to the address bus or the data bus.

The 6800 differs from the INS8080 in that the 6800 has a single read/write (R/$\overline{W}$) strobe and a valid memory address (VMA), whereas the INS8080 has separate read and write strobes ($\overline{I/OR}$ and $\overline{I/OW}$). Normally, to obtain a read pulse, VMA, R/$\overline{W}$ and ϕ_2 are gated together and, for a write, R/$\overline{W}$ is inverted. ϕ_2 is the 6800 phase 2 system clock. Also notice that the 6800 $\overline{INT}$ interrupt input is active low. This enables a standard wired-OR open collector design to be implemented.

Figure 20 illustrates some typical 6800 software utility routines for either polled or interrupt interfaces. Again notice double start instructions.

3.3 Z80 Interface

Interfacing the Z80 to the ADC0808 is much the same as interfacing to an INS8080/INS8224/INS8228 CPU group. CPU instruction timing is very similar, except the read/write control signals are slightly different. Instead of the $\overline{I/OW}$ write strobe there is the $\overline{IOREQ}$ and $\overline{WR}$ and instead of $\overline{I/OR}$, $\overline{IOREQ}$ and $\overline{RD}$ are supplied.

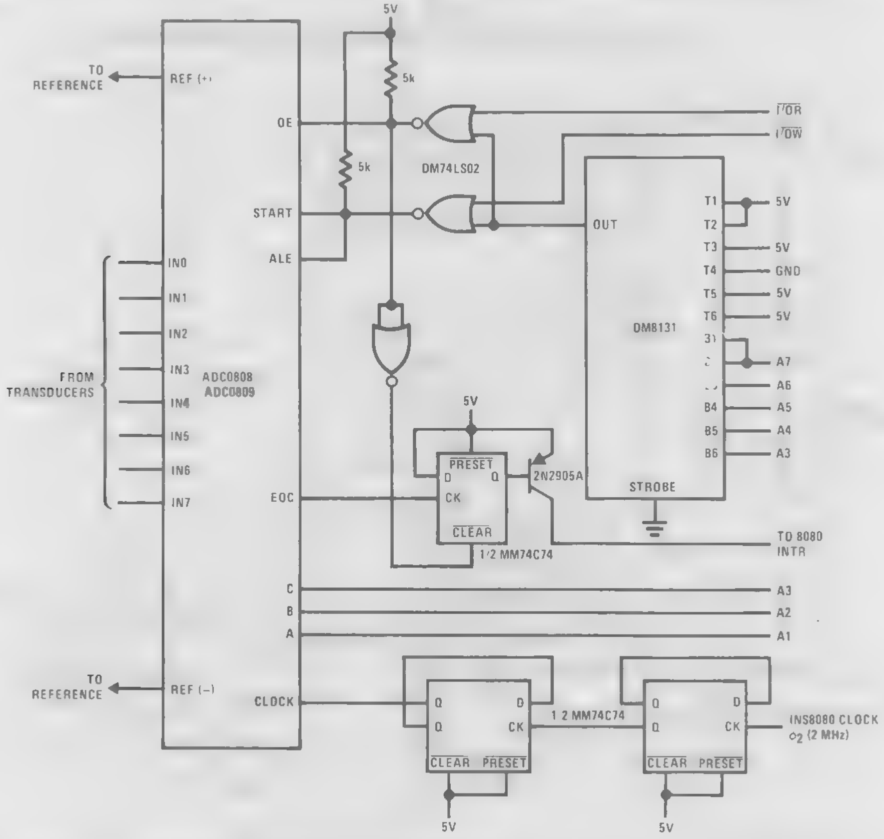
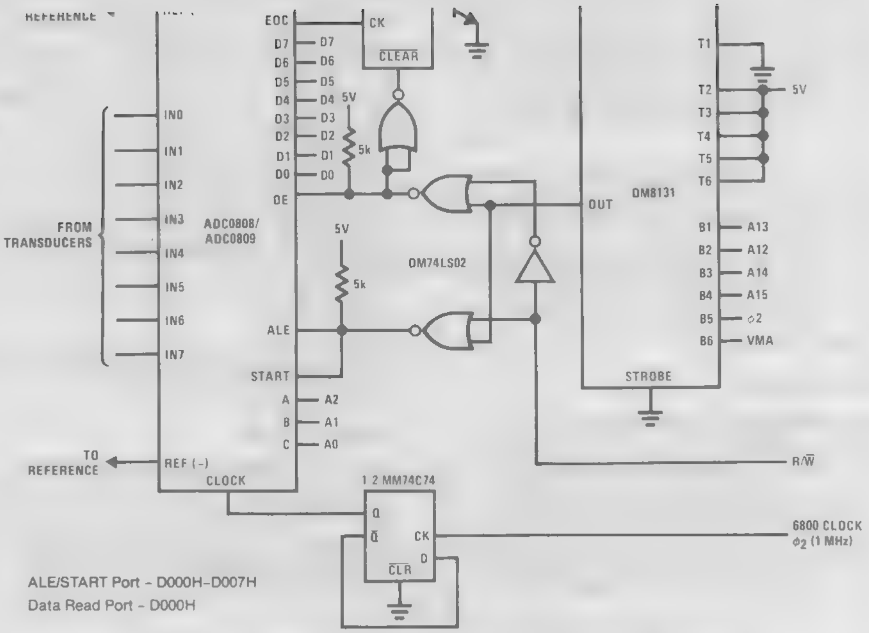


FIGURE 17. Interrupt-Type INS8080/INS8224/INS8228 Interface using 6-Bit Bus Comparator



ALE/START Port - D000H–D007H
Data Read Port - D000H

FIGURE 18. Typical 6800 Interface with Partial Address Decoding

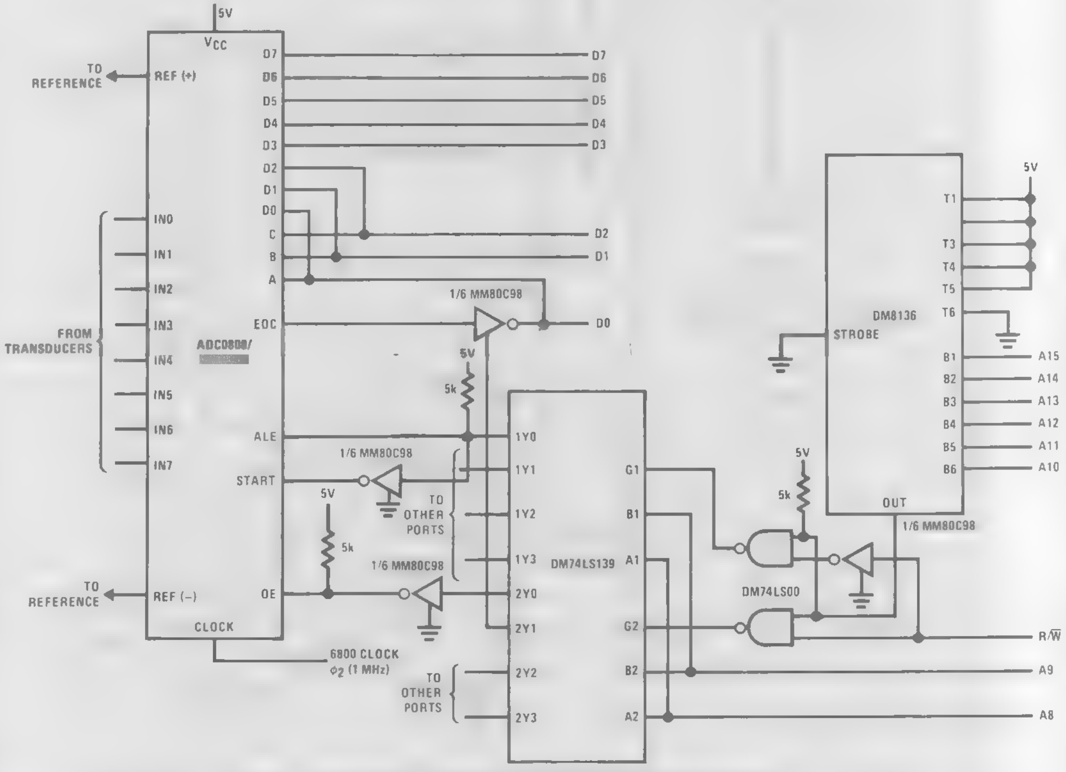


FIGURE 19. Fully Decoded 6800 Interface Address

```
*
* UTILITY ROUTINES FOR ADC0808/ADC0809 INTERFACE
*
*
* LOAD AND START CONVERSION (FIGURE 18)
*
 STATUS           EQU        $D800         START ADDRESS FOR CHANNEL 0
 DATA             EQU        $D800         CONVERTER DATA ADDRESS
*
*
*
 START            STA        STATUS        SELECT CHANNEL 0 AND START
                  STA        STATUS        DO AGAIN TO LET INPUTS SETTLE
                  LDX        #VECTOR       LOAD INTERRUPT VECTOR ADDRESS
                  STX        $FFF8         STORE IT
                  — —                      EXECUTE MISC PROGRAM
                  — —
                  — —
                  CLI                      ENABLE INTERRUPT IF NOT ALREADY
                  — —                      EXECUTE MISC PROGRAM
                  WAI                      WAIT FOR INTERRUPT
*
* INTERRUPT HANDLER (FIGURE 18)
*
 VECTOR           LDAA       DATA          LOAD DATA RESET INTERRUPT
                  CLI                      ENABLE INTERRUPTS (OPTION)
                  — —                      EXECUTE PROGRAM
                  RTI                      RETURN TO MAIN PROGRAM
*
* START AND TEST CONVERSION POLLED MODE (FIGURE 19)
*
 DATA2            EQU        $F800         CONVERTER DATA ADDRESS
 CHANN2           EQU        02            CHANNEL 2 ADDRESS
 EOCIN            EQU        $F900         EOC INPUT PORT
 START 2          LDAA       CHANN 2       LOAD A ACCUMULATOR
                  STAA       STATUS        LOAD ADDRESS AND START
                  NOP                      WAIT
                  STAA       STATUS        RESTART TO LET MUX SETTLE
                  NOP                      8 NOPS TO WAIT FOR EOC
                  — —                      TO GO LOW
                  LDAA       EOCIN         LOAD EOC STATUS BIT
                  ANDA       01            MASK BITS 1-7
                  BEQ        READY         IF A = 0 THEN CONVERTER DONE
*
*
                  — —                      EXECUTE MISC PROGRAM

*
* CONTINUOUS POLLING OF EOC (FIGURE 19)
*
*
 POLLIT           LDAA       EOCIN         LOAD EOC STATUS
                  ANDA       CHANN 2       MASK MSBs
                  BNE        POLL IT       IT ACC ≠ 0 NOT READY, LOOP
 READY            LDAA       DATA          ELSE READ DATA
                  — —                      CONTINUE PROGRAM
                  — —
```

FIGURE 20. Typical I/O Routines for ADC0808/ADC0809 and 6800 Interface

Figure 21 shows a very simple Z80 interface, which is similar to the INS8080 interface of *Figure 13*, except that the interrupt flip-flop design is closer to the 6800 designs. This is because the Z80 $\overline{\text{INT}}$ is active low as is the 6800, but the INS8080 INT is active high.

Figure 22 shows a fully decoded bus comparator design where the DM8131 decodes 5 address bits and the $\overline{\text{IOREQ}}$ I/O request strobe. Two NOR gates gate the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes for ALE, START and OE inputs.

4.0 CONCLUSION

Both the ADC0808 and the ADC0809 can be easily used in microprocessor controlled environments. Many sophisticated medium throughput applications can be handled with a minimum of extra hardware, but additional hardware can increase flexibility and simplify software. Putting both the multiplexer and A/D on the same chip frees the designer from matching multiplexers and A/Ds to implement a 7 or 8-bit accurate system. Design time and overall system cost can be reduced by using these low cost converters.

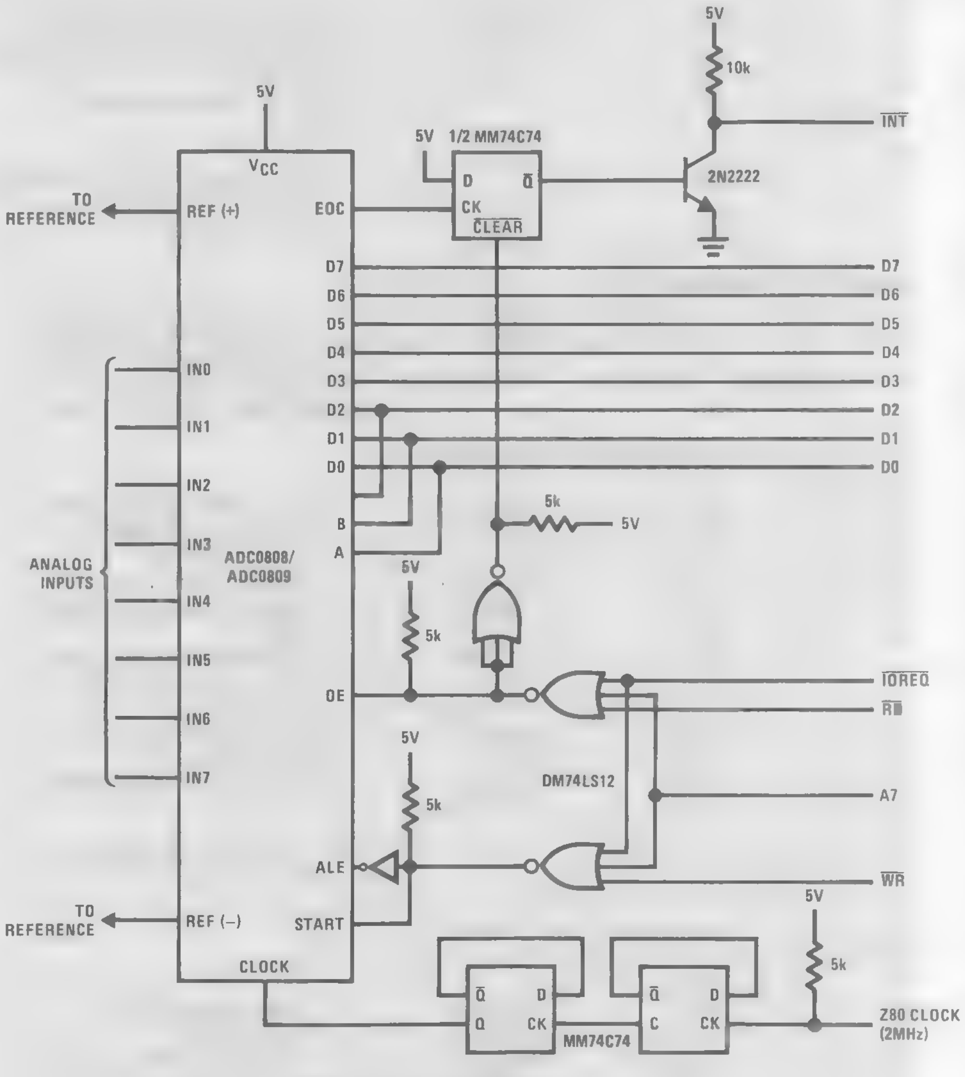


FIGURE 21. Simple Z80 Interface

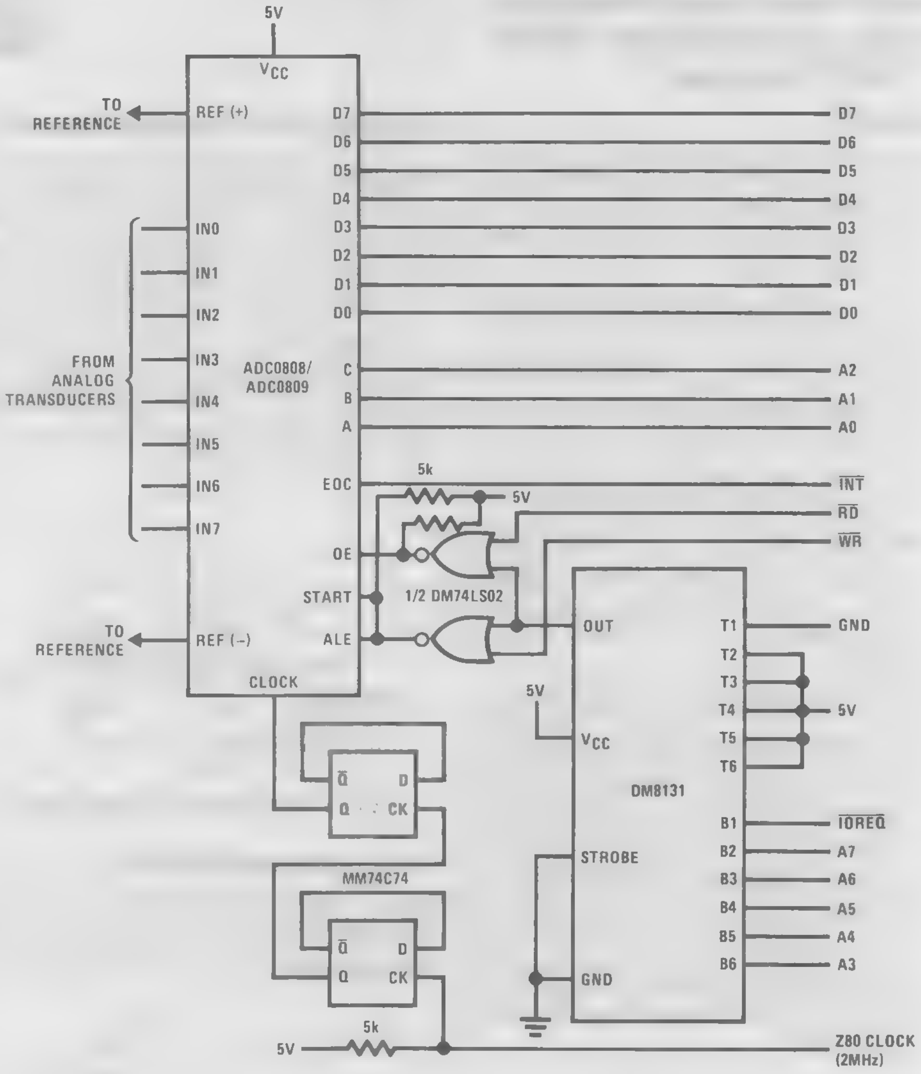


FIGURE 22. Z80 Partial Decoding Interface

Electrostatic Discharge Prevention — Input Circuits and Handling Guide for CMOS Devices

Introduction

During the past few years, there have been significant increase in the usage of low-power CMOS devices in system designs. This has resulted in more stringent attention to handling techniques of these devices, due to their static sensitivity, than ever before.

All CMOS devices, which are composed of complementary pairs of n- and p-channel MOSFET's, are susceptible to damage by the discharge of electrostatic energy between any two pins. This sensitivity to static charge is due to the fact that gate input capacitance (5 picafarads typical) in parallel with an extremely high input resistance (10^{12} ohms typical) lends itself to a high input impedance and hence readily builds up the electrostatic charges, unless proper precautionary measures are taken. This voltage build-up on the gate can easily breakdown the thin (1000Å) gate oxide insulator beneath the gate metal. Local defects such as pinholes or lattice defects of gate oxide can substantially reduce the dielectric strength from a breakdown field of $8\text{-}10 \times 10^6$ V/cm to $3\text{-}4 \times 10^6$ V/cm. This then becomes the limiting factor on how much voltage can be applied safely to the gates of CMOS devices.

When a higher voltage, resulting from a static discharge, is applied to the device, permanent damage like a short to substrate, V_{DD} pin, V_{SS} pin, or output can occur. Now static electricity is always present in any manufacturing environment. It is generated whenever two different materials are rubbed together. A person walking across a production floor can generate a charge of thousands of volts. A person working at a bench, sliding around on a stool or rubbing his arms on the work bench can develop a high static potential. Table 1 shows the results of work done by Speakman[1] on various static potentials developed in a common environment. The ambient relative humidity, of course, has a great effect on the amount of static charge developed, as moisture tends to provide a leakage path to ground and helps reduce the static charge accumulation.

Table 1. Various Voltages Generated in 15%-30% Relative Humidity (after Speakman[1])

Condition	Most Common Reading (Volts)	Highest Reading (Volts)
Person walking across carpet	12,000	39,000
Person walking across vinyl floor	4,000	13,000
Person working at bench	500	3,000
16-lead DIPs in plastic box	3,500	12,000
16-lead DIPs in plastic shipping tube	500	3,000

Standard Input Protection Networks

In order to protect the gate oxide against moderate levels of electrostatic discharge, protective networks are provided on all National CMOS devices, as described below.

Figure 1 shows the standard protection circuit used on all A, B, and 74C series CMOS devices. The series resistance of 200 ohms using a P^+ diffusion helps limit the current when the input is subjected to a high-voltage zap. Associated with this resistance is a distributed diode network to V_{DD} which protects against positive transients. An additional diode to V_{SS} helps to shunt negative surges by forward conduction. Development work is currently being done at National on various other input protection schemes.

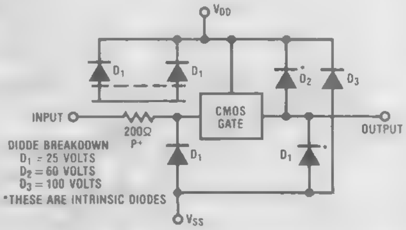


Figure 1. Standard Input Protection Network

Other Protective Networks

Figure 2 shows the modified protective network for CD4049/4050 buffer. The input diode to V_{DD} is deleted here so that level shifting can be achieved where inputs are higher than V_{DD}.

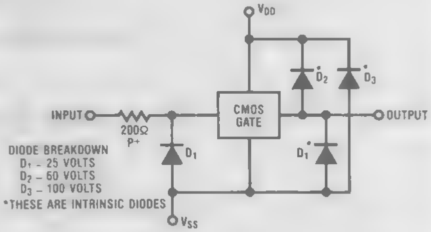


Figure 2. Protective Network for CD4049/50 and MM74C901/2

Figure 3 shows a transmission gate with the intrinsic diode protection. No additional series resistors are used so the on resistance of the transmission gate is not affected.

All CMOS circuits from National's CD4000 Series and 74C Series meet MIL-STD-38510 zap test requirements of 400 volts from a 100 pF charging capacitor and 1.5 kΩ series resistance. This human body simulated model of

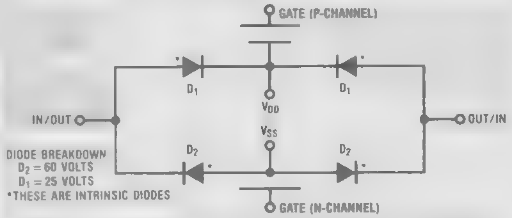


Figure 3. Transmission Gate with Intrinsic Diodes to Protect Against Static Discharge

100 pF capacitance in series with 1.5 kΩ series resistance was proposed by Lenzlinger[2] and has been widely accepted by the industry. The set-up used to perform the zap test is shown in Figure 4.

V_{ZAP} is applied to DUT in the following modes by charging the 100 pF capacitor to V_{ZAP} with the switch S_1 in position 1 and then switching to position 2, thus discharging the charge through 1.5 kΩ series resistance into the device under test. Table 2 shows the various modes used for testing.

Table 2. Modes of High-Voltage Test

Mode	+ Terminal	− Terminal
1	Input	V_{SS}
2	V_{DD}	Input
3	Input	Associated Output
4	Associated Output	Input

Pre- and post-zap performance is monitored on the input leakage parameter at $V_{DD} = 18$ Volts. It has been found that all National's CMOS devices of CD4000 and 74C families can withstand 400 volts zap testing with above mentioned conditions and still be under the pre- and post-zap input leakage conditions of ±10 nA.

Handling Guide for CMOS Devices

From Table 1, it is apparent that extremely high static voltages generated in a manufacturing environment can destroy even the optimally protected devices, by reaching their threshold failure energy levels. For preventing such catastrophies, simple precautions taken could save thousands of dollars for both the manufacturer and the user.

In handling unmounted chips, care should be taken to avoid differences in voltage potential between pins. Conductive carriers such as conductive foams or conductive rails should be used in transporting devices. The following simple precautions should also be observed.

1. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
3. Table tops should be covered with grounded conductive tops. Also test areas should have conductive floor mats.

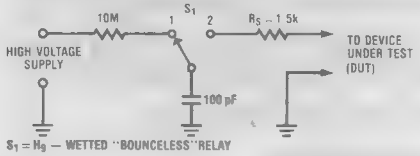

S1
10M
1
2
RS – 1 5k
HIGH VOLTAGE SUPPLY
TO DEVICE UNDER TEST (DUT)
100 pF
S1 = Hg — WETTED "BOUNCELESS" RELAY

Figure 4. Equivalent RC Network to Simulate Human Body Static Discharge (After Lenzlinger[2])

Above all, there should be static awareness amongst all personnel involved who handle CMOS devices or the sub-assembly boards. Automated feed mechanisms for testing of devices, for example, must be insulated from the device under test at the point where devices are connected to the test set. This is necessary as the transport path of devices can generate very high levels of static electricity due to continuous sliding of devices. Proper grounding of equipment or presence of ionized-air blowers can eliminate all these problems.

At National all CMOS devices are handled using all the precautions described above. The devices are also transported in anti-static rails or conductive foams. Anti-static, by definition[3] means a container which resists generation of triboelectric charge (frictionally generated) as the device is inserted into, removed from, or allowed to slide around in it. It must be emphasized here that packaging problems will not be solved merely by using anti-static rails or containers as they do not necessarily shield devices from external static fields, such as those generated by a charged person. Commercially available static shielding bags, such as 3M company's low resistivity ($\leqslant 10^4$ ohms/sq.) metallic coated polyester bags, will help prevent damages due to external stray fields. These bags work on the well-known Faraday cage principle. Other commercially available materials are Legge company's conductive wrist straps, conductive floor coating, and various other grounding straps which help prevent against the electrostatic damage by providing conductive paths for the generated charge and equipotential surfaces.

It can be concluded that electrostatic discharge prevention is achievable with simple awareness and careful handling of CMOS devices. This will mean wide and useful applications of CMOS in system designs.

Footnotes

1. T.S. Speakman, "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to ESD," 12th Annual Proc. of Reliability Physics, 1974.
2. M. Lenzlinger, "Gate Protection of MIS Devices," IEEE Transac. on Electron Devices, ED-18, No. 4, April 1971.
3. J.R. Huntsman, D.M. Yenni, G. Mueller, "Fundamental Requirements for Static Protective Containers." Presented at 1980 Nepcon/West Conference, Application Note — 3M Static Control Systems.

Simplified Multi-Digit LED Display Design Using MM74C911/MM74C912/MM74C917 Display Controllers — AN-257

Simplified Multi-Digit LED Display Design Using MM74C911/MM74C912/MM74C917 Display Controllers

National Semiconductor
Application Note 257
Larry Wakeman
January 1981

I. Introduction

The MM74C911, MM74C912 and MM74C9127 are CMOS display controllers that control multiplexing of 8-segment LED displays. These devices each have an on-chip multiplex oscillator and associated logic to easily implement multi-digit displays with minimal additional hardware. These controllers were designed to be easily interfaced to a microprocessor as a small 4-or 6-byte area of write-only memory (WOM), but they are not limited to this environment.

The MM74C911 is the simplest of these devices. It has one data input for each of its eight segment outputs, allowing direct control of any LED segment. Both the MM74C912 and MM74C917 have five data inputs which accept either BCD (MM74C912) or hexidecimal (MM74C917) data, plus decimal point. The MM74C911 can interface up to four 8-segment displays and the MM74C912/MM74C917 can control up to six 8-segment displays.

II. Functional Description — MM74C911

The functional block diagram for the MM74C911 is shown in *Figure 1.* The eight data inputs are buffered and bussed to the four dual-port latches. To write data into a particular latch, K1 and K2 address inputs are decoded and the proper latch is enabled when $\overline{CE}$ and $\overline{WE}$ are taken low.

The latch outputs are controlled by the multiplexer (MUX) logic. All four latch data outputs are commonly bussed, and are sequentially read by the MUX logic. The bussed 8-segment outputs are then buffered by bipolar segment driver transistors, which are enabled when $\overline{SOE}$ is low, and are tri-stated when Segment Output Enable ($\overline{SOE}$) is held high. This allows easy display blanking without loss of data.

The multiplexer logic controls all of the timing for the MM74C911 and also generates the digit output strobes. The timing diagram is shown in *Figure 2.*

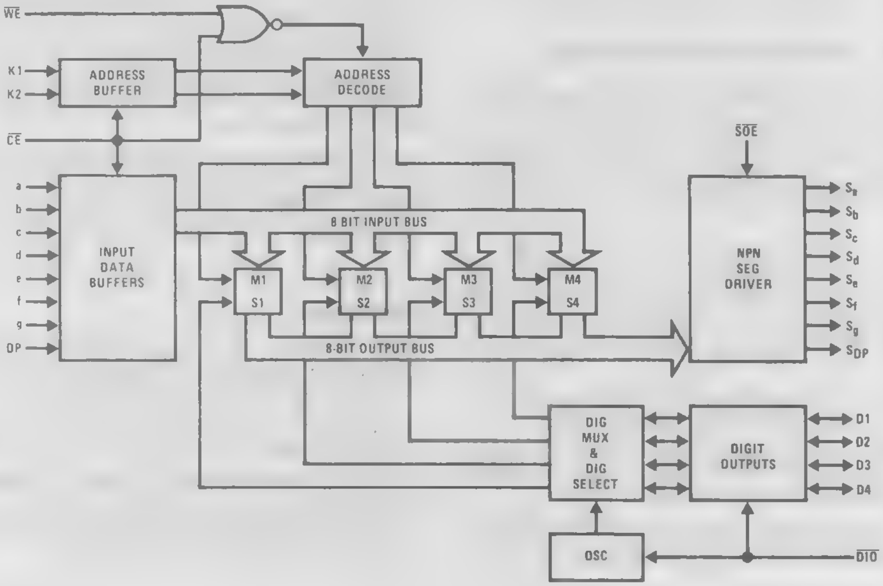


Figure 1. MM74C911 Block Diagram

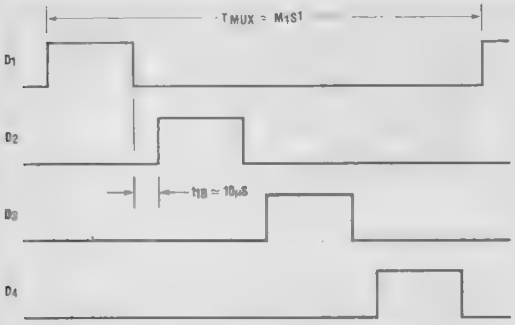


Figure 2. Mux Timing for MM74C911

By raising the Digit In-Out ($\overline{DIO}$) input high, the internal oscillator is disabled and the digit outputs become inputs which control reading of the 4-digit latches. This allows the MM74C911 to be slaved to other multiplex timing signals. If both $\overline{SOE}$ and $\overline{DIO}$ are held high, both the display and oscillator are disabled causing the MM74C911 to be in a low-power mode where it typically draws less than 1µA. *Figure 3* shows the truth table for these control inputs.

$\overline{DIO}/\overline{OSE}$	$\overline{SOE}$	MODE
0	0	NORMAL DISPLAY MODE
0	1	DISPLAY BLANKED
1	0	WILL DISPLAY ONE DIGIT*
1	1	LOW POWER MODE

Figure 3. Operating Modes for the MM74C911/MM74C912/MM74C917 (*The 74C911 Digit Outputs become inputs.)

III. Functional Description — MM74C912/MM74C917

The functional block diagram for the MM74C912 and MM74C917 is shown in *Figure 4*. These devices are very similar to the MM74C911. There are only five data inputs on the MM74C912 and MM74C917 which are buffered, then bussed to six 5-bit dual-port latches. The address present on K1, K2, and K3 will dictate which of the six latches will be loaded when both $\overline{CE}$ and $\overline{WE}$ are low. The outputs of all of the latches are commonly bussed and fed into a decoder ROM which converts BCD (MM74C912) or hexidecimal (MM74C917) code to seven segment. The fifth bit is the decimal point, which bypasses the ROM. The 8-segment bits are then buffered by eight NPN-segment drivers. Like the MM74C911, these outputs are tri-stateable and will blank the display when $\overline{SOE}$ is held high.

All of the multiplexing is controlled by an internal oscillator and control logic. The logic sequentially reads each latch and activates the digit outputs. The oscillator can be disabled by raising the Oscillator Enable ($\overline{OSE}$) input high, but the digit outputs do not become inputs and thus the MM74C912, and MM74C917 can not be slaved. However, by raising both $\overline{SOE}$ and $\overline{OSE}$ high, these parts can be put into a low-power mode similar to the MM74C911. *Figure 3* shows the controller operating modes.

The MM74C912 and the MM74C917 are identical except for the last seven ROM locations. The ROM outputs are shown in *Figure 5* for both parts.

IV. Display Interface Design

A. Common Cathode LED's

Since the MM74C911/MM74C912/MM74C917 contain all the multiplex circuitry necessary to operate a 4- or 6-digit display, all the designer must do is choose apropriate segment resistors and digit drivers to properly illuminate the LEDs. A typical LED connection is shown in *Figure 6*. Based on the selected display, a certain segment current will be required. This current will determine the value of the segment resistor and the type of digit driver necessary. The design for the MM74C911 is

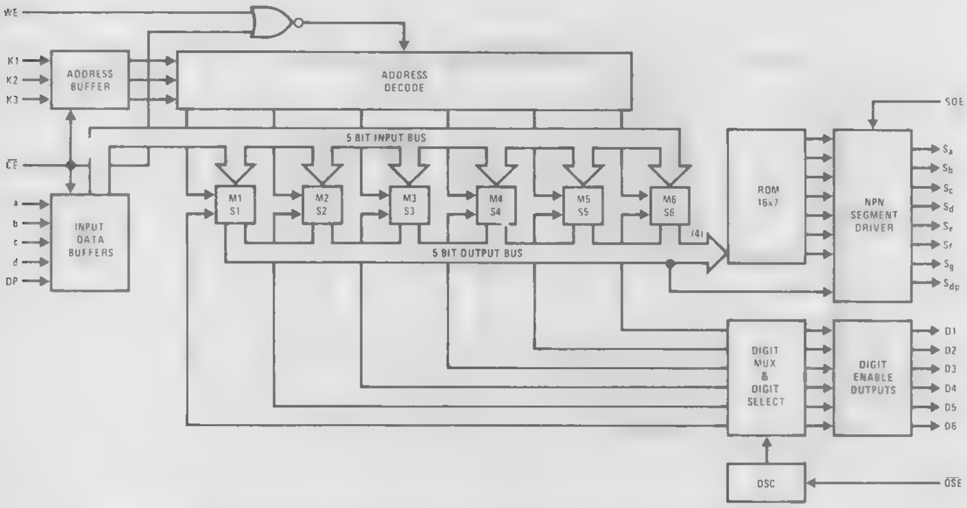
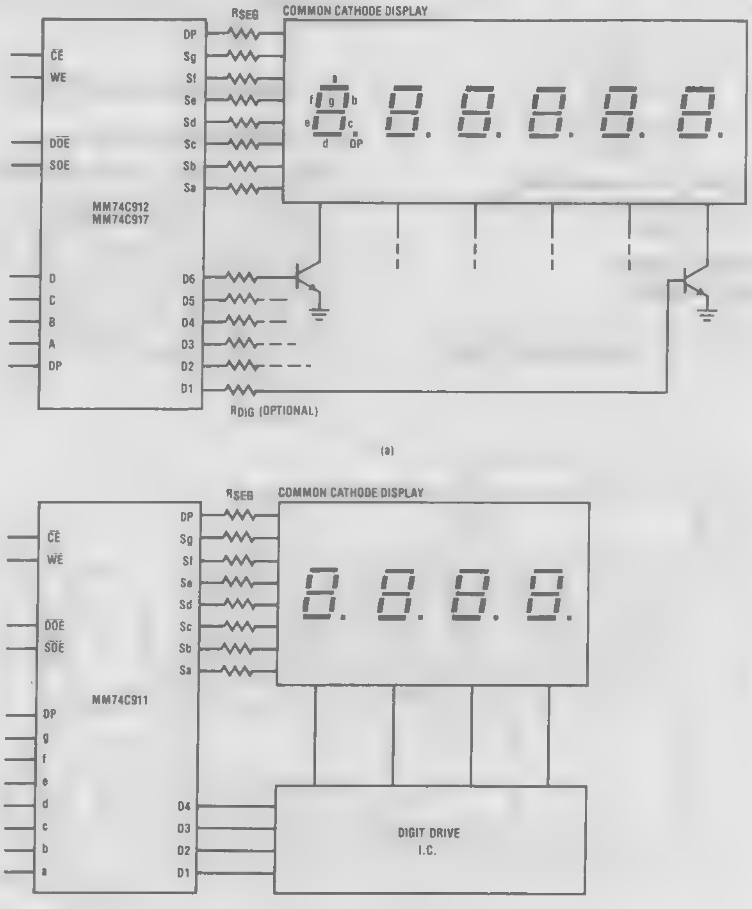


Figure 4. MM74C912 and MM74C917 Display Controller

MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	F.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	o	°	‾	-	_		.
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5. MM74C912/MM74C917 Character Fonts



(a)

(b)

Figure 6. Typical LED Connections for (a) MM74C912/MM74C917 (b) MM74C911

nearly the same as for the MM74C912/MM74C917 except that due to multiplexing the 6-digit controllers must be designed to a higher peak current value.

As an example, suppose the the NSN781 (2-digit, 0.7″ common catholde LED display) has been selected. These displays require an average current of 8 mA per segment for good illumination. The MM74C911 multiplexes four digits; thus, any one digit is on ¼ of the time. Each digit must have a peak current four times its average current to achieve the same brightness. The MM74C911 must supply about 32 mA per segment, and the MM74C912/MM74C917 would have to supply a current six times the average current or about 48 mA.

The maximum digit driver current is the maximum number of "on" segments multiplied by the segment current. For the MM74C911 design, the digit current is ~260 mA, and is ~380 mA for the MM74C912/MM74C917. Using this digit current value, the digit driver can be selected. *Figure 7* shows possible digit driver ICs, but discrete transistors or Darlingtons may also be used, and may be desireable in some higher current applications. It is also important to keep in mind that the output voltage of the driver at the designed current, as this voltage can affect the display controllers current drive. For most designs, an output voltage of <2 V is reasonable.

Once the digit driver has been chosen and the output voltage at the desired current is known, the segment resistor, R_{SEG} can be calculated using:

$$R_{SEG} = \frac{V_{SEG} - V_{LED} - V_{DO}}{I_{SEG}}$$

where V_{LED} is the voltage across the LED, 1.8 V; V_{DO} is the digit driver output voltage at the chosen current; I_{SEG} is the peak segment current; and V_{SEG} is the MM74C911 or MM74C912 segment driver output voltage at the peak segment current, which can be determined from the curves in *Figure 8*.

In most cases, R_{SEG} can be more quickly determined from *Figure 9* which plots R_{SEG} vs. average segment current. These curves are plotted for various digit driver output voltages using current values from *Figure 8*. Thus, for the above example, if a DS75492 driver I.C. is used with the MM74C911 to interface to the NSB781 LEDs $R_{SEG} = 38\,\Omega$ assuming the drivers output voltage is 1.0 V. Note that *Figure 7* tabulates minimum output drive where the above V_{DO} is an approximation of the DS75492s typical V_{DO} at 260 mA.

Part Number	Driver Type	Number of Drivers	Minimum Output Drive
DS75492	Darlington Driver	6	250 mA@1.5 V
DS75494	Multiple Transistor Driver	6	150 mA@0.35 V
DS8646	Transistor Driver	6	84 mA@0.55 V
DS8658	Transistor Driver	4	84 mA@0.55 V
DS8870	Darlington Driver	6	350 mA@1.4 V
DS8871/2	Transistor Driver	8/9	40 mA@0.5 V
DS8877	Transistor Driver	6	35 mA@0.5 V
DS8920	Transistor Driver	9	40 mA@0.5 V
DS8963	Darlington Driver	8	500 mA@1.5 V
DS8978	Transistor Driver	9	100 mA@0.7 V
DS8692	Transistor Driver	8	350 mA@1.0 V

Figure 7. Typical LED Digit Drivers and Their Characteristics

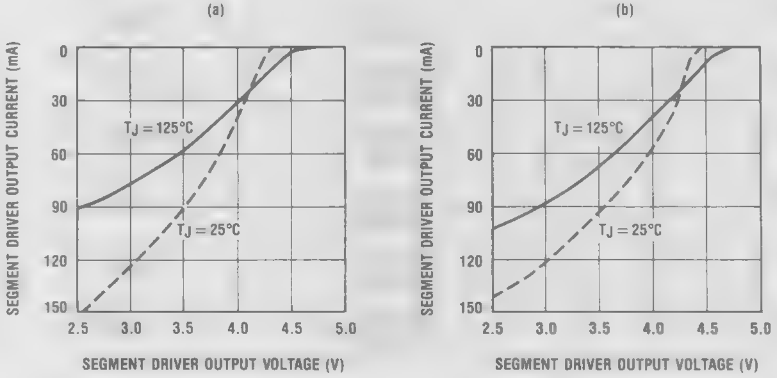


Figure 8. Typical Segment Driver Current vs. Output Voltage for (a) MM74C911 (b) MM74C912/MM74C917

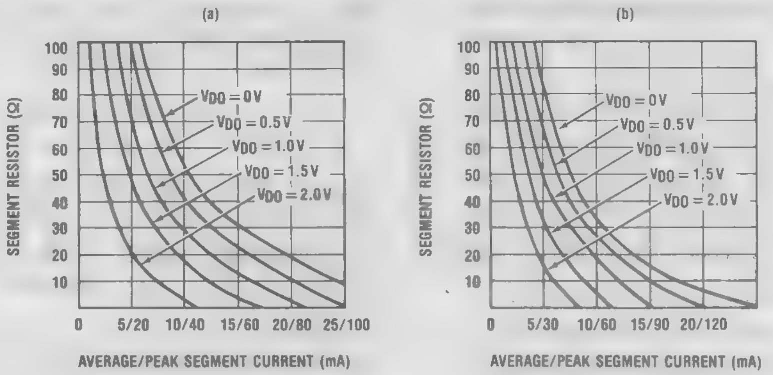


Figure 9. Average LED Segment Current vs. Segment Resistor for (a) MM74C911 (b) MM74C912/MM74C917

Figures 10 and *11* tabulate some typical segment resistor values for various National LED displays. (See Optoelectronics Databook for detailed specifications.) This table was compiled for a well lit room, but variation in ambient lighting may require some slight modification in the typical segment resistor values.

If a transistor digit driver is being used, it is sometimes desireable to use a base current limiting resistor between the controller's output and the transistor's base. This will help limit the power dissipation of the display controller in critical situations. The digit resistor, R_{DIG} can be calculated using:

$$R_{DIG} = \frac{V_{DIG} - V_{DI}}{I_{DI}}$$

where V_{DI} is the digit driver input voltage, 0.7V for a transistor, I_{DI} is the desired digit driver current and V_{DIG} is the controller's digit output voltage for the chosen current which can be found from *Figure 12*.

When the MM74C911 is to be used as a "master" to drive another MM74C911 or other logic, the digit outputs must have a high output voltage of 3.0V to driver another MM74C911 or 3.5V to drive standard CMOS logic. The digit resistor should be $> 300\Omega$ for $V_{OH} \geqslant 3.0V$ and $R_{DIG} > 350$ for $V_{OH} \geqslant 3.5V$.

A final design consideration is power dissipation. When designing a low-power system where the total current is to be minimized, the total system power consumption is simply:

$$P_T \cong V_{CC}[I_{DO} + I_{DI}]$$

DISPLAY			DRIVER	TYPICAL RANGE OF SEGMENT RESISTORS
PART NO.	HEIGHT (IN.)	NO. OF DIGITS		
NSA1298	0.110	9	DS75492	300-1000 Ω 300-2000 Ω*
NSA1558	0.140	8	DS75492	200-800 Ω 200-1800Ω*
NSN381	0.3	2	DS75492 2N3904	15-80 Ω
NSB3881	0.5	4	DS75492 2N3904	15-80 Ω
NSN581	0.5	2	DS75492 2N3904	10-60 Ω
NSB5881	0.5	4	DS75492 2N3904	10-60 Ω
NSN781	0.7	2	DS75492 2N3904	10-50 Ω
NSB7881	0.7	4	DS75492 2N3904	10-50 Ω

Figure 10. MM74C911 Segment Resistor Values for Various Displays ($V_{CC} = 5V$) (*Using Red LED Filter over Display)

DISPLAY			DRIVER ($R_D = 0$)	TYPICAL RANGE OF SEGMENT RESISTORS
PART NO.	HEIGHT (IN.)	NO. OF DIGITS		
NSA1298	0.110	9	DS75494	200-800 Ω 300-1500 Ω*
NSA1558	0.140	8	DS75494	150-700 Ω 150-1000Ω*
NSN381	0.3	2	DS75492	5-50 Ω
NSB581	0.5	2	DS75492	5-50 Ω
NS5931	0.5	6	DS75492 2N8004	5-40 Ω
NSN781	0.7	2	DS75492 2N8004	5-30 Ω

Figure 11. MM74C912/MM74C917 Segment Resistor for Average Intensity for Various Displays (*Using Red LED Filter over Display)

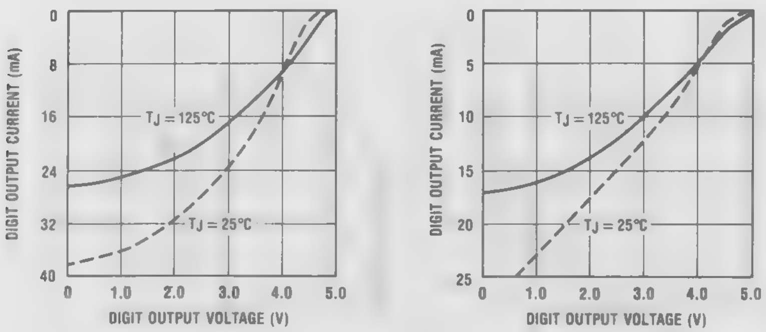


Figure 12. Typical Digit Driver Current vs. Output Voltage for (a) MM74C911 (b) MM74C912/MM74C917

where I_{DO} is the maximum digit driver output current, V_{CC} is the power supply voltage, and I_{DI} is the digit driver input current.

When a circuit design employs large segment currents, the maximum dissipation should be calculated to ensure that the power consumption of the controller or digit driver is within the maximum limits. The display controller power dissipation is:

$$P_C = S(I_{SEG})(V_{CC} - V_{SEG})$$

where I_{SEG} and V_{SEG} are the peak segment current and segment voltage, as previously determined; and S is the maximum number of segments lit per digit. The maximum package dissipation for the controllers vs. temperature is shown in *Figure 13*.

To gain an understanding of how segment current affects the controllers power dissipation, *Figure 14* plots average and peak LED segment current vs. package dissipation for both the MM74C911 and the MM74C912/MM74C917. These typical curves are plotted using the typical segment driver output currents and voltages from *Figure 8*.

As the digit driver output voltage V_{DO} becomes larger, the driver dissipates more power, thus the designer should also ensure that the driver's dissipation is not exceeded. Generally, the standard digit driver IC will dissipate around ½ watt. (See specific data sheets.) Driver power dissipation can be calculated by:

$$P_D = (V_{DO})(I_{DIG})$$

where V_{DO} and I_{DIG} are the digit driver output voltage and current. In a standard digit driver, one output will be active all the time, but if discrete transistors are used, each transistor is turned on 25% of the time. The average power dissipation for each discrete transistor digit driver is ¼ of the above equation.

B. Common Anode LED Display

Although connecting the MM74C911/MM74C912/MM74C917 to common anode displays is somewhat more difficult than to common cathode displays, it can be done. These controllers still provide all the necessary timing signals, but some extra buffering must be added to ensure the correct logic levels and drive capability.

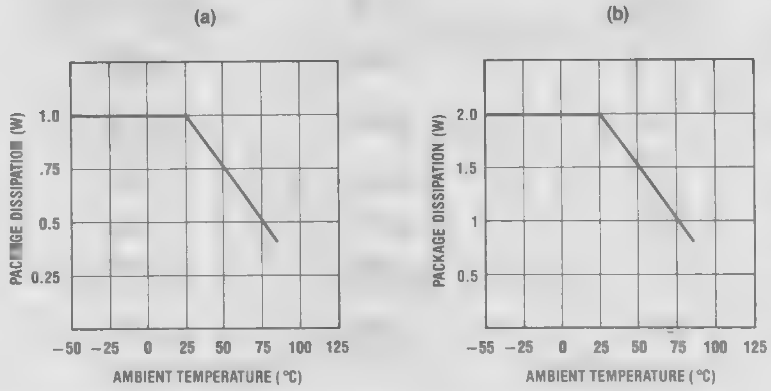


Figure 13. MM74C911/MM74C912MM74C917 Maximum Power Dissipation for (a) Plastic "N" Package (b) Ceramic "J" Package (Note $T_{J(MAX)}$ = 125°C Maximum Junction Temperature)

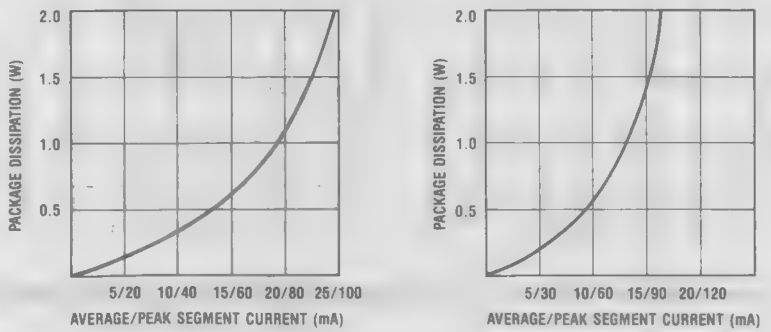


Figure 14. Typical Power Dissipation vs. Segment Current for (a) MM74C911 (b) MM74C912/MM74C917

To drive common anode displays, the display controller's segment outputs must be inverted and the digit outputs must be current buffered. *Figure 15* shows a simple circuit to interface to most common anode displays. An 8-digit calculator digit driver IC, DS8871, is used to drive the display segments. Segment resistors on the controller's segment outputs are not necessary but may be necessary on the outputs of the DS8871 driver.

For higher current displays, the choice of digit driver transistor is important as the digit current will depend on how high the digit driver output of the display controller can pull up due to the emitter follower configuration. For good display brightness, a high gain medium power transistor should be used.

C. Vacuum Florescent (VF) Displays

The MM74C911/MM74C912/MM74C917 are not directly capable of driving VF displays, but serve as a major functional block to ease driving 4- or 6-digit displays. The controllers provide the multiplex timing for this display, but the segment and digit outputs must be level shifted, and a filament voltage must be applied.

In *Figure 16*, a DS8654 or similar device is used to translate the segment and digit voltages to 30V to drive the segment plates and digit grids. The AC filament voltage is derived from a separate low-voltage transformer which is biased by a zener. Since there is no pull-down in the DS8654, pull-down resistors must be added. The exact anode and cathode voltages and the bias zener will depend on the display used, but the basic circuit is the same.

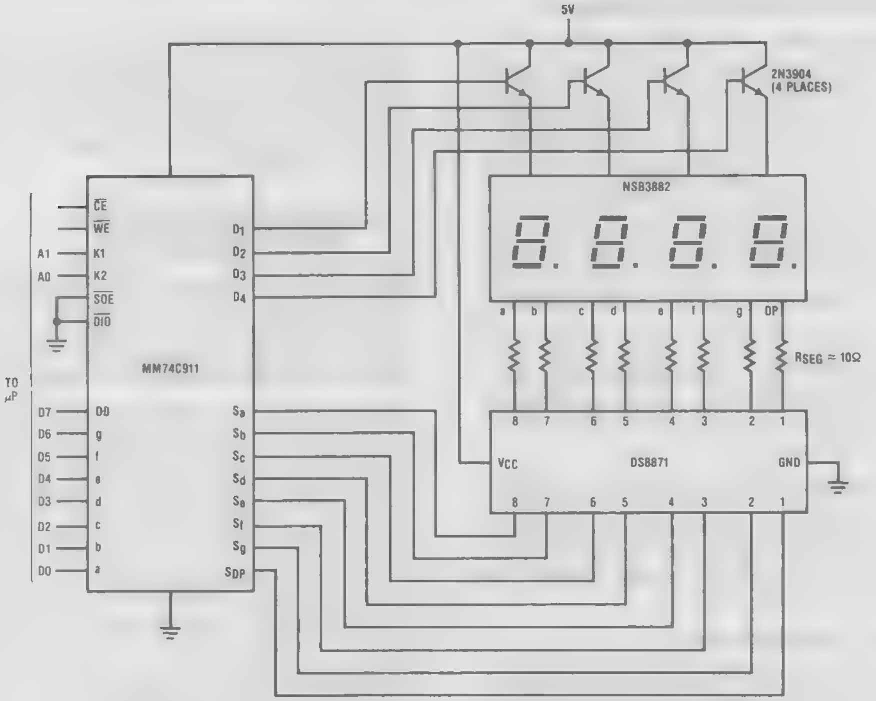


Figure 15. MM74C911 to Common Anode LED Interface Using 9 Digit Driver

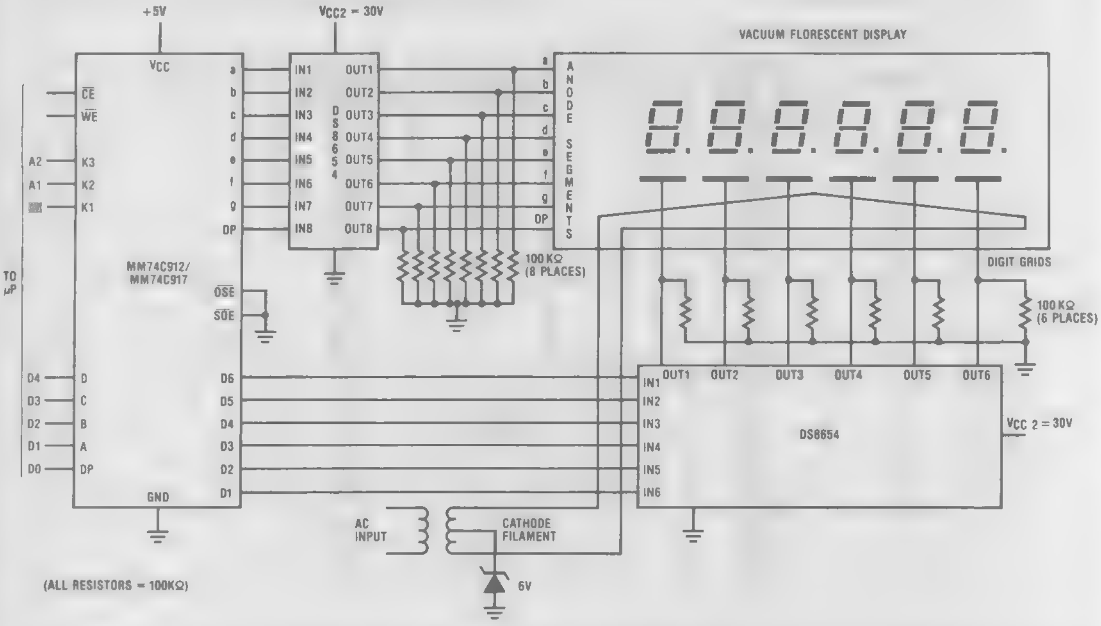


Figure 16. MM74C912/MM74C917 to Vacuum Fluorescent Display Interface

displays. In many cases, it may be desireable to enable a small microprocessor to display prompt messages where the use of more complicated alpha-numeric displays is not justified. For these cases, the MM74C911 is ideal, because any combination of segments can be controlled. *Figure 17* shows many of the possible letters and numbers that can be displayed along with their binary and hexidecimal values on 8-segment displays.

There is no reason to restrict the MM74C911 to alpha-numeric displays, as the controller allows direct control of individual LEDs. The MM74C911 can be connected to a mixture of numerical and discrete LEDs as typified by *Figure 18*. Thus status and numerical data can be simultaneously controlled.

Taking this one step further, all the LEDs could be discrete as shown in *Figure 19*. This type of arrangement is multipurpose. The LEDs could be configured as a 4 × 8 matrix or possible two-bar graphs of 16 LEDs, *Figure 20*, or maybe some sort of binary data display. There are many variations possible.

VI. Slaving The MM74C911

As mentioned, the MM74C911 has the unique feature of being able to be slaved to external multiplex logic or a "master" MM74C911. This feature is useful when the controller is to be synchronized with a master. *Figure 21* shows a typical application where two MM74C911s are used to drive a 16-segment alpha-numeric display. In order to drive this display, synchronization is required to ensure that both controllers are outputting the same digit information at the same time.

This can be advantageous when using smaller displays that require little power to begin with.

VII. MM74C912/MM74C917 Display Applications

Both the MM74C911/MM74C912 have predetermined character fonts and this limits their versatility, but greatly simplifies their application in hex and decimal display application. Still, there are a few small "tricks" that can be used to stretch the controller's capabilities.

In many applications, the decimal point segment is not needed, particularly when the MM74C917 is used. Generally, this part is used to display hexidecimal address and data information where decimal points are rarely needed. These segments could be used for status information. *Figure 23* shows a typical implementation. The status LEDs could indicate power, run and halt status information of a host μP or could indicate the type of instruction being executed. Although the MM74C912 applications would tend to use the decimal point more often, it is equally capable of implementing *Figure 23*.

Another possibility, if all six digits are not required, is to use the unused digits for status indicators. A possible example using the MM74C917 is shown in *Figure 24*, and another possible implementation for the MM74C912 is shown in *Figure 25*. In both of these applications, four bits of data is loaded into digits 1 and/or 2. Depending on the data loaded, various combinations of discrete LEDs would be lit. The tables included in these figures illustrate numerical combinations and their results.

CHARACTER	HEX CODE FOR 74C911	DISPLAY	CHARACTER	HEX CODE FOR 74C911	DISPLAY
0	FC	0	J	78	J
1	60	1	L	1C	L
2	DA	2	N	2A	n
3	F2	3	O	FC	0
4	66	4	O	3A	o
5	B6	5	P	CE	P
6	BE	6	R	0A	r
7	E0	7	S	B6	5
8	FF	8	T	8C	t
9	F6	9	U	7C	U
			U	38	u
A	EE	A	Y	76	y
B	3E	b	Y	4E	Y
C	9C	C			
D	7A	d	(Blank)	00	
E	9E	E	.	01	.
F	8E	F	—	02	-
G	BC	G	=	12	=
H	6E	H	?	CA	?
H	2E	h	⩾	D1	⩾
I	0C	I	<	9B	c
I	20	'			

Figure 17. Segment Codes for Various Characters Using 8-Segment Displays (MSB of Hex Code is segment a, LSB is Decimal Point ie for 0 (a = 1, b = 1, c = 1, d = 1, e = 1, f = 1, g = 0, dp = 0) = FC)

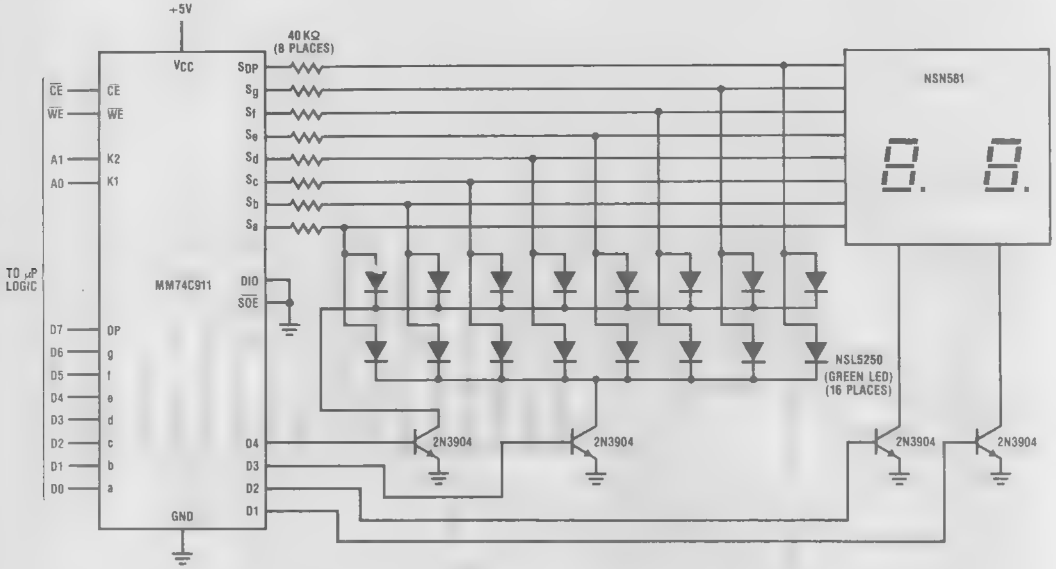


Figure 18. Discrete and Numeric Display

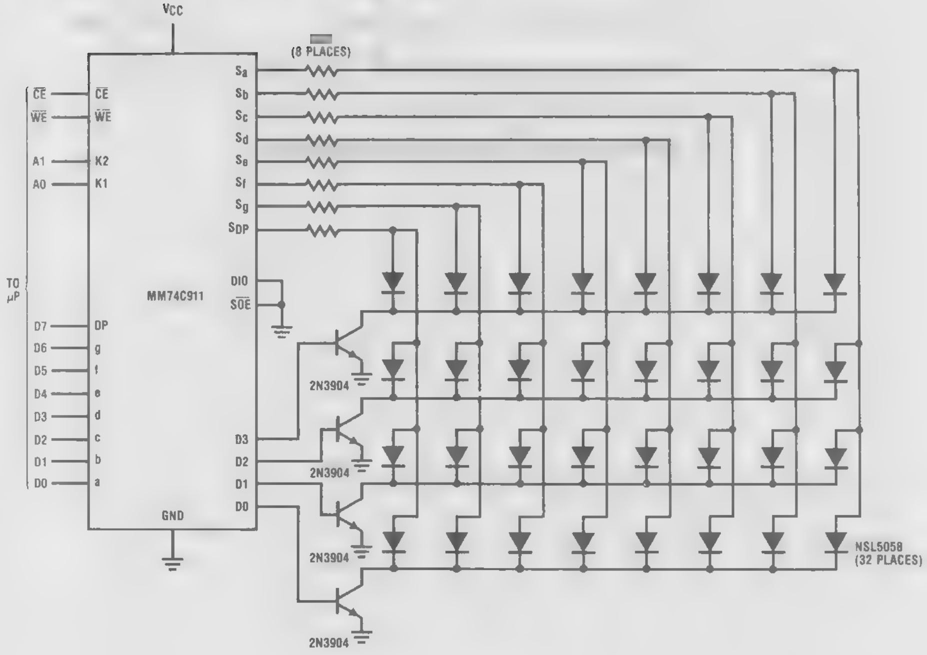


Figure 19. Discrete LED Matrix Display

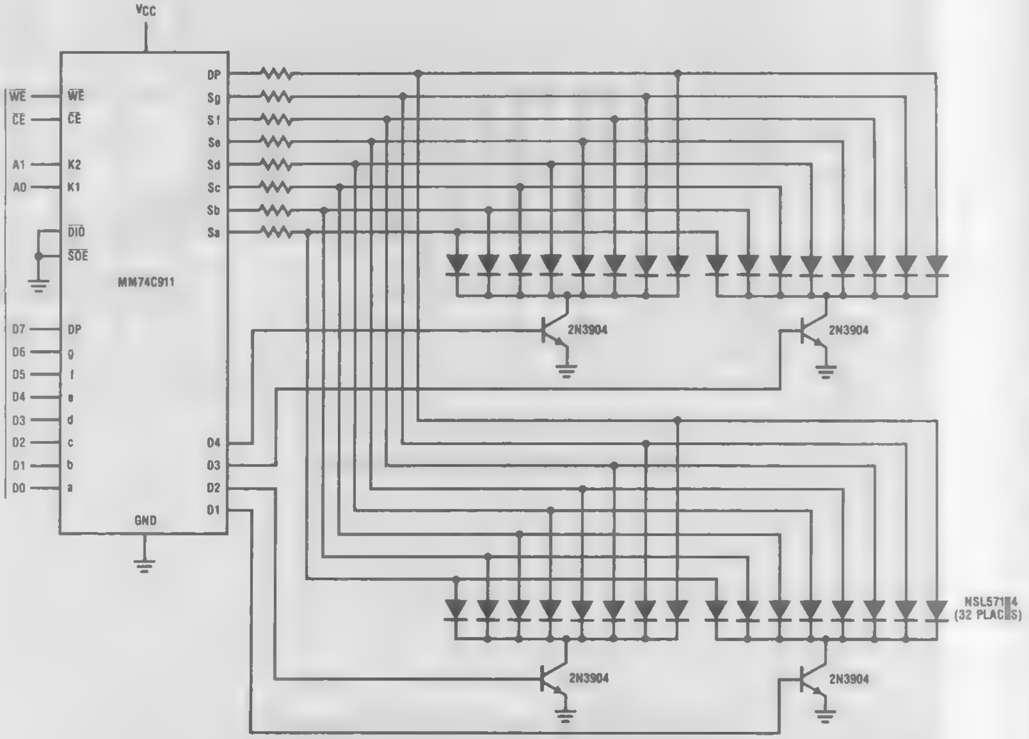


Figure 20. Dual 16 Element Bar Graph Display

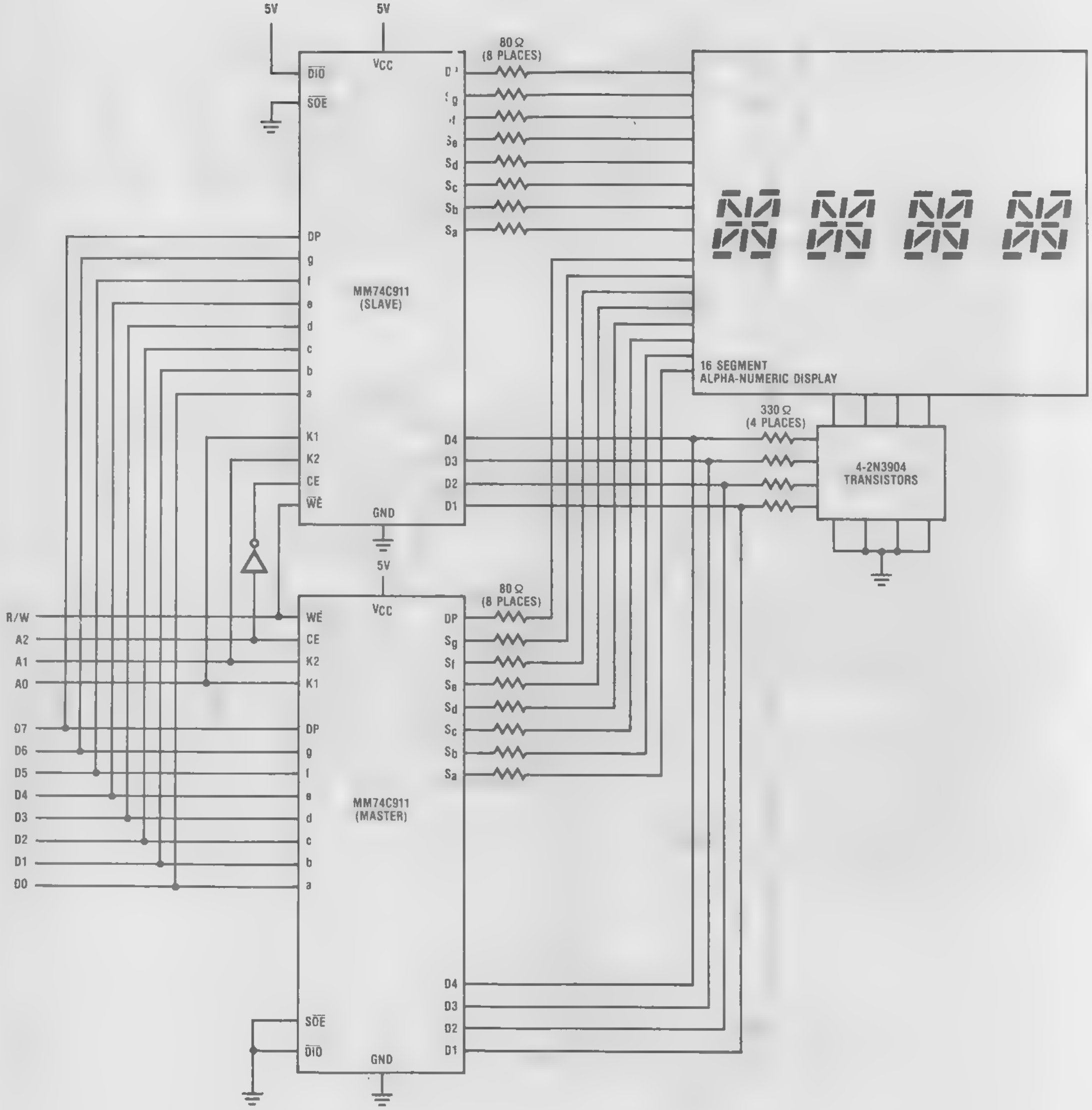


Figure 21. Interfacing to Alphanumeric Displays

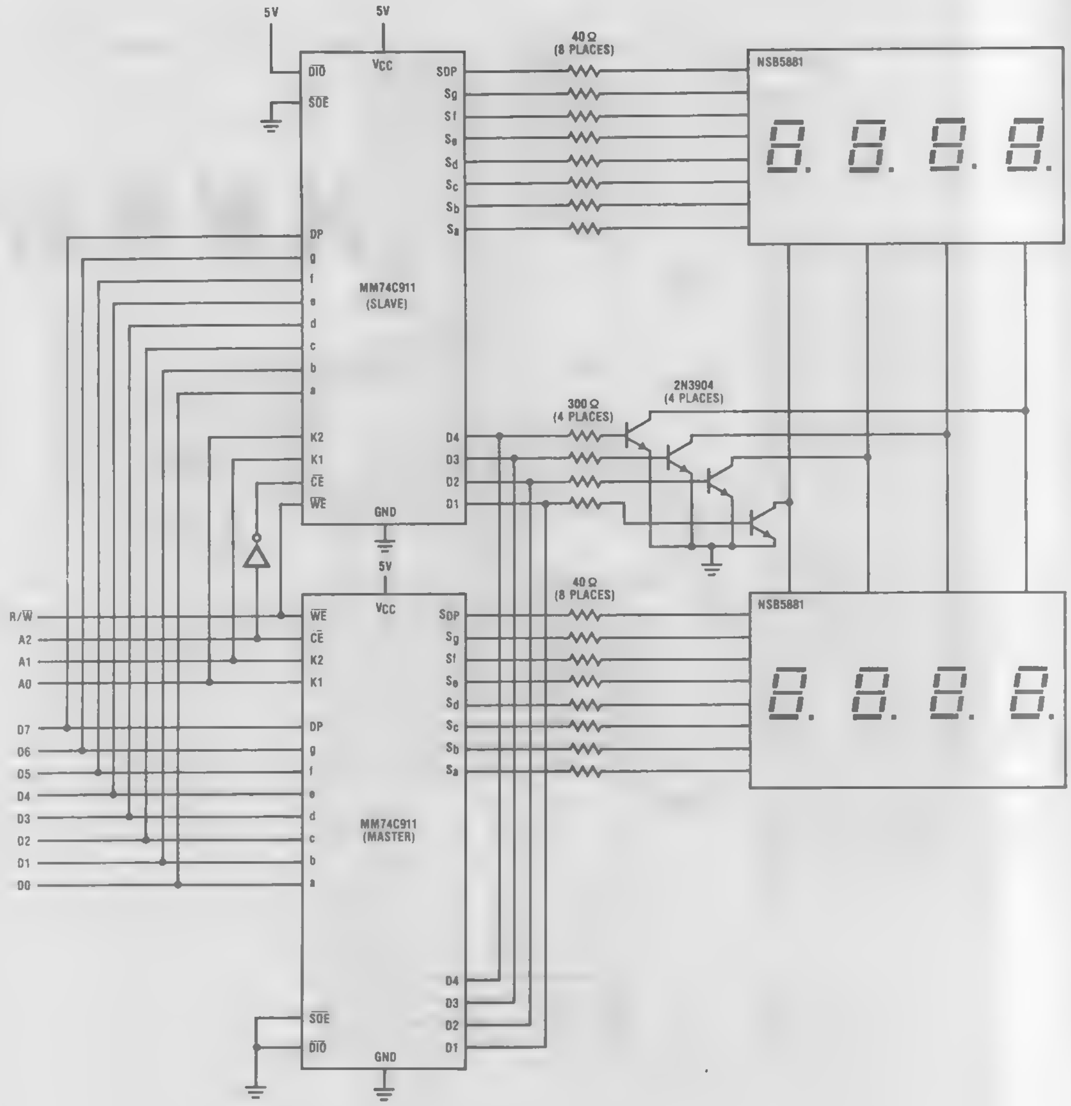


Figure 22. Multi-Digit Displays

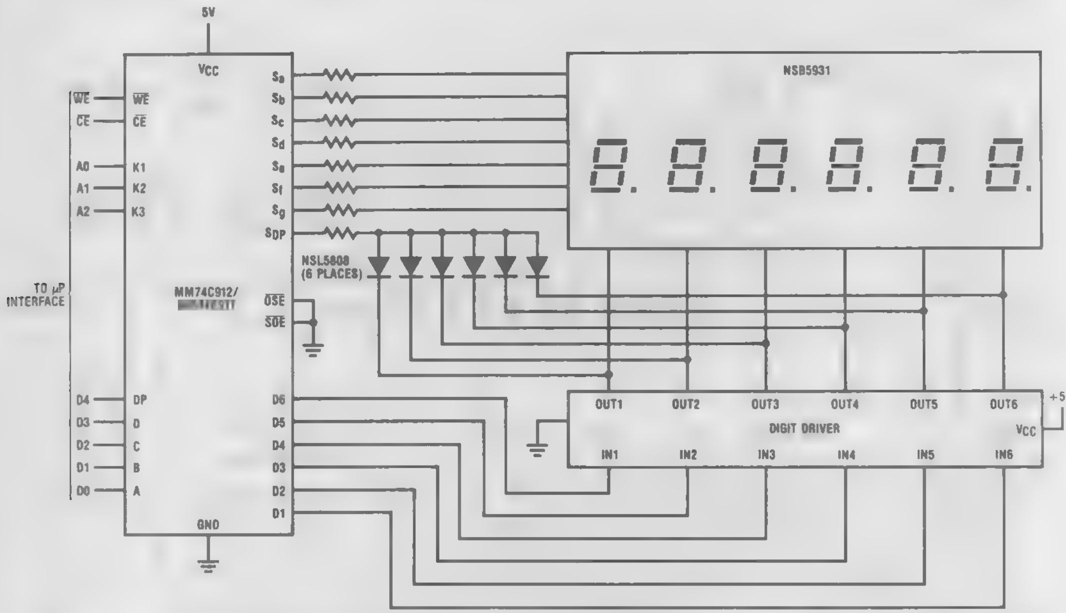
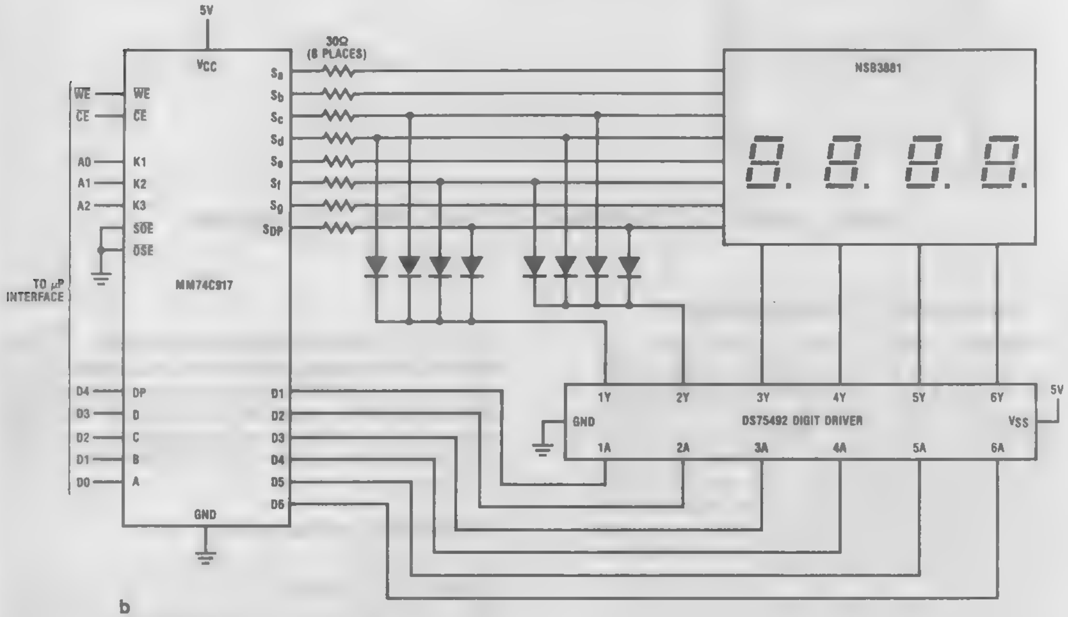


Figure 23. 7-Segment Displays with 6-Discrete LED Indicators for MM74C912/MM74C917 Using "DP" Segment

a

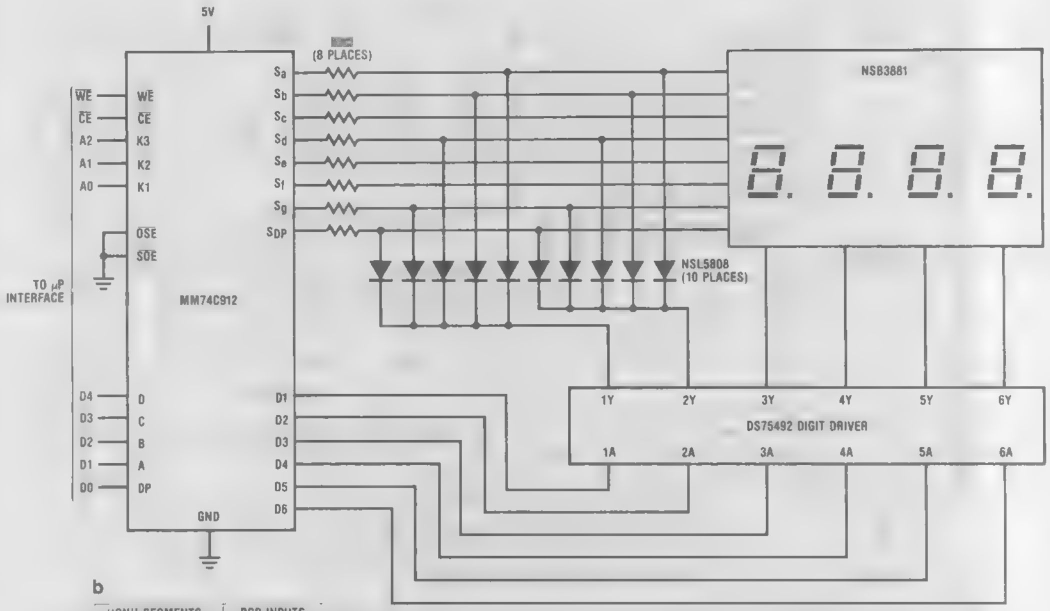


b

LED'S (1 = ON)				INPUTS				
DP	f	d	c	A	B	C	D	DP
1/0	0	0	0	—	—	—	—	1/0
1/0	0	0	1	0	0	0	1	1/0
1/0	0	1	0	0	0	1	0	1/0
1/0	0	1	1	0	0	1	1	1/0
1/0	1	0	0	1	1	1	1	1/0
1/0	1	0	1	0	1	0	0	1/0
1/0	1	1	0	1	1	0	0	1/0
1/0	1	1	1	1	0	0	0	1/0

Figure 24. MM74C917 (a) Display with 8 Discrete LED's (b) Inputs for LED Output Table

a



b

"ON" SEGMENTS					BCD INPUTS				
DP	G	D	B	A	D	C	B	A	DP
1/0	0	0	0	0	1	1	1	1	1/0
1/0	0	0	0	1	1	1	0	0	1/0
1/0	0	0	1	0	0	0	0	1	1/0
1/0	0	0	1	1	0	1	1	1	1/0
1/0	0	1	0	0	1	1	1	0	1/0
1/0	0	1	0	1	—	—	—	—	1/0
1/0	0	1	1	0	—	—	—	—	1/0
1/0	0	1	1	1	0	0	0	0	1/0
1/0	1	0	0	0	1	1	0	1	1/0
1/0	1	0	0	1	—	—	—	—	1/0
1/0	1	0	1	0	0	1	0	0	1/0
1/0	1	0	1	1	1	0	1	1	1/0
1/0	1	1	0	0	1	0	1	0	1/0
1/0	1	1	0	1	0	1	0	1	1/0
1/0	1	1	1	0	—	—	—	—	1/0
1/0	1	1	1	1	1	0	0	0	1/0

Figure 25. MM74C912 (a) 4 Digit Display with Discrete LEDs (b) I/O Data Table

VIII. Interfacing To Microprocessors

The CMOS LED display controllers can be easily interfaced to most of the popular microprocessors with the addition of only a few ICs. Most microprocessor data and address bus logic is specified to be TTL compatible. A standard TTL logic high, V_{OH} is supposed to be ≥ 2.4 at full load which is not compatible with a CMOS $V_{IH} \geq 3.5V$. Although microprocessor inputs will typically pull-up above 3.5V, this is not guaranteed over the entire temperature range. It is recommended that pull-up resistors be added to raise this level above 3.5V. Under most conditions, a 5-10K resistor should suffice.

The write timing of the display controllers is illustrated in *Figure 26*. The minimum write access time is 430ns for the MM74C912/MM74C917 and 450ns for the MM74C911. A write to the controller is accomplished by placing the desired data on the data inputs, lowering the $\overline{CE}$ and $\overline{WE}$ inputs, and then raising them to complete the write. Even though $\overline{CE}$ and $\overline{WE}$ are interchangeable, $\overline{CE}$ is usually derived from the address decoding logic and $\overline{WE}$ is connected to the CPU write strobe. Other than the slight timing differences between the MM74C911 and the MM74C912/MM74C917, the only other major microprocessor interfacing differences are that the MM74C912/MM74C917 have an additional digit address bit which must be connected to the microprocessors address bus, and the MM74C911 has eight data inputs whereas the MM74C912/MM74C917 have only five.

A. Interfacing To The INS8080

These controllers can be connected to the INS8080/INS8224/INS8238 CPU group with no external logic if no more than a minimal amount of address decoding is required. Since the INS8080 has a separate memory and I/O port address spaces, one of the I/O port address bits could be directly connected to the $\overline{CE}$ input. *Figure 27* illustrates this using an MM74C911. Whenever an OUT instruction is executed causing the $\overline{I/OW}$ (INS8080 write enable signal) to go low and the address is such that A7 is low, A0 A1 will select the digit to be written. If more decoding is required, some external gating logic may be added to the $\overline{CE}$ input.

The MM74C912/MM74C917 would be interfaced by connecting the A, B, C, D and DP to bit D0–D4 of the data bus and connecting K1–K3 to A_0–A_2. Writing data to these controllers would be the same as writing to the MM74C911

B. Interfacing to the Z80™*

To connect these display controllers to the Z80 microprocessor, only a minor modification to the INS 8080 need be made. The Z80 control signals are slightly different from the INS8080. Instead of the INS8080 I/O write strobe, the Z80 has an I/O request line ($\overline{\text{IOREQ}}$), which goes low to indicate an I/O port is to be accessed, and a write ($\overline{\text{WR}}$) strobe which indicates that a memory or I/O write is to be done. By OR-ing, these together an equivalent $\overline{\text{I/OW}}$ signal is generated as shown in *Figure 28*.

C. Interfacing to the NSC800

The NSC800 has very different timing because the lower eight address bits and the data bus are multiplexed. But when connecting the display controllers as I/O ports, the interface is only slightly different from the INS8080 design. When an I/O instruction is executed, the port address that appears on A0–A7 is duplicated on A8–A15, and this address can be used directly. The controller $\overline{\text{WE}}$ input must be decoded from a $\overline{\text{WR}}$ (write enable) and IO/$\overline{\text{M}}$ (I/O or memory enable) as shown in *Figure 29*. Note that since the NSC800 is a CMOS microprocessor, no pull-up resistors are needed.

Figure 29 uses address bit A15 which is equivalent to bit A7 on the previous examples. As with the previous examples, if more address decoding is required, either gates or decoders could be connected to the $\overline{\text{CE}}$ input.

D. Interfacing To The 6800

When using the INS8080, Z80, or NSC800, these processors have separate I/O and memory address spaces. This usually allows simpler interfaces to be designed. The 6800 has no separate I/O addressing so I/O ports are usually mapped into a small block of memory. This requires more address decoding to ensure that memory and I/O don't overlap.

Figure 30 shows a DM8131 6-bit address bus comparator whose B_n inputs are a combination of A15–A12 address bits, the Φ_2 (6800 system clock) and the VMA (Valid Memory Access) control signal. When these inputs equal the corresponding T_n inputs, the output goes low. The 6800 R/$\overline{\text{W}}$ signal is connected to the $\overline{\text{WE}}$.

E. Interfacing To The INS8060/INS8070

Like the 6800, the INS8060/8070 series of microprocessors don't have any separate I/O addressing, so the MM74C911/MM74C912/MM74C917 must be memory addressed, but unlike the 6800 both the INS8070 series and the INS8060 have separate read/write strobes, which can simplify interfacing the display controllers. *Figure 31* illustrates a typical INS8060 interface. The $\overline{\text{NWDS}}$ (write enable) is directly connected to the MM74C912s $\overline{\text{WE}}$ input and the DM8131 provides the address decoding for the controller. The INS8060 has only 12 address bits (unless using paged addressing) so bits A_6–A_{11} are decoded by the comparator.

The INS8070 series microprocessor has the identical $\overline{\text{NWDS}}$ signal but has 16 address bits. Thus *Figure 31* would connect the A10–A15 address bits to the DM8131.

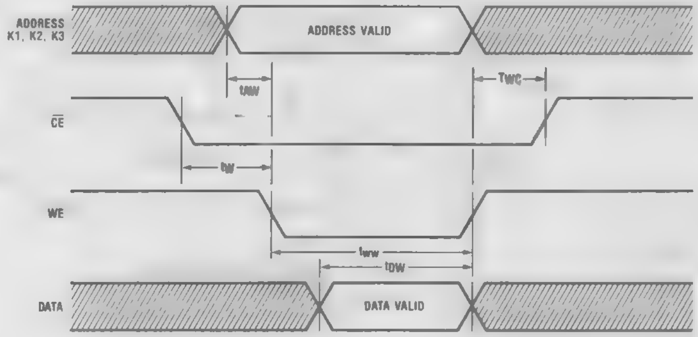


Figure 26. MM74C911/MM74C912/MM74C917 Timing Diagram (See data sheets for numbers)

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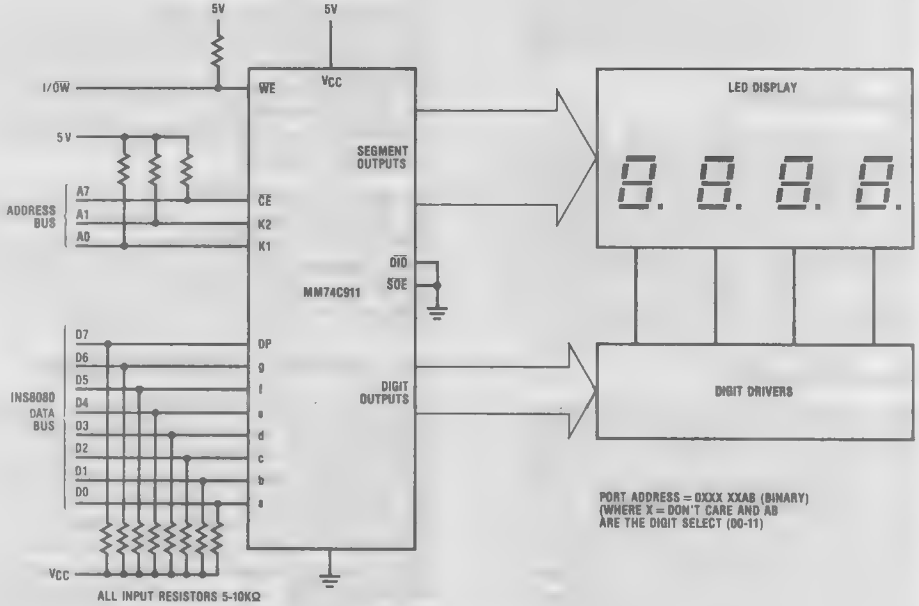
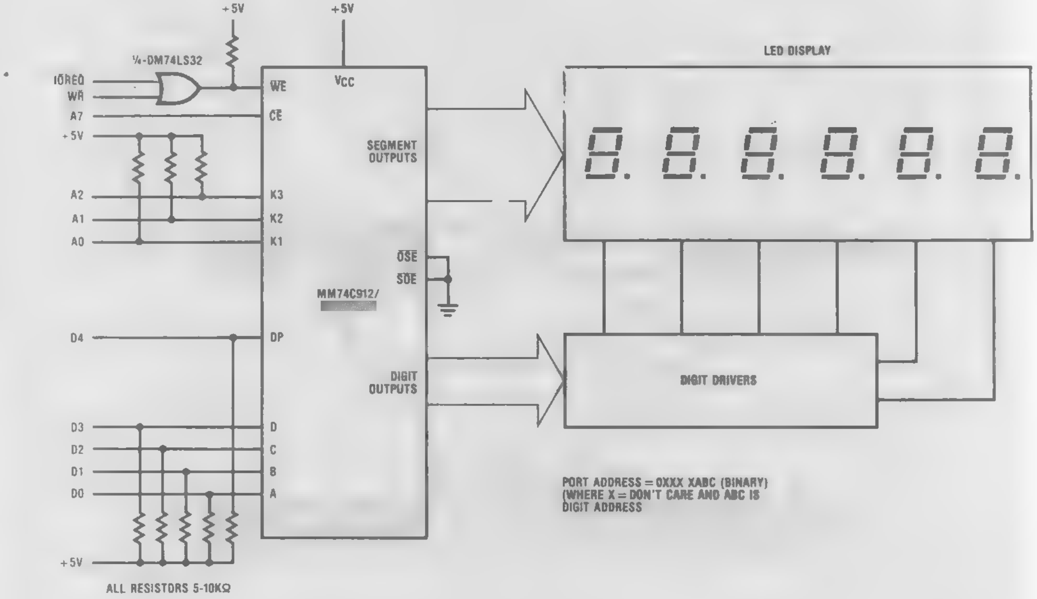
*Z-80 is a trademark of Zilog Inc.



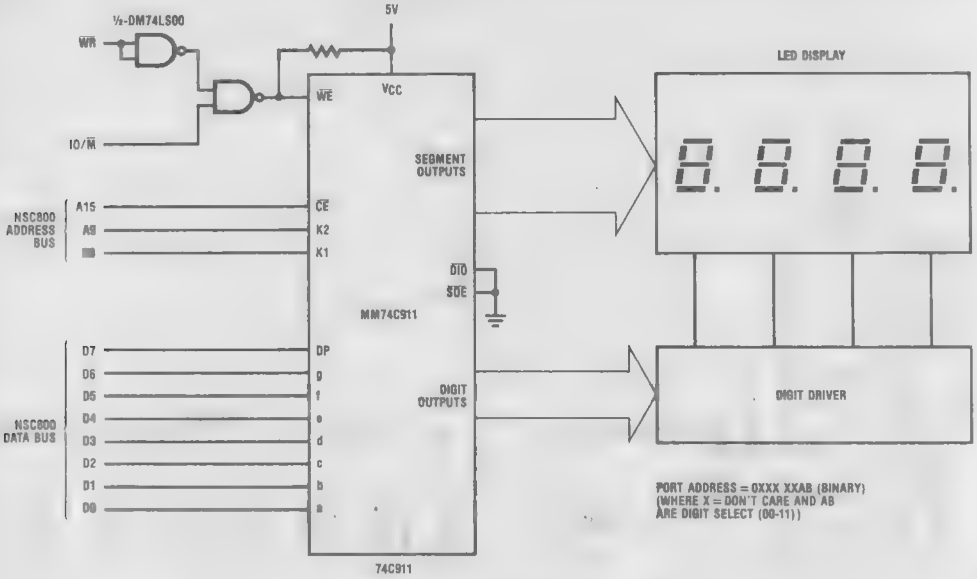
PORT ADDRESS = 0XXX XXAB (BINARY)
(WHERE X = DON'T CARE AND AB
ARE THE DIGIT SELECT (00-11)

Figure 27. INS8080/INS8224/INS8238 Interface to MM74C911



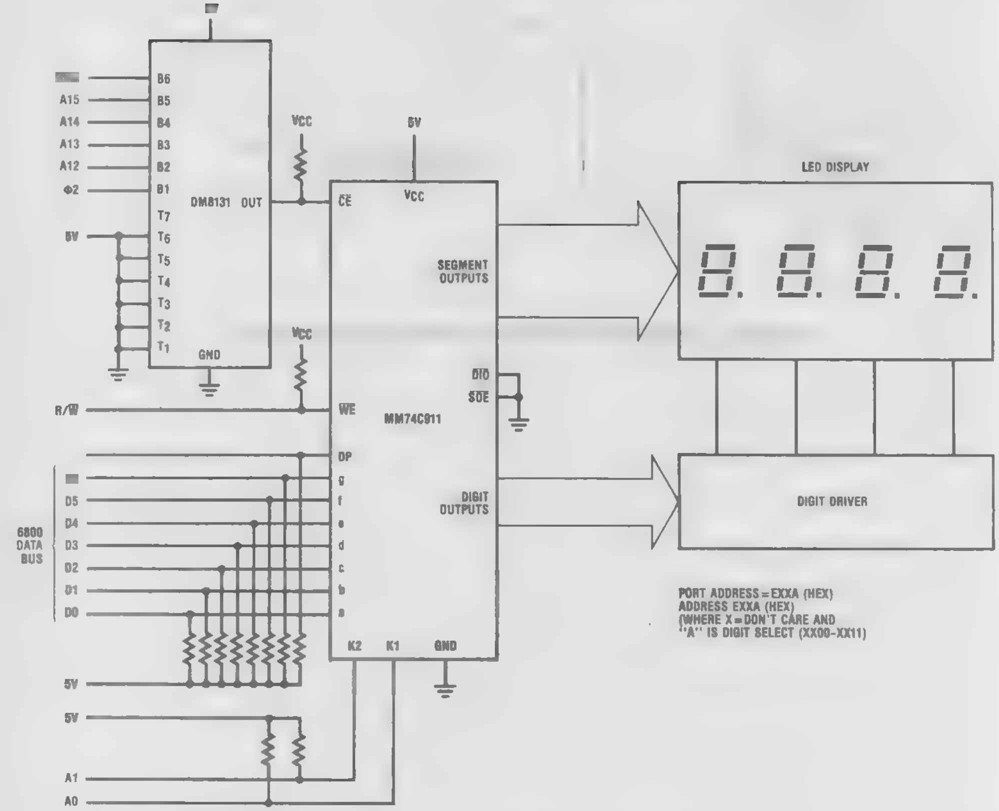
PORT ADDRESS = 0XXX XABC (BINARY)
(WHERE X = DON'T CARE AND ABC IS
DIGIT ADDRESS

Figure 28. Z80 Interface to MM74C912/MM74C917



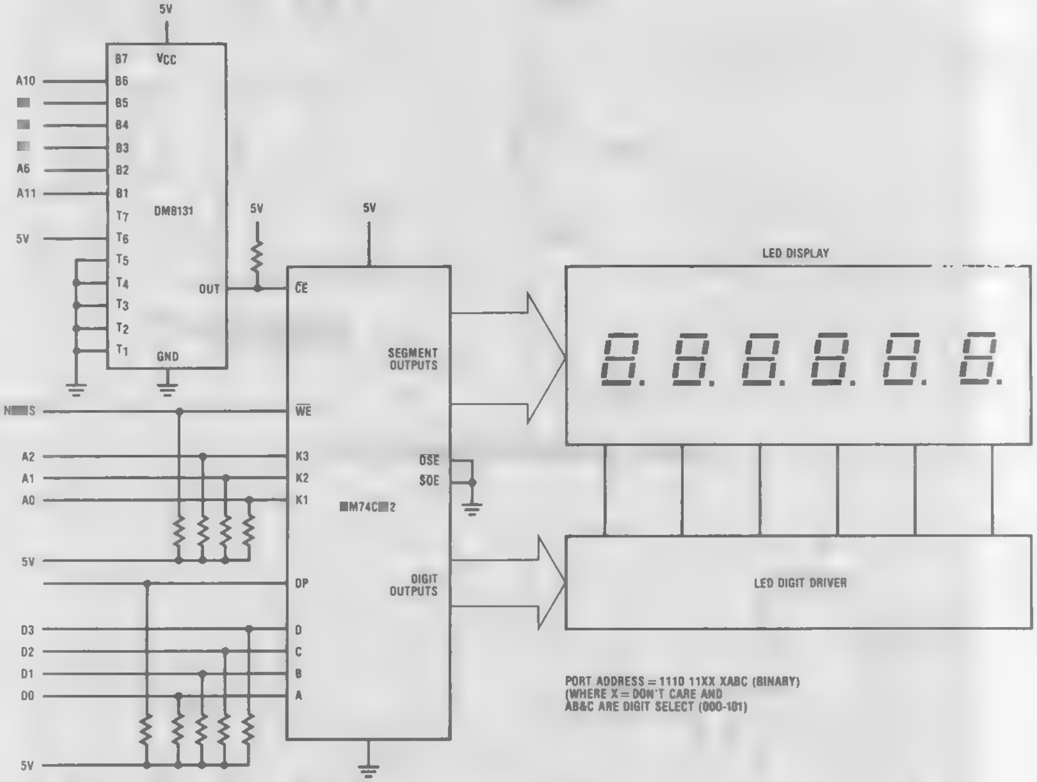
PORT ADDRESS = 0XXX XXAB (BINARY)
(WHERE X = DON'T CARE AND AB
ARE DIGIT SELECT (00-11))

Figure 29. NSC800 Interface to MM74C911



PORT ADDRESS = EXXA (HEX)
ADDRESS EXXA (HEX)
(WHERE X = DON'T CARE AND
"A" IS DIGIT SELECT (XX00-XX11)

Figure 30. MM74C911 to 6800 Microprocessor Interface



PORT ADDRESS = 1110 11XX XABC (BINARY)
(WHERE X = DON'T CARE AND
AB&C ARE DIGIT SELECT (000-101)

Figure 31. MM74C912/MM74C917 to INS8060 (SC/MP) Interface

signals. A typical method uses a 2–4 line decoder or a 3–8 line decoder. Where the total time from a stable address to the write pulse goes inactive is ≥ 1 μS, a CMOS decoder such as the MM74C42 or MM74C154 can be used, but if faster accessing is required, their LS equivalents should be employed.

Figure 32 shows a typical implementation of a 16-digit display using half of a DM74LS139 decoder to provide the $\overline{CE}$ signals for each controller.

G. Making The MM74C911/MM74C912/ MM74C917 Look Like RAM

So far, the discussion of addressing the controllers has been to separate the devices from memory, but there are certain advantages to not doing this. In many instances, microprocessor software requirements are such that data outputted to the controller also must be remembered by the microprocessor for later use. Since data cannot be read from the display controllers, the processor must also write the data in a spare register or stored in RAM simultaneously and can be read later by the CPU.

Figure 31 shows a simple example of this using an MM74C912 controller and two MM2114 1K × 4 memory chips. A DM74LS30 is used to detect when the last eight bytes of this memory is being accessed and enables the controller display. Thus, the last eight bytes of the RAM contains a duplicate copy of what the display controller is displaying.

IX. Conclusion

All three controllers provide simple and inexpensive interfaces to multiplexed multidigit displays. These devices are particularly well suited to microprocessor environments, but any type of CMOS compatible control hardware can be used. The MM74C911/MM74C912/ MM74C917 can most easily drive common anode displays. By providing most of the multiplex circuitry into one low-cost integrated circuit, the burden of designing discrete multiplexing has been eliminated.

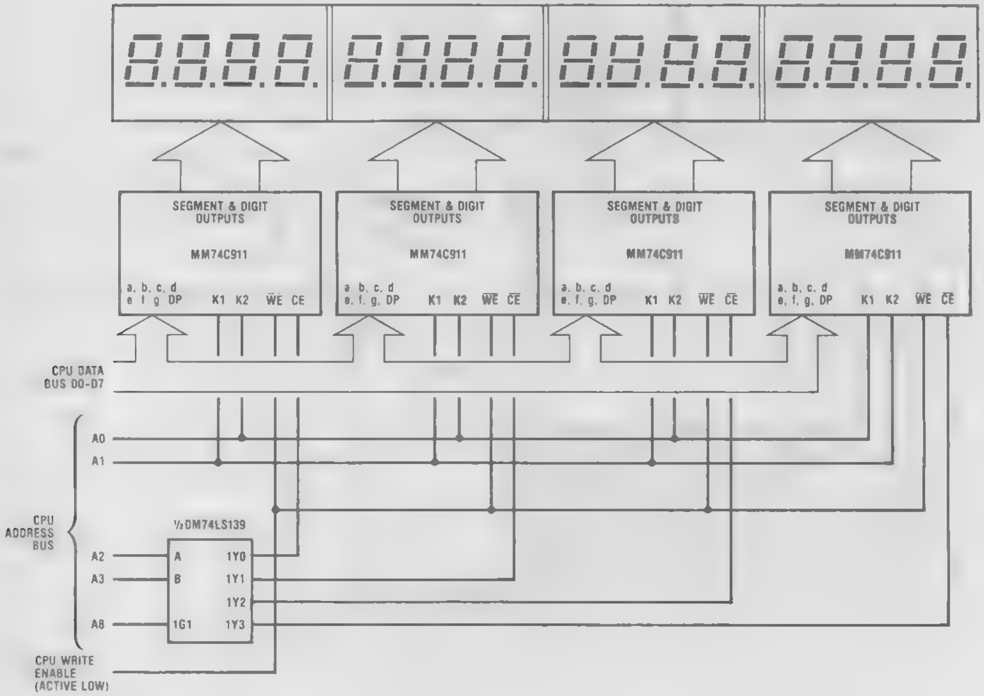


Figure 32. Multi-Digit Array

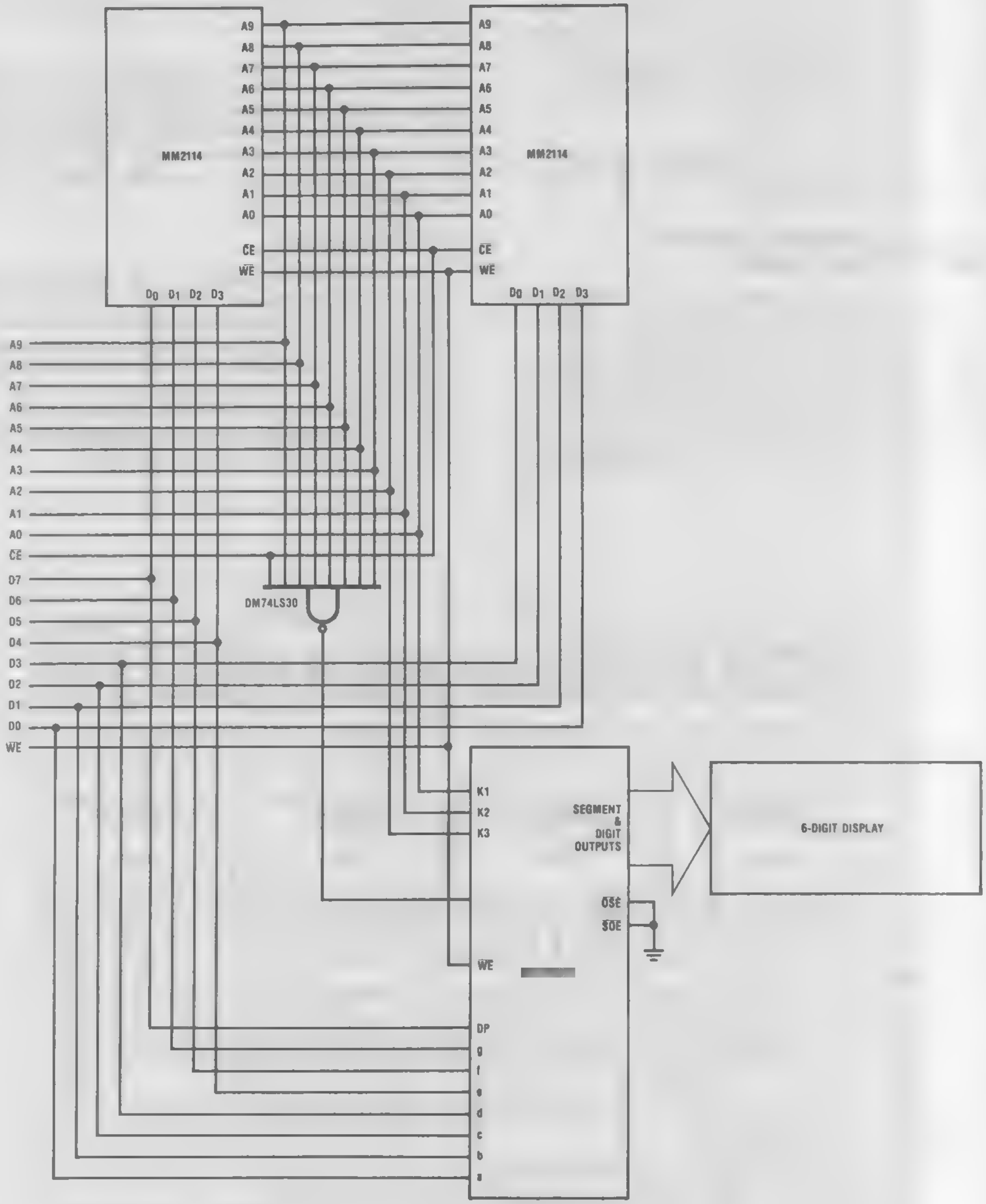


Figure 33. Display Controller Mapped Over RAM (5-10 KΩ Pull-up Resistors may be needed on MM74C912 Inputs)

Data Acquisition Using the ADC0816 and ADC0817 8-Bit A/D Converter with On-Chip 16 Channel Multiplexer

National Semiconductor
Application Note 258
Larry Wakeman
January 1981

I. Introduction

The ADC0816 and ADC0817, CMOS 16-Channel Data Acquisition devices are selectable multi-input 8-bit A/D converters. In addition to a standard 8-bit successive approximation type A/D converter, these devices contain a 16 channel analog multiplexer with 4-bit latched address inputs. They include much of the circuitry required to build an 8-bit accurate, medium through-put data acquisition system.

These two converters are similar to the ADC0808/ADC0809 A/D converters except that the ADC0816/ADC0817 have 16 analog inputs instead of 8, and the multiplexer output and the A/D comparator input are externally available. (The ADC0808/ADC0809 connect these internally.) This feature is useful when connecting signal processing circuitry to the A/D. Also the ADC0816/ADC0817 have an expansion control pin to allow addition of more multiplexers, hence more input channels.

The ADC0816 is identical to the ADC0817 except for accuracy. The ADC0816 is the more accurate part, having a total unadjusted error of ±½ LSB. The ADC0817 has a total unadjusted error ±1 LSB. In many applications where a slightly lower accuracy is tolerable, the ADC0817 represents a more economical solution.

II. Functional Description

The ADC0816/ADC0817 can be subdivided into two major functional blocks; a multiplexer/latch and an A/D converter, *Figure 1*. The multiplexer/latch is composed of a 16 channel multiplexer, a 4 bit channel select register, and some channel select decoding circuitry.

The channel select address is loaded on the positive transition of the Address Latch Enable (ALE) input.

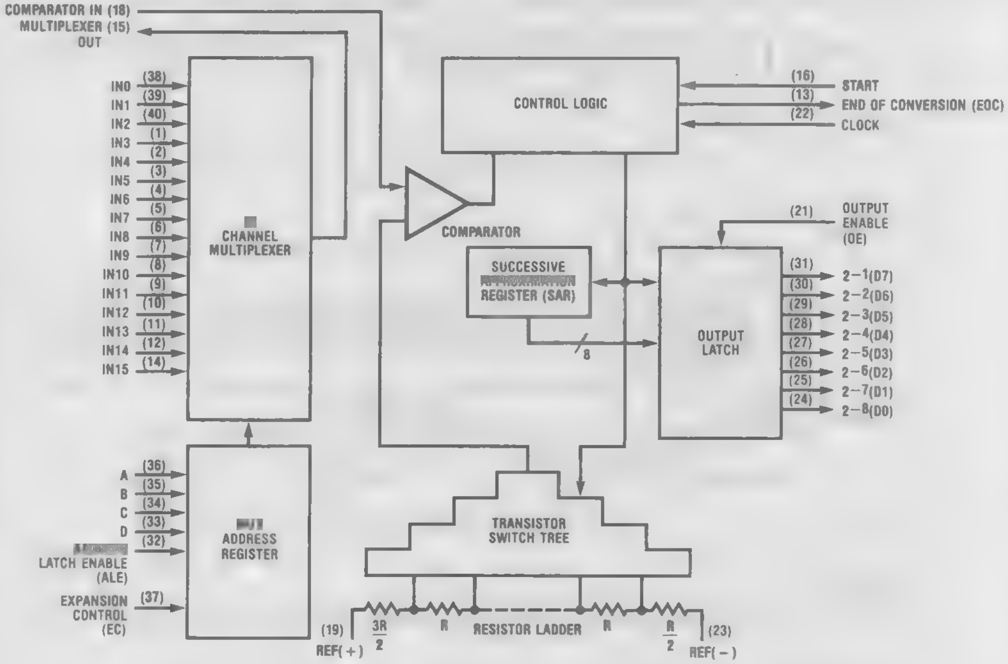


Figure 1. ADC0816/ADC0817 Functional Block Diagram

Figure 2 shows this addressing scheme. A multiplexer enable pin called Expansion Control (EC) is also provided. Taking this pin low will disable the on chip multiplexer, allowing other multiplexers to be used, thus expanding the number of inputs.

ADDRESS D	C	B	A	EXPANSION CONTROL	SELECTED CHANNEL
0	0	0	0	1	IN0
0	0	0	1	1	IN1
0	0	1	0	1	IN2
0	0	1	1	1	IN3
0	1	0	0	1	IN4
0	1	0	1	1	IN5
0	1	1	0	1	IN6
0	1	1	1	1	IN7
1	0	0	0	1	IN8
1	0	0	1	1	IN9
1	0	1	0	1	IN10
1	0	1	1	1	IN11
1	1	0	0	1	IN12
1	1	0	1	1	IN13
1	1	1	0	1	IN14
1	1	1	1	1	IN15
X	X	X	X	0	NONE

Figure 2. Analog Input Selection Table

The output of the multiplexer usually feeds the input of the second major functional block, the A/D converter. This converter is a successive approximation type converter that is composed of a comparator, 256R type resistor ladder, successive approximation register (SAR), control logic, and output data latch.

Under normal operation the control logic of the A/D will first detect a positive going pulse on the START input. On the rising edge of this pulse the internal registers are cleared, and will remain clear as long as START is high. When the START input goes low, the conversion is initiated. The control logic will cycle to the beginning of the next approximation cycle at which time End of Conversion goes low and the conversion is started. During a conversion, the control logic will select a tap on the resistor ladder, and route the signal through a transistor switch tree to the input of the comparator. The comparator will decide whether this tap voltage is higher or lower than the input signal and indicate this to the control logic. The control logic then decides which tap is to be selected next. Meanwhile, the SAR maintains a record of the conversion's progress. This algorithm takes 8 clock periods per approximation and requires 8 aproximations to convert 8 bits. Thus 64 clock periods are required for a complete conversion.

Once the entire conversion is completed the data in the SAR is loaded into the output register. This is a TRI-STATE® register which requires that its outputs be enabled by raising the Output Enable (OE or TRI-STATE) input. The data can then be read by the controlling logic.

During operation, the EOC output must be monitored to determine whether the device is actively converting or is ready to output data. Once the channel address is loaded, a positive going pulse on START will start the conversion and cause EOC to fall. When EOC goes high again the data is ready to be read, which, as was previously stated, is accomplished by raising the OE input. The data can be read any time prior to one clock period before the completion of the *next* conversion. The ADC0816/ADC0817 timing is shown in *Figure 3.* (See data sheet for exact specifications.)

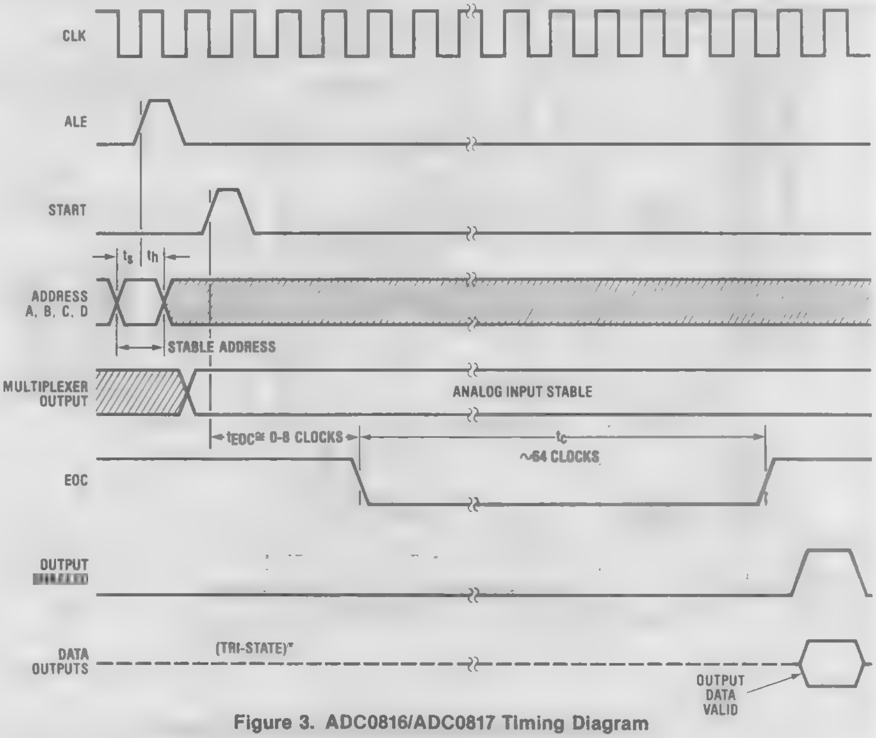


Figure 3. ADC0816/ADC0817 Timing Diagram

III. Analog Input Designs

A. Ratiometric Conversion

The external availability of both ends of the 256R resistor ladder makes this converter ideally suited to use with ratiometric transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full scale value. In other words, the actual value of the transducers output is of no great importance, but the ratio of this output to the full scale reference is valuable. For example, the potentiometric transducers of *Figure 4* have this feature.

The prime advantage of these transducers is that an accurate reference is not required. However, the reference should be noise free because voltage spikes during a conversion could cause inaccurate results.

Perhaps the simplest method to obtain a reference would be to use a voltage already present in the system, the power supply. As shown in *Figure 4* the 5V supply can be easily conected as the reference, but care must be taken to reduce power supply noise. The supply lines should be well bypassed with filter capacitors and it is recommended that separate PC board traces be used to route the 5V and ground to the reference inputs and to the supply pins.

B. Absolute Conversion

Absolute conversion refers to the use of transducers whose output value is not related to some other voltage. The "absolute" value of the transducer's output voltage is very important. This implies that the reference must be very accurately known to be able to accurately determine the value of the transducers output. *Figure 5* shows a typical grounded reference connection using the LM336-5, 5V reference. Note that ratiometric transducers can also be used in this application along with absolute transducers.

In most of the following applications either absolute or ratiometric transducers can be used. The only difference being that when absolute transducers are employed, more accurate references should be used.

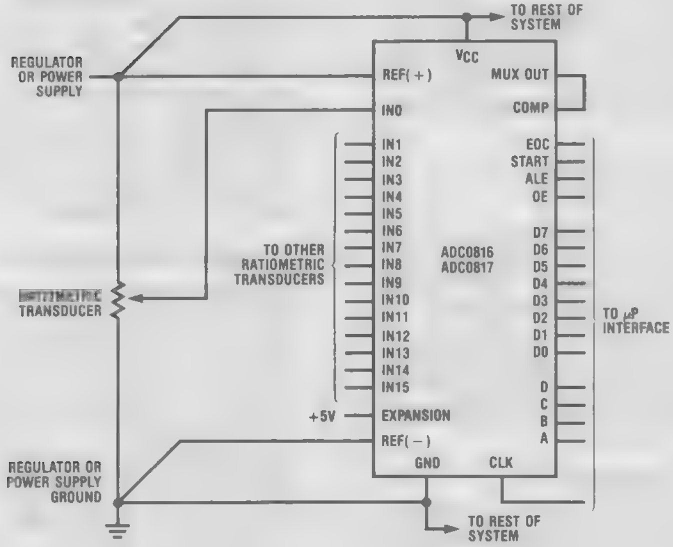


Figure 4. Simple Ratiometric Converter Using Power Supply as Reference

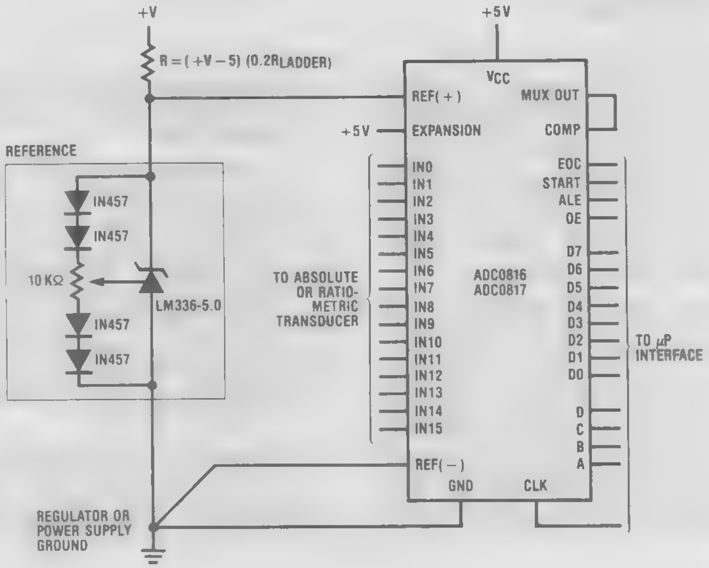


Figure 5. Simple Absolute Converter Using LM336-5.0 Converter

C. Reference Manipulation

In some small systems (particularly CMOS systems) where a reference is required, one can use the reference as a supply as shown in *Figure 6*. In this case the LM336-5 is used to generate the 5V reference and also the 5V supply. An unregulated supply greater than 5V is required to allow the reference to operate. The series resistor, R, is chosen such that the maximum current needed by the system is supplied while keeping the LM336-5 in regulation. The value of this resistor is simply:

$$R = \frac{V_S - V_{REF}}{I_{AD} + I_{TR} + I_p + I_R}$$

where V_S = unregulated supply voltage; V_{REF} = reference voltage; $I_{LAD} = V_{REF}/1\,K\Omega$, resistor ladder current; I_{TR} = transducer currents; I_p = system power supply requirements; and I_R = minimum reference current.

Figure 7 shows a simple method of buffering the references to provide higher current capabilities. This eliminates the I_p term in the above equation. In Figures 5, 6, and 7, it is advisable to add some supply bypass capacitors to reduce noise, typically 0.1 μF.

D. Reference Voltage Variation

In some cases it is possible to eliminate the need for gain adjustments on the analog input signals by varying the Ref(+) and Ref(−) voltages to achieve various full scale ranges. The reference voltage can be varied from 5V to about 0.5 volts with the one restriction that $[V_{Ref(+)} - V_{Ref(-)}]/2 = (V_{CC} - GND)/2 \pm 0.1$ volts. In other words, the center of the reference voltage must be within ±0.1V of mid-supply. The reason for this is that the reference ladder is taped by an n or p-channel MOSFET switch tree. Offsetting the voltage at the center of the switch tree from $V_{CC}/2$ will cause the transistors to incorrectly turn off, resulting in inaccurate and erratic conversions. However, if properly applied, this method can reduce parts counts as well as eliminate extra power supplies for the input buffers.

Figure 8 shows a simple supply centered reference where R1 and R2 offset Ref(+) and Ref(−) from V_{CC} and Ground. An LM336, 2.5V reference is shown here, but any reference between 0.5V and 5V can be used. For odd reference values the simple op amp scheme shown in *Figure 9* can be used. Single power supply op amps such as the LM324's or LM10's would work well. R1, R2, and R3 form a resistor divider in which R1 and R3 center the reference at $V_{CC}/2$ and R2 can be varied to obtain the proper reference magnitude.

E. Analog Channel Expansion

The ADC0816/ADC0817 have an expansion control (EC) pin which is actually a multiplexer enable. When this signal is low, all the switches are inhibited so that another signal can be applied to the comparator input. Additional channels can be implemented very simply, as shown in *Figure 10*. This design has expanded the number of channels from 16 to 32. To address the channels, 5 address lines are required. The lower 4 bits are directly applied to the A/D's A, B, C, and D inputs. All 5 bits are also applied to an MM74C174 Hex "D" flip-flop which is used as an address latch for the two CD4051's. The 1Q, 2Q, and 3Q outputs of the MM74C174 feed the CD4051 address inputs 4Q and 5Q are gated to form enable signals for each CD4051. 5Q is also routed to the EC input to properly enable the A/D's multiplexer.

The CD4051s are used with a 5V supply, so their specifications are very similar to the ADC8016/ADC0817 multiplexer. Thus, anything that can be done with the ADC0816/ADC0817 multiplexer can be done with the CD4051's. This includes making use of the previously discussed input designs as well as others.

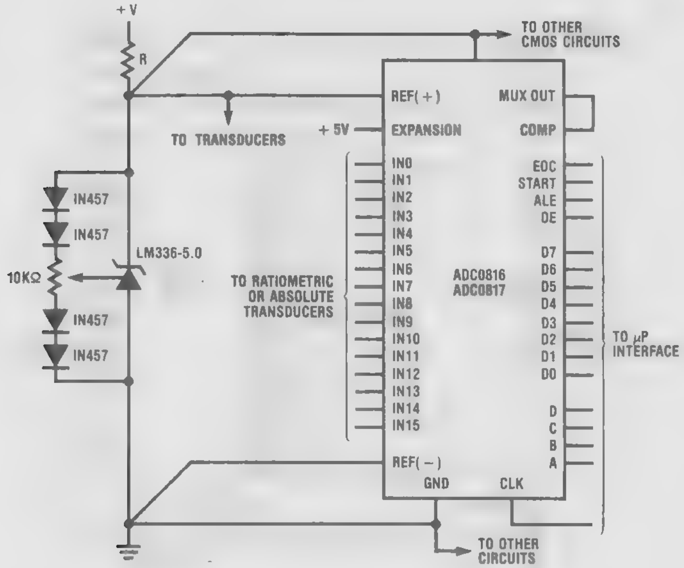


Figure 6. Reference Used as Power Supply

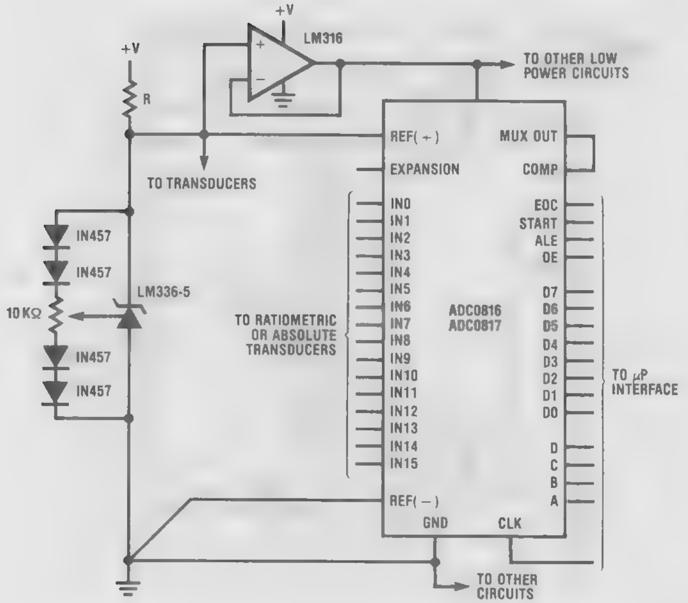


Figure 7. Buffered Reference Used as Power Supply

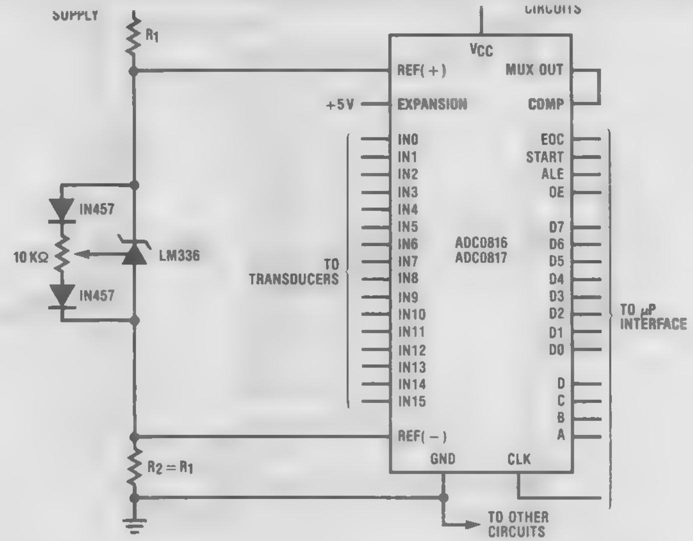


Figure 8. Supply Centered Reference Using LM336 2.5V Reference

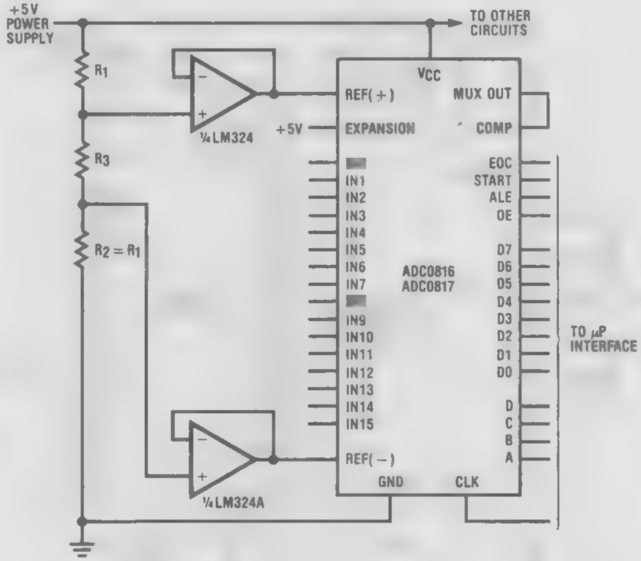


Figure 9. Supply-Centered Reference Using Buffered Resistor Divider

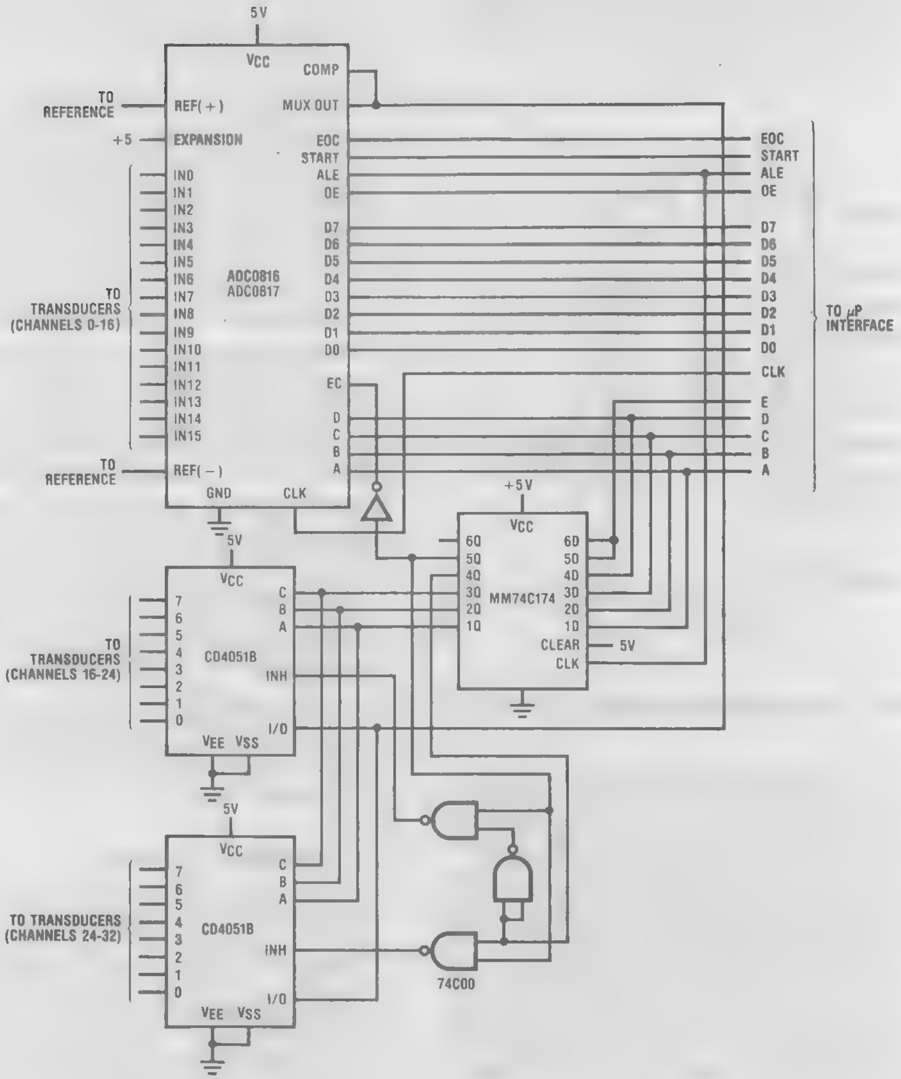


Figure 10. Simple 32 Channel A/D Converter

F. Differential Analog Inputs

An easy, and sometimes overlooked method for implementing a differential input scheme is shown in *Figure 11.* This approach actually implements the differential in software. All 16 channels are paired into positive and negative inputs. Then the controlling logic or microprocessor will convert each channel of a differential pair, load each result, and then subtract the two results. This method requires two single ended conversions to do one differential conversion, hence the effective differential conversion time is twice that of a single channel or a little over 200 μs (Ck = 640 kHz). The differential inputs should be stable throughout both of the conversions to produce accurate results.

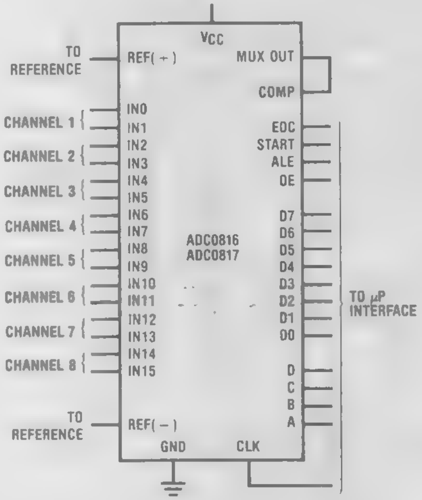


Figure 11. Simple 8 Differential Channel Converter

A 16 channel differential system can be realized by modifying *Figure 10.* This is accomplished by changing the CD4051's addressing and adding a differential amplifier in between the multiplexer outputs and the comparator input. The select logic for the CD4051's has been modified to enable the switches to be selected in parallel with the ADC0816/ADC0817. The outputs of the three multiplexers are connected to a differential amplifier, composed of 2 inverting amplifiers with gain and offset trimmers. A dual op amp configuration of inverting amplifiers can more easily be trimmed and has less stringent feed-back resistor matching requirements, as compared to a single op amp design. The transfer equation for the dual op amp amplifier shown in *Figure 12* is:

$$V_o = \left[\frac{R_2R_5}{R_1R_3}\right]V_1 - \left[\frac{R_5}{R_4}\right]V_2$$

Propagation delay through the op amps should be considered to provide sufficient time between the analog switch selection and start conversion to allow the analog signal at the comparator input to settle. Using the LF356 op amp, this delay should be about 5μs.

G. Input Signal Buffering

There are three basic ranges of input signal levels that can occur when interfacing the ADC0816/ADC0817 to the "real world". These are: a) signals which exceed V_{CC} and/or go below ground; b) signals whose input ranges are less than V_{CC} and Ground, but are different than the reference range; c) and signals that have an input range that is equal to the reference range. Each of these situations require different buffering.

The last situation, case "c" is usually trivial. No buffering is required unless the source impedance of the input signal is very high. If this is the case a buffer may be added between the multiplexer output and comparator input pins. If a high input impedance op amp is used, the input leakage looking from the multiplexer input can be greatly reduced. This circuit is shown in *Figure 13.* Using a buffer like this eliminates the necessity for large capacitors on the multiplexer inputs (explained later), but these buffers usually require two supplies and can contribute their own conversion errors.

If the input signal is within the supply, but the reference cannot be manipulated to conform to the full input range, the unity gain buffer of *Figure 13* can be replaced by another op amp as shown in the *Figure 13* inset. This type of amplifier will provide gain and/or offset control to create a full scale range equal to the reference.

The third case, c, where the input range exceeds V_{CC} and/or goes below ground, the input signals must be level shifted before they can go to the multiplexer with the only exception being when the magnitude of the input voltage range is within 5V, but outside the 0-5V supply range. In this case the supply for the entire chip could be shifted to the analog input range, and the digital signals level shifted to the system's 5V supply.

A typical example would be bipolar inputs from −2.5V to +2.5. If the ADC0816/ADC0817 have their supply and reference derived as shown in *Figure 14*, then the ±2.5V logic outputs need only to be level shifted to 0 and 5V logic levels, *Figure 15.*

H. Digital Data Acquistion

The ADC0816/ADC0817 make good analog data acquisition subsystems, but there are many instances where these converters are good digital data acquisition systems as well. If a system has unused channels, digital inputs can be connected to these channels instead of being separately buffered into the system. In the case of a microprocessor system this could eliminate an I/O port and associated logic. The speed at which this input is accessed is one conversion cycle, but many times this will be fast enough. These inputs can be used as input switches, power supply indicator devices, or other system status flags. The microprocessor converts the digital input channel and reads it. Software then decides whether the input is high enough or low enough to cause a particular action.

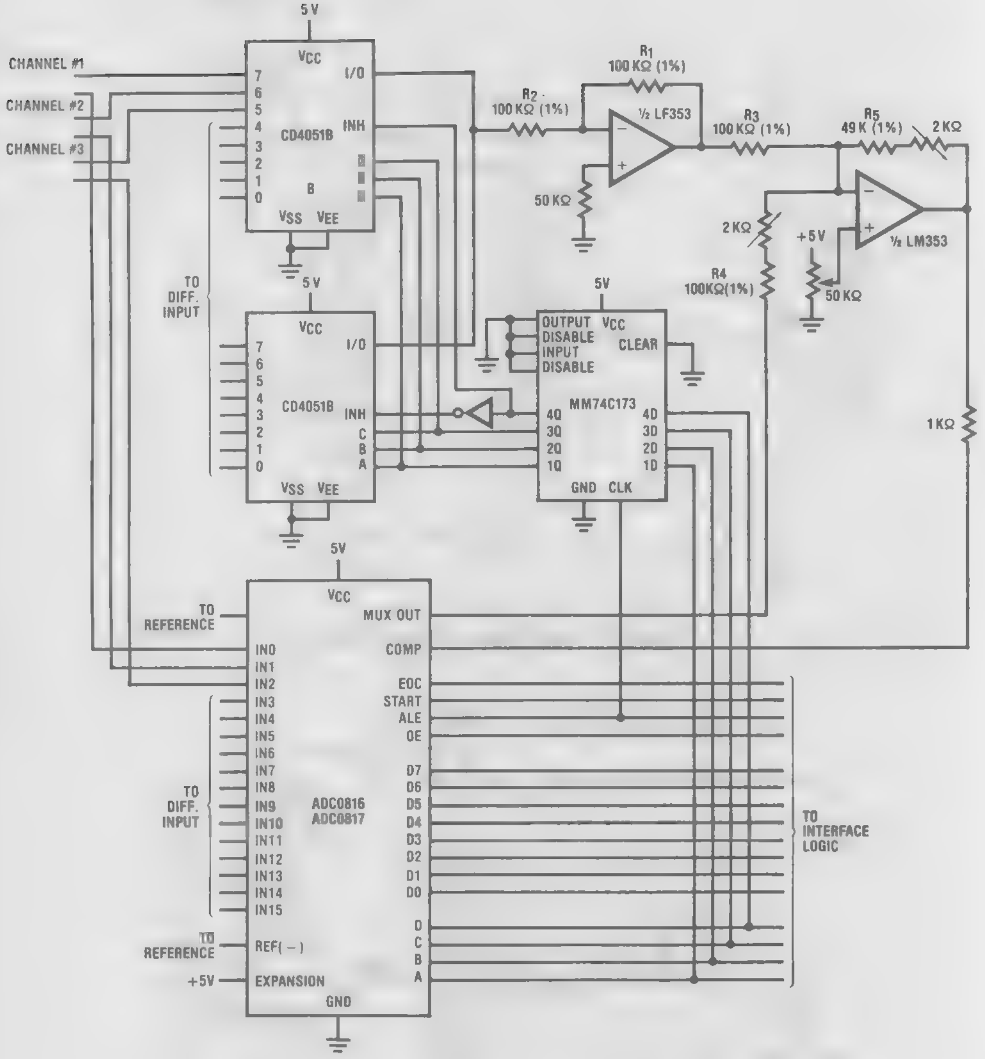


Figure 12. Differential 16 Channel A/D Converter

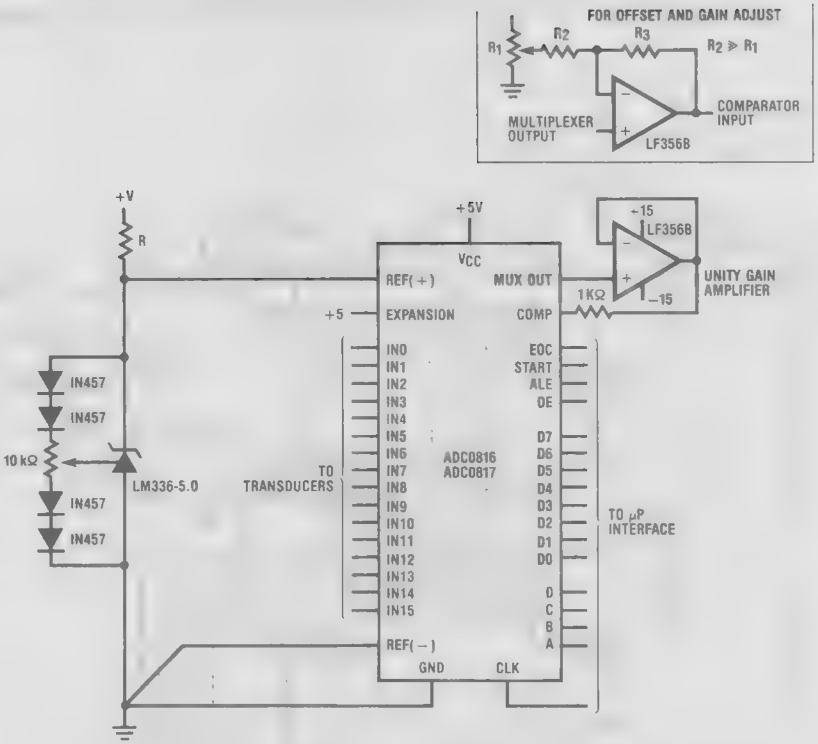


Figure 13. Single Input Amplifier Buffering

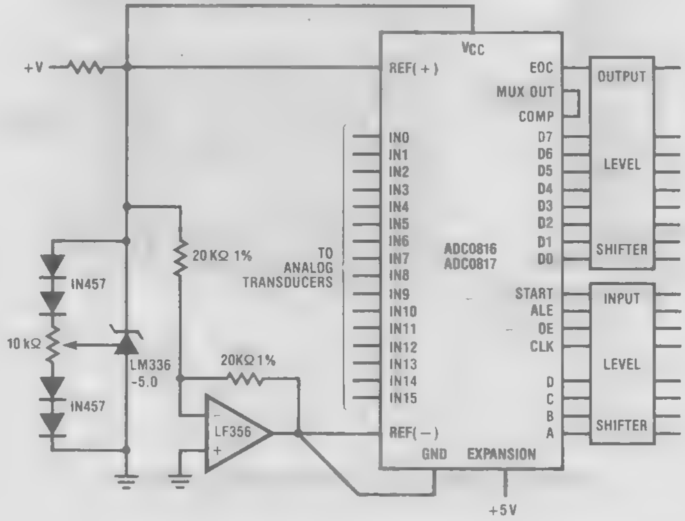


Figure 14. ±2.5V Input Range Data Acquisition

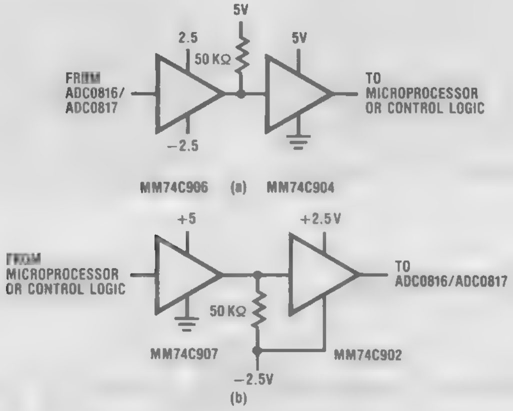


Figure 15. Input/Output Level Shifters

I. Input Considerations

In most instances interfacing analog circuitry is very straightforward, but there are some constraints that should be observed if a reliable accurate system design is to result. One major consideration, input source impedance is actually somewhat more complicated than it appears. One would expect that the input current would be a small D.C. current, but due to the nature of the comparator, it is not. The A/D's comparator is a capacitor sampling comparator whose input current is a series of spikes. *Figure 16* shows a simplified model of the comparator input.

When determining a single bit value during a conversion, S1 will close causing C_C and C_p to charge to the input voltage. Then S1 is opened and S2 is closed sampling the ladder. The input current is an RC transient charging current whose magnitude and duration is dependent on the values of C_c, C_p, R_s, R_m and R_L. The duration of the transient must be shorter than the input sample period, and the sample period is dependent on the converter's clock frequency. Thus the maximum source impedance is dependent on the clock period. At a clock frequency of 1 MHz, $R_s \leqslant 1k$; and at 640 kHz, $R_s \leqslant 2k$. The source impedance of potentiometric transducers vary as a function of wiper position. Thus transducers with a value of $\leqslant 10k$ at a frequency of 640 kHz and $\leqslant 5k$ at 1 MHz are suitable.

When a sample-and-hold or some other active device is inserted between the multiplexer and comparator pins, the output impedance of the transducers are no longer as restricted and depend more on the particular Sample/Hold or op amp chosen. The critical parameter now is the source impedance of the buffer which should be $\leqslant$ 3k at a clock frequency of 1 MHz and $\leqslant$ 5kΩ with the clock equal to 640 kHz.

If higher impedances are unavoidable, RC charging errors can be reduced to an average current error by placing a capacitor = 1 μF, from the multiplexer input to ground. Adding this capacitor will average the transient current spikes and cause a small DC current error which for a potentiometric transducer is:

$$V_{ERR} = \frac{Rp}{8}(I_{IN})\frac{Ck}{640\,kHz}\text{ Volts}$$

where Rp = total potentiometer resistance; $I_{IN} = 2\mu A$ (maximum input current at 640 kHz); and Ck = clock frequency. For a standard buffer source impedance the voltage error is:

$$V_{ERR} = I_{IN}(R_s)\ \frac{Ck}{640\,kHz}\text{ Volts}$$

where R_s = buffer source impedance; $I_{IN} = 2\mu A$ (maximum average input current at 640 kHz); and Ck = clock frequency.

In addition, whenever analog signals are present in a digital system, several precautions should be exercised to reduce noise on the analog inputs. The analog input signals and the reference input should be kept physically isolated from the digital signals and a single point analog ground should be employed.

J. Protecting the Analog Inputs Against Over Voltages

During normal operation, it is important to keep the analog input voltages to the multiplexer or comparator between V_{CC} and Ground to ensure proper operation. There may be some occasions where over or under voltages cannot be avoided. Protecting the analog inputs, due to their unique nature, can be more difficult than digital inputs. The most effective method is to use external Schottky diodes as shown in *Figure 17a*. Since the Schottky knee voltage is 0.4 volts the IN5166 diodes of *Figure 17a* will safely shunt currents up to several milliamps. To shunt possible currents larger than several milliamps some series resistance may be added to limit these currents as shown in *Figure 17b*, but this value resistor must be no greater than the values specified in the previous section.

A less expensive solution would be to replace the Schottky diode with some standard switching diodes, *Figure 17b*, but since these diodes could only partially shunt the input current from the internal clamp diodes, some series resistor should be used as in *Figure 17c*. If the external diode must shunt a large amount of current the two series resistors of *Figure 17d* should be used. If the input design is such that the input can exceed only one supply the diode going to the other supply can be omitted.

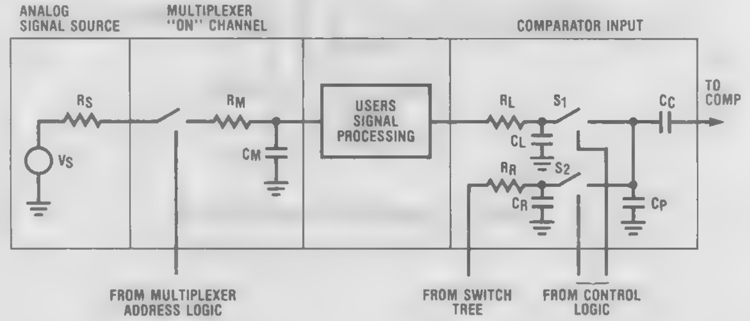


Figure 16. Simplified Multiplexer/Comparator Equivalent Circuit

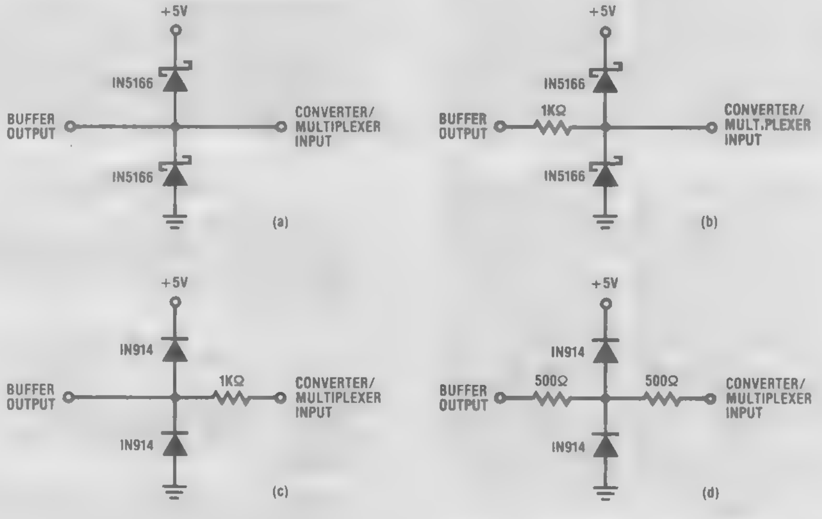


Figure 17. Analog Input Protection Circuitry

IV. Signal Conditioning

There are many applications where it is desirable to add some signal processing circuitry to improve circuit performance. Typical additions would be filter circuits, sample/holds, gain controlled amplifiers, and others. Here again the external accessibility of the multiplexer output and comparator input pins can greatly reduce the amount of circuitry required by enabling the use of only one circuit required by enabling the use of only one circuit all 16 outputs instead of 1 for each input.

A. Gain Control

Previous examples of gain manipulation have dealt with one fixed gain for all 16 channels, but there are occasions where variable gain or selectable gain may improve accuracy and simplify hardware and/or software.

Figure 18 shows a typical method for gain control. The CD4051, analog multiplexer, is placed in the feedback loop of a simple non-inverting op amp. The gain of this op amp is controlled by selecting one of the CD4051's analog switches. This will switch a resistor in and out of the feedback loop. If these resistors, R_{2N}, are of different values, different gains are realized. These gains are given by:

$$A_V = 1 + \frac{R_{2N}}{R_1}$$

A microprocessor or some control logic would select a gain by latching the channel address into a MM74C173. It is important to ensure the output of the LF356B does not exceed the power supply, so before a new channel is selected the gain of the op amp should be reduced to a safe value. The 1k resistor on the output of the LF356 is to help protect the comparator inputs from accidental over or under voltages. Two back biased diodes placed from the input to V_{CC} and Ground (IN914 or Schottky) will offer further protection.

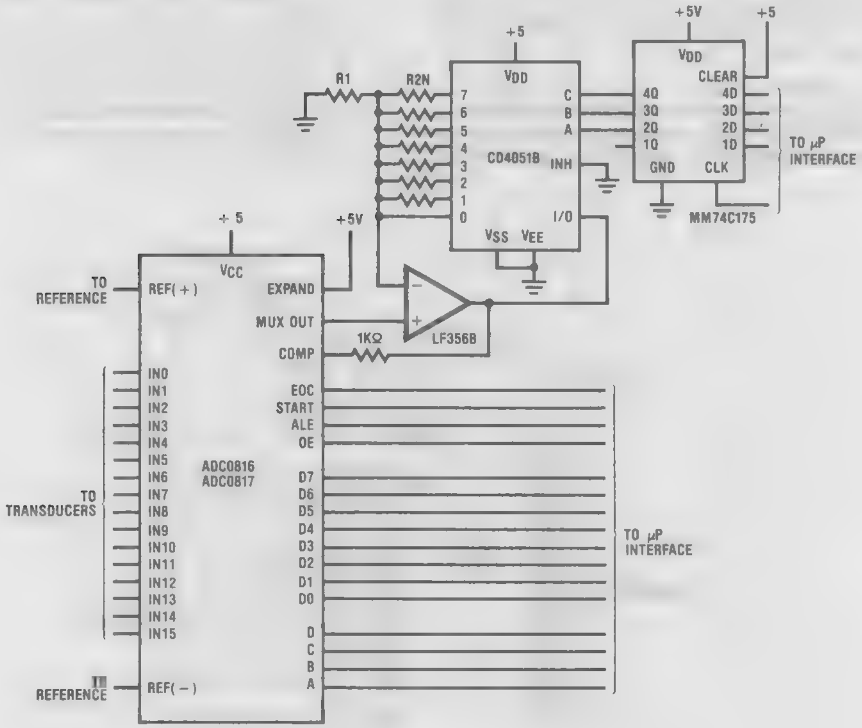


Figure 18. Microprocessor Controlled Gain

B. Sample/Holds

The only major data acquisition element not included on the ADC0816 is a sample/hold circuit. If the input signals are fast moving then a S/H should be used to quickly acquire the signal and then hold it while the ADC0816/ADC0817 converts it. This circuit can be easily implemented by inserting it between the multiplexer output and the comparator input.

The simplest solution is to tie a capacitor on the multiplexer output and then tie this pin to the comparator input pin. The expansion control pin is used as a sample control. When this pin is high one switch is on and the capacitor voltage will follow the input. However, when the expansion control pin is pulled low, all switches are turned off and the capacitor holds its last value, almost. The input bias to the comparator is about 2μA (worst case with Ck = 640 KHz). Thus the droop rate for a 1000 pF is approximately 2000 V/S or about 0.2 V/conversion. This is totally impractical. If a 0.01 μF capacitor is used instead then the droop rate is 20 mV, which may be satisfactory. Unfortunately, the acquisition time is on the order 100 μS, or about the length of a conversion.

The problem is that the comparator input leakage is too high for this sample and hold. To eliminate this, the input can be buffered by using an LM356B. *Figure 19.* The leakage, now due mostly to multiplexer leakages, is reduced to approximately 100 nA. The droop per conversion is typically less than 1.0 mV per conversion when using a 1000 pF capacitor and the acquisition time is approximately 20 μS.

A more accurate solution would be to isolate the capacitor from both the multiplexer comparator pins of the ADC0816/ADC0817. This is easily accomplished by using the LF398 monolithic sample/hold, as shown in *Figure 20.* The acquisition time for this part is typically 4 μS to 0.1%, and the droop rate is 20 μV/conversion. This circuit has its own hold control thus the expansion control is free to be used normally.

The choice of the hold capacitor is critical to the performance of the sample/hold circuit. Some capacitors are composed of dielectrics that will have an initial droop after the hold is strobed. This is due to dielectric absorption. Polypropylene and polystyrene dielectrics have very little dielectric absorption and thus make excellent sample/hold capacitors. Such materials as mylar polyethylene have higher absorption properties and should not be used.

C. Filtering Analog Inputs

Under some conditions the analog input may have come from a noisy environment and to recapture the original signal some filtering may be required. Typically high frequency noise must be filtered. The ADC0816/ADC0817 can easily accommodate the addition of many standard low pass filters. Another useful filter is a 50 Hz or 60 Hz notch filter to eliminate the nose contributed to the circuit by A.C. power lines.

It is particularly easy to place a single passive filter between the multiplexer output and comparator input pins, but passive filters must be carefully designed to reduce input loading. The filter capacitor will tend to average the comparator sampling current as mentioned in the Input Considerations section. To eliminate this, the passive filter can be buffered by an op amp or an active filter could be used.

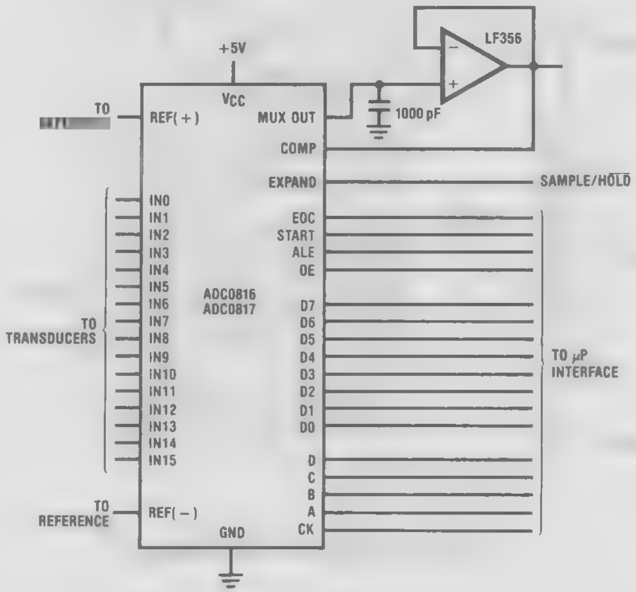


Figure 19. Op Amp Sample Hold Circuit

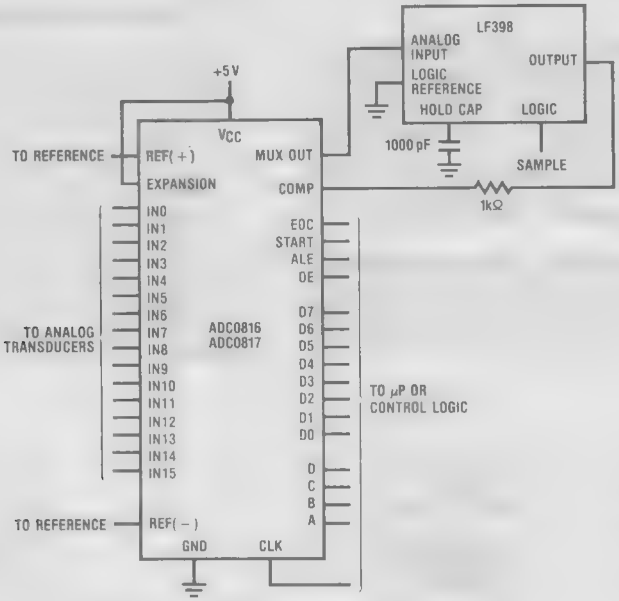


Figure 20. Sample/Hold Converter Using LF398

V. Microprocessor Interface

The interface requirements for the ADC0816/ADC0817 interconnection to various microprocessors are essentially the same as the ADC0808/ADC0809 requirements. The devices can be connected to the CPU so that it looks either like a memory location or I/O port. The data transfers can be initiated by either an interrupt to the CPU or the CPU can periodically interrogate the A/D. When trying to implement an absolute minimum components count system, the I/O port (as opposed to memory) addressing will usually require fewer components.

There are several design considerations that apply to most microprocessor systems when interfacing the ADC0816/ADC0817. Even though the actual timing of CPU read and write cycles vary, in general, a microprocessor will output the address and data (if write operation) onto its busses. A certain time later the Read or Write strobes will go active for a specified time. The interface logic must detect the state of the address and data busses and initiate the specified action. For the ADC0816/ADC0817 these actions are; 1) load channel address, 2) start conversion, 3) detect end of conversion and 4) read resultant data. These actions are performed by decoding the read/write strobes, address, and data information to form the and ALE and START pulses, then detect EOC, and finally read the data.

For the most part the decoding and strobe generation is straight forward. The START, ALE, and OE strobes will generally be of the same duration as the CPU read/write strobes and positive going (ALE can be negative going). One subtle choice is where to derive the A, B, C, and D channel select address. These lines can be connected to either the address bus or the data bus. The advantage of connecting them to the data bus is that in minimum systems, more I/O address lines are available for simple decoding. When the A, B, C, and D inputs are connected to the address bus each analog channel becomes a separate I/O port.

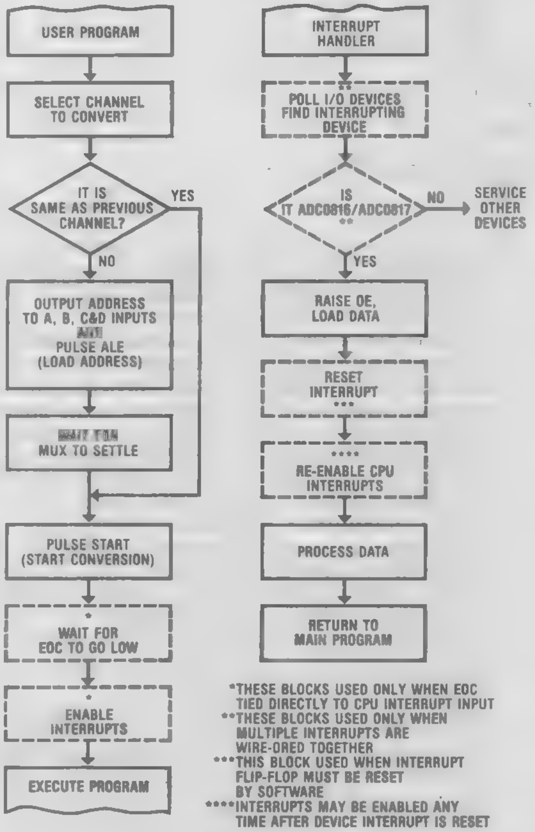
In most designs it is very tempting to tie START and ALE together, enabling one pulse to both write the channel address and then start the conversion. However, it is very important that the signal on the comparator input be stable before the conversion starts, otherwise the first and most important successive approximation could be in error. Usually the START and ALE pulses are the same length as the CPU read and write strobes which are normally between 0.2 to 1.μS long. Thus the conversion may start within 1μS of the address select latching. (Remember the channel is selected on the rising edge of ALE and the conversion begins within 8 clock periods of the falling edge of START.) For converter clocks greater than 500 KHz, 1μS may not be enough time to allow the analog input signal to propagate through the multiplexer and any additional signal conditioning circuitry such as buffers, S/H's, etc. There are, however, a couple of easy fixes that can correct this possible problem. First, the START/ALE pulse could be stretched to the proper length by using a one-shot (MM74C221 or similar) to generate a pulse as long as the total delay from multiplexer input to comparator input. Secondly, the problem can be circumvented by "double pulsing" the converter. This can be easily accomplished in software by writing to the START/ALE address twice. The first pulse latches the desired channel address and starts the conversion. The second pulse must again load the same channel address, which will not change the multiplexer's state, and will then restart the conversion. Of course, the second pulse must occur after the comparator input has settled.

Even though the hardware to interface the ADC0816/ADC0817 to various microprocessors will differ and the system software will vary, the basic routines to operate the ADC0816/ADC0817 are usually similar. There are many variations, but *Figures 21 & 22* illustrate flow charts that typify these routines. These routines

This does not necessarily have to be true, but write instructions are conceptually easier and little is gained by designing the logic such that read instructions intiate these pulses. The OE pulse must be created by an I/O or memory read as the converter's data must be read.

The major design consideration is whether EOC should be polled by the microprocessor or whether EOC should cause an interrupt. This decision is system dependent, however the following applications illustrate both methods.

group have separate I/O read ($\overline{\text{I/OR}}$) and I/O write ($\overline{\text{I/OW}}$) strobes which imply that the INS8080 has separate I/O addressing. In small systems this means that very little or no address decoding is necessary. *Figure 23* shows a very simple interface which uses two NOR gates to gate the I/O strobes with the most significant address bit A7. The INS8080 has 8 bits of port address which will yield a maximum of 4 I/O ports if inputs A, B, C, and D are connected to the address bus. A MM74C74 flip-flop is used as a divide-by-2 to generate a converter clock of 1MHz. If the INS8080 system clock is ≤1MHz this flip-flop is unnecessary.



*THESE BLOCKS USED ONLY WHEN EOC TIED DIRECTLY TO CPU INTERRUPT INPUT

**THESE BLOCKS USED ONLY WHEN MULTIPLE INTERRUPTS ARE WIRE-ORED TOGETHER

***THIS BLOCK USED WHEN INTERRUPT FLIP-FLOP MUST BE RESET BY SOFTWARE

****INTERRUPTS MAY BE ENABLED ANY TIME AFTER DEVICE INTERRUPT IS RESET

Figure 21. Flow Chart for Interrupt Control of ADC0816/ADC0817

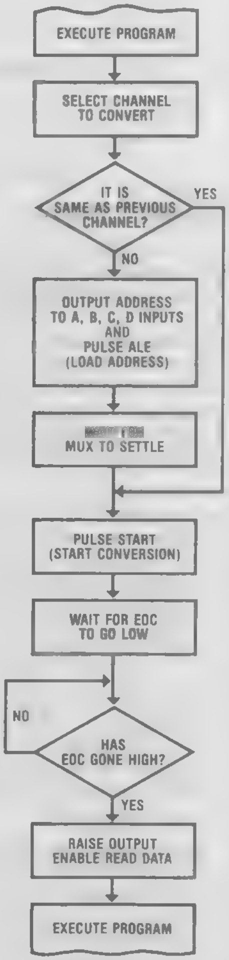

EXECUTE PROGRAM
SELECT CHANNEL TO CONVERT
IT IS SAME AS PREVIOUS CHANNEL?
YES
NO
OUTPUT ADDRESS TO A, B, C, D INPUTS AND PULSE ALE (LOAD ADDRESS)
WAIT FOR MUX TO SETTLE
PULSE START (START CONVERSION)
WAIT FOR EOC TO GO LOW
NO
HAS EOC GONE HIGH?
YES
RAISE OUTPUT ENABLE READ DATA
EXECUTE PROGRAM

Figure 22. Flow Chart to Control ADC0816/ADC0817 in a Polled I/O Mode

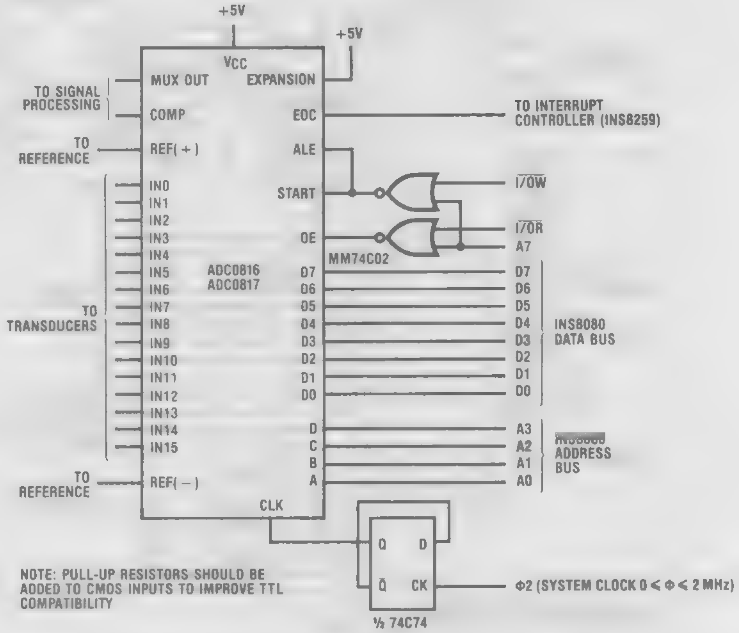


Figure 23. Simple INS8080/8224/8228 to ADC0816/ADC0817 Interface

Typical software would first write the channel address to the converter and start it. As mentioned before, two start pulses should be sent to the ADC0816/ADC0817 to allow the comparator input to settle. After the second start pulse the CPU could execute other program segments until it is interrupted by EOC going high. Depending on the interrupt structure, program control would then be given to the interrupt handler which reads the converter's data.

The second interface circuit, *Figure 24* utilizes a DM74LS139 dual 2-4 decoder in which one-half of the chip is used to create read pulses and the other half write pulses. The START and OE inputs are inverted to provide the correct pulse polarity. This interface partially decodes A6 and A7 to provide more I/O capabilities than before. This circuit also implements a simple polled I/O structure. The EOC output is placed on the data bus by a TRI-STATE® inverter when the inverter is enabled by an INS8080 read.

B. Interfacing to the Z80™

The Z80™, even though architecturally similar to the INS8080, uses slightly different control lines to perform I/O reads and writes. In *Figure 25* a NOR gate approach similar to *Figure 22* is shown to interface the Z80 to the ADC0816/ADC0817. Instead of $\overline{\text{I/OR}}$ and $\overline{\text{I/OW}}$ strobes the Z80™ has $\overline{\text{RD}}$ (read) and $\overline{\text{WR}}$ (write) strobes which are gated with $\overline{\text{IOREQ}}$ (I/O request). In the Z80™ interface, to show a slight variation, START is connected to OE instead of ALE. This will cause a new conversion to be started whenever the data is read which may seem unusual, but can actually be useful if the converter is to be continually restarted upon completion of the previous conversion. Address bit A6 is used to derive a strobe which will place EOC on the data bus to be read by the CPU.

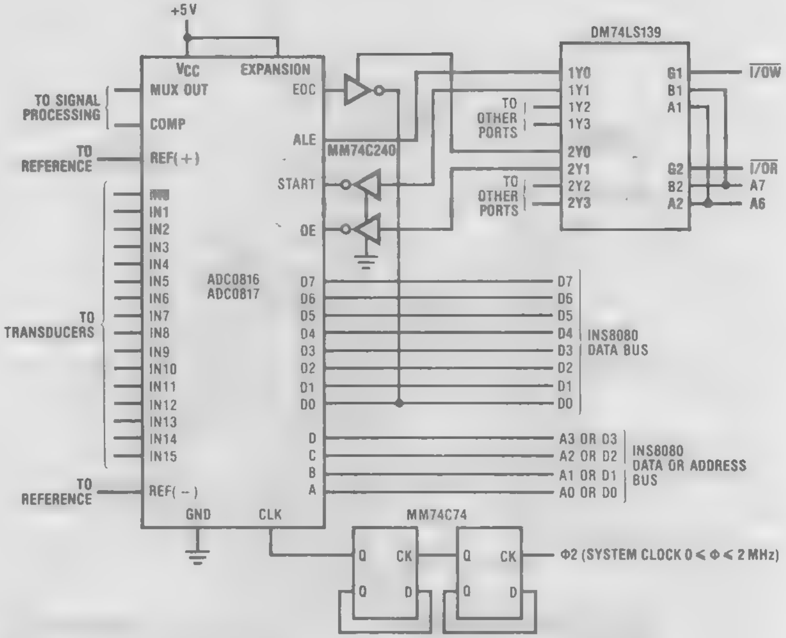
Figure 26 uses a 6 bit comparator to decode A4-A7 and $\overline{\text{IOREQ}}$. Two NOR gates are used to gate the ALE/START and OE pulses. This design functions the same as *Figure 23* except that the DM8131 provides much more decoding.

C. Interfacing to the NSC800

The NSC800 interface is actually very similar to the INS8080 I/O interface, even though their timing is very different. The NSC800 multiplexes the lower 8 address bits on the data bus at the beginning of each cycle. When accessing memory, A0-A7 must be latched out at the beginning of a read or write cycle, but for I/O accessing; the NSC800 duplicates the 8 bit I/O addresses on A8-A15 address lines and latches are not necessary since these lines aren't multiplexed. The I/O read and write strobes are derived from a $\overline{\text{RD}}$ (read) and $\overline{\text{WR}}$ (write) line and the IO/$\overline{\text{M}}$ signal.

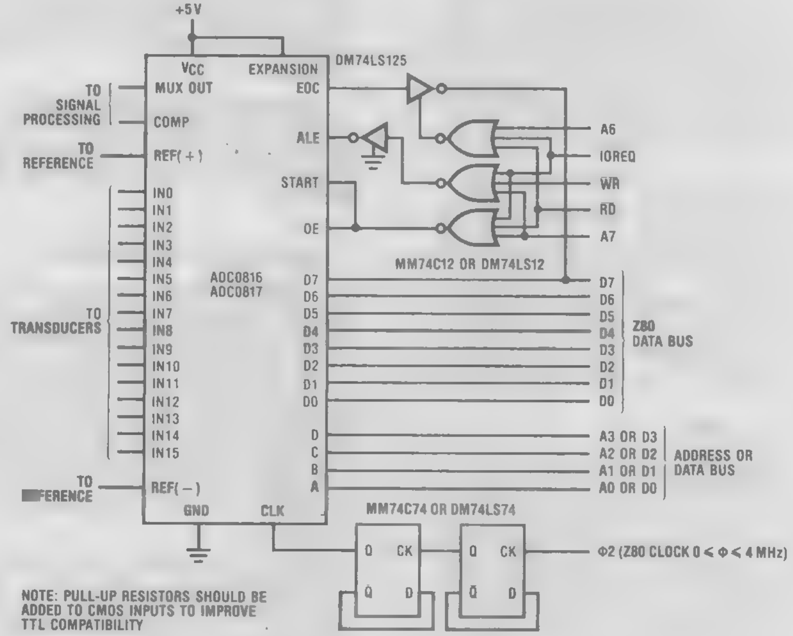
Figure 27 shows a design using a dual 2-4 line decoder which decodes A15, and A14 and is enabled by the read/write strobes. TRI-STATE® inverters are used to implement a scheme similar to *Figure 24*. This scheme has START and ALE accessed separately so that "double pulsing" isn't required.

Z80 is a trademark of Zilog.



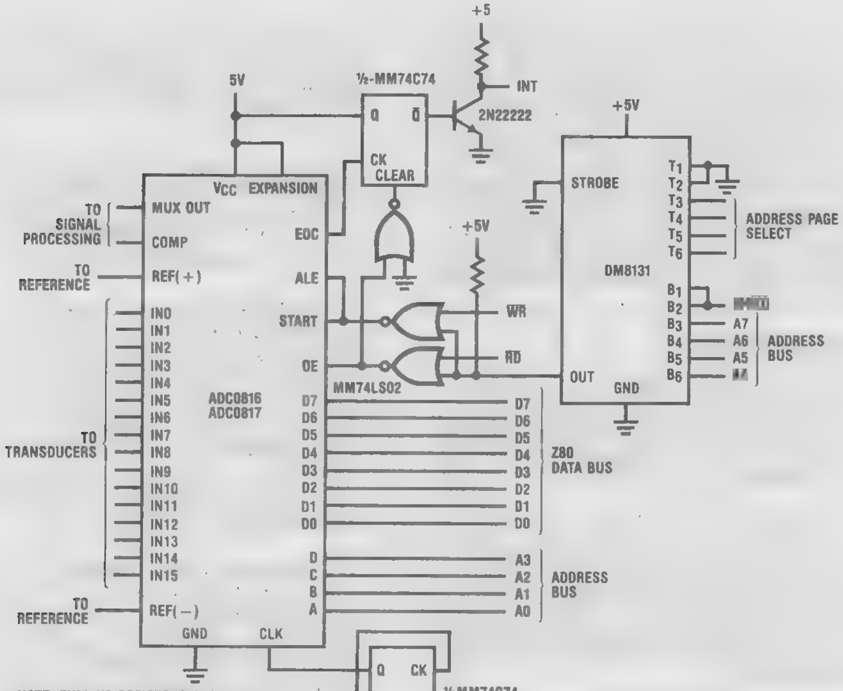
NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

Figure 24. Partial Address Decoding INS8080/8224/8228 to ADC0816/ADC0817



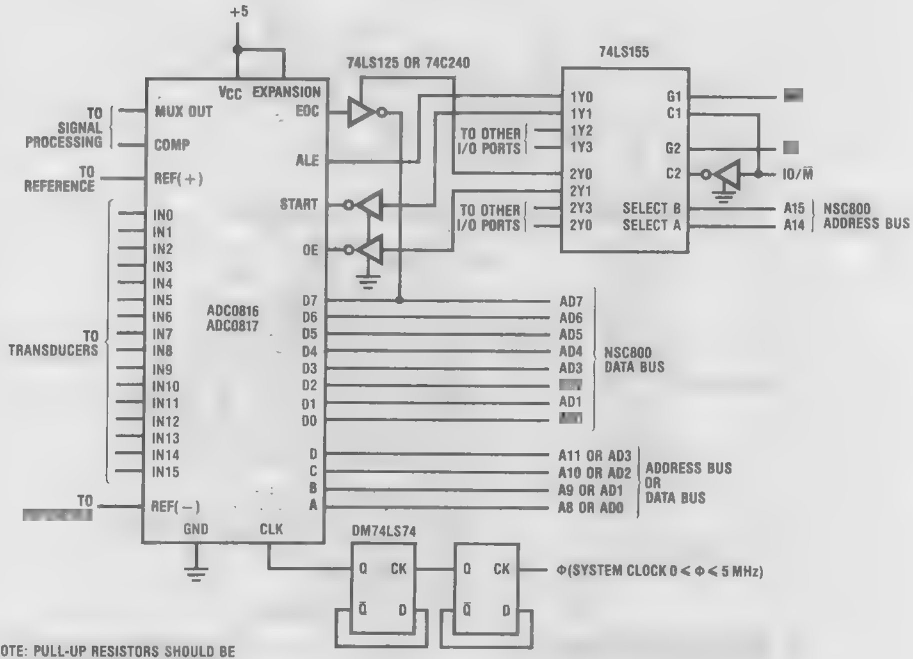
NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

Figure 25. Simple Z80 Interface to ADC0816/ADC0817



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

Figure 26. Decoded Z80 Interface



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

Figure 27. Partially Decoded NSC800 to ADC0816/ADC0817 Interface

The next design, *Figure 28,* uses the same simple NOR gating scheme as *Figure 23,* except the NSC800 control signals are slightly different. A simple interrupt scheme for EOC is employed using an MM74C74. When EOC goes high the flip-flop is set and $\overline{\text{INTR}}$ goes low. When the NSC800 acknowledges the interrupt by lowering $\overline{\text{INTA}}$, the flip-flop will reset. If more than one interrupt can occur simultaneously either $\overline{\text{INTA}}$ should be gated with EOC, or some other signal instead of $\overline{\text{INTA}}$ must be used. This is required since it is possible for the NSC800 to detect another interrupt and clear the ADC0816/ADC0817 interrupt before it's detected.

D. Interfacing to the 6800

The 6800 has no separate I/O addressing capabilities, so the system I/O must be addressed as though it is memory. As mentioned before, memory mapping can require more address decoding in order to separate memory from I/O, but in small systems very minimal parts count is still attainable.

Figure 29 illustrates an interface which uses a DM8131 comparator to partially decode the A12, A13, A14, and A15 address lines with the Φ_2 clock and Valid Memory Address (VMA), to provide an address decode pulse for the two NOR gates which in turn generate the START/ALE Pulse and the output enable signal. This design will locate the A/D in one 4k byte block.

This design tied EOC to $\overline{\text{IREQ}}$ interrupt through an inverter. This is only usable in single interrupt systems since the 6800 has no way of resetting this interrupt except by starting a new conversion. Since EOC is directly tied to the interrupt input, the controlling software must not re-enable interrupts until 8 converter clock periods after the START pulse when EOC is low.

The memory control signals are very different from the INS8080 type CPU's. One line indicates whether the operation is a read or write, R/$\overline{\text{W}}$ instead of separate read/write outputs on the INS8080/Z80/NSC800. This signal along with VMA indicate a valid read/write operation.

Figure 30 is slightly more complex, but provides more I/O port strobes. A NAND gate and inverter are used to decode the addresses, VMA and Φ_2 clock. The I/O addresses are located at 1110XXXXXAABBBB (Binary); where X = don't care; A = 00 (Binary) for ALE write or Data read and A = 01 for START write or IREQ reset/EOC read; and B = channel select address if A, B, C and D are connected to the address bus and ALE is accessed. A dual 2-4 line decoderis used to generate these strobes and inverters are used tocreate the correct logic levels.

The 6800 supports only a wired-OR interrupt structure. In a multi-interrupt environment only one interrupt is received and the interrupt handler routine must determine which deveice has caused the interrupt and service that device. (Although the INS8080/Z80/NSC800 can implement a similar structure, hardware interrupt controllers can also be used which will automatically vector the μP to the correct service routine.) To do this EOC is brought out to the data bus so the CPU can check it.

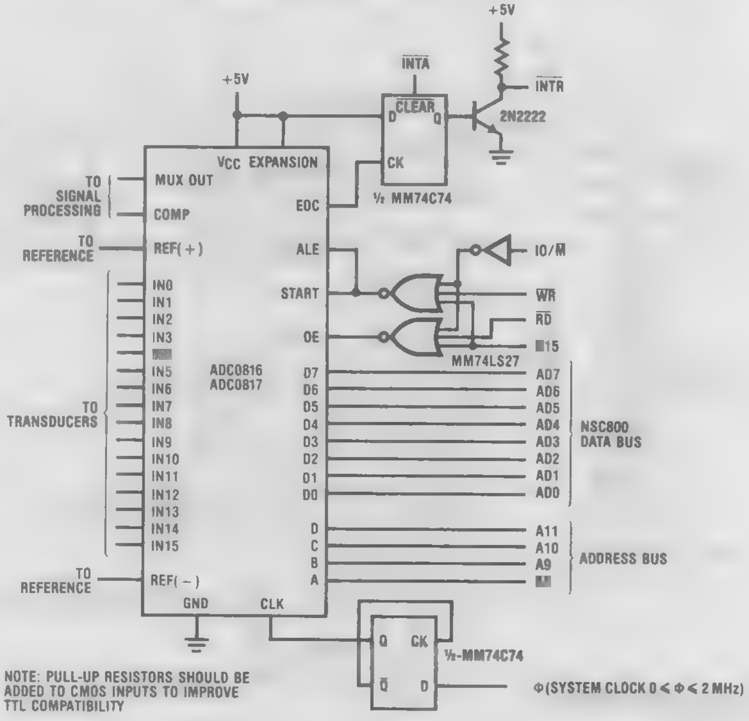


Figure 28. Minimal NSC800 to ADC0816/ADC0817 Interface

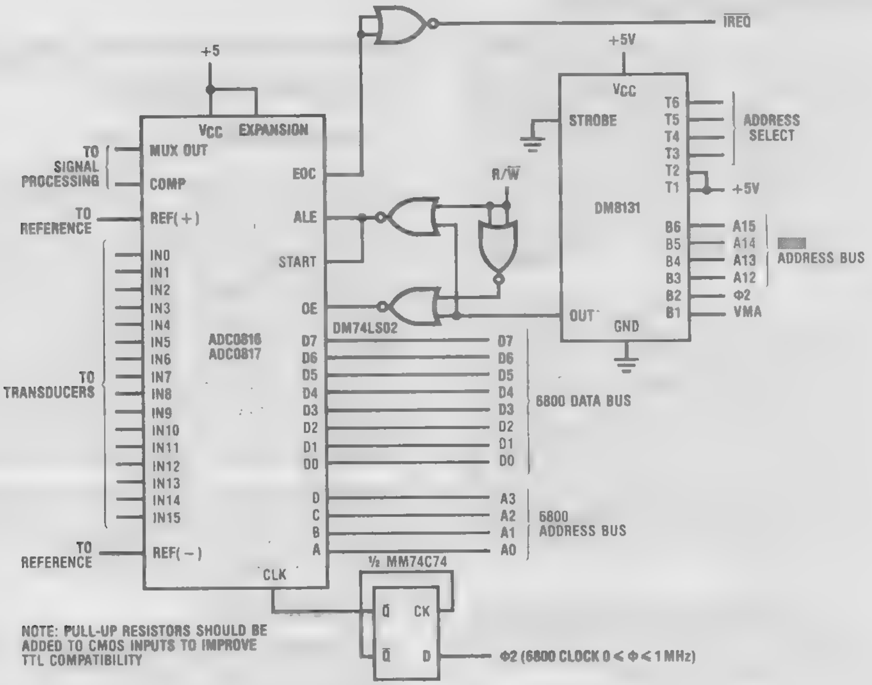


Figure 29. 6800 to ADC0816/ADC0817 Interface

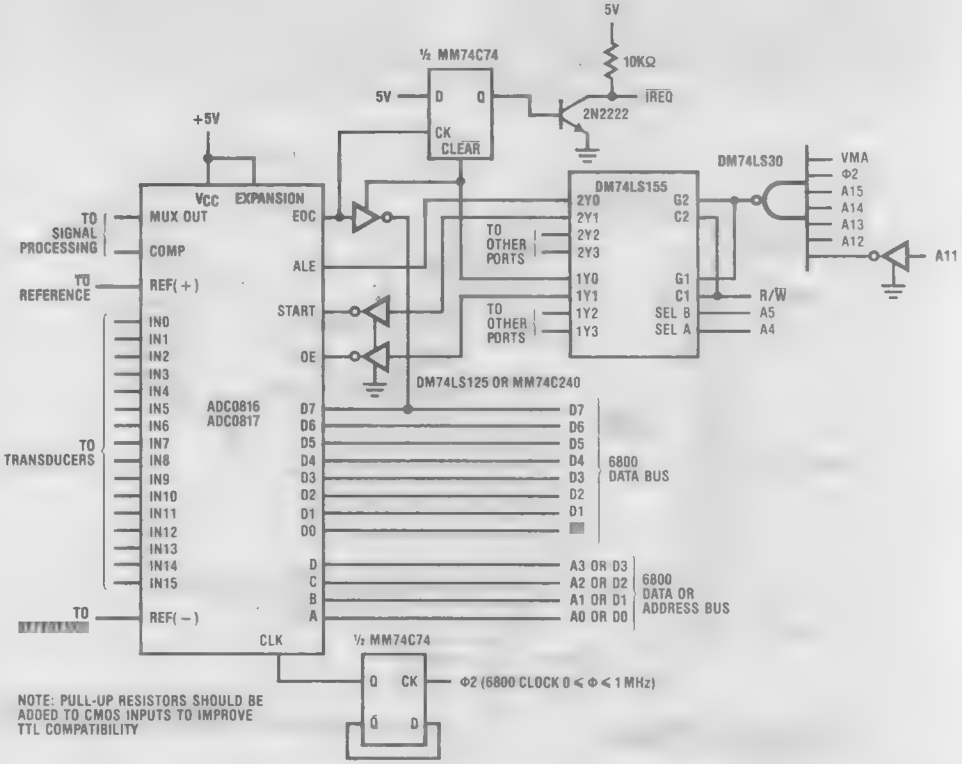


Figure 30. Partially Decoded 6800 to ADC0816/ADC0817 Interface

cessors have no separate I/O addressing thus all I/O ports must be memory mapped. The INS8060 has 12 bits of direct addressing (16 bits with paged addressing) and may require less decoding that a 16 bit µP when not using more than one page. The INS8070 has a 16 bit address bus and will have similar decoding requirements as the 6800, except that there are no equivalent Φ_2 or VMA signals.

Figure 31 shows an interface using the DM8131 bus comparator to decode A11–A6 address bits. The output of the DM8131 is gated with NRDS and NWDS to generate the START/ALE and OE strobes. START and ALE are tied together and should be pulsed twice to ensure a proper conversion. The EOC output is applied to the INS8060 SENSE A input. This input can be used as a polled input where its level can be determined by reading the µP status flag register. If the CPU's interrupt enable is set, then the SENSE A input becomes an active high interrupt input which will transfer control to the user's handler routine.

The INS8070 timing is very similar to the INS8060. Read ($\overline{\text{NRDS}}$) and write ($\overline{\text{NWDS}}$) enable lines are provided and since the INS8070 does not have separate I/O addressing, all I/O is memory mapped.

Figure 32 shows an interface where a DM74LS139 dual 2-4 decoder and DM74LS30 are used for address decoding. When $\overline{\text{NWDS}}$ is low, CPU writes to memory and 1Y0–1Y3 outputs will be decoded depending on A4 and A5 address lines. During a read operation $\overline{\text{NRDS}}$ will be low again enabling 1Y0–1Y3 outputs. The INS8070 also has SENSE inputs like the INS8060, inputs, SENSE A and SENSE B.

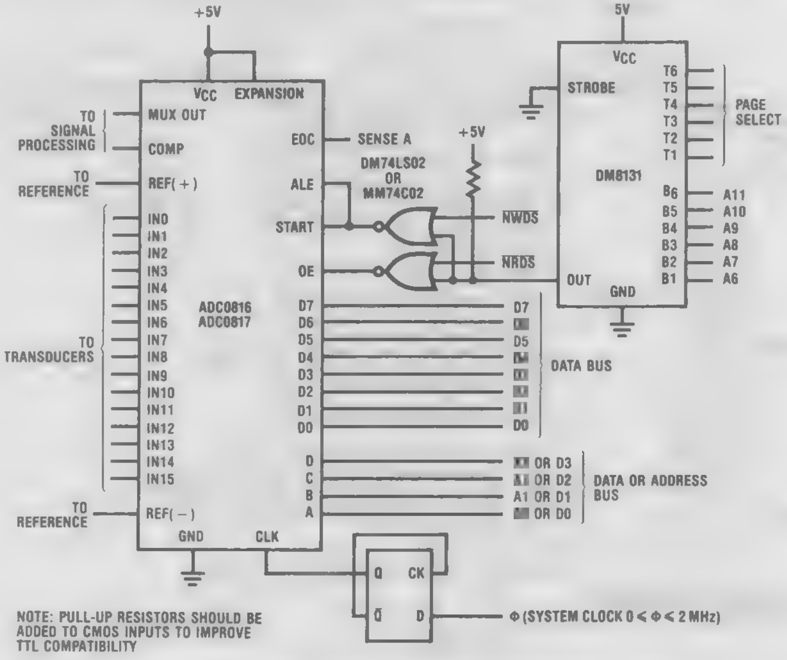
F. Parallel Interface Circuits

In some cases µP support chips can be used to interface the ADC0816/ADC0817 to microprocessors. Most parallel I/O chips can be used, and provide enough flexibility to enable all functions to be under software control. Typical parallel I/O chips that could be used are INS8255, 6820, Z80-PIO and others. Typically these support IC's would be connected directly to the data and control pins and the software would manipulate the START and ALE pins via the interface chip. In some cases the chips provide handshaking and/or interrupt capabilities which can ease the converter interface. In some cases, the interface circuits will not provide a clock, and therefore must be provided externally.

While use of parallel I/O circuits simplify designs and increase versatility, they are more expensive than the 1 or 2 SSI or MSI circuits that they would replace, and thus not always the best choice.

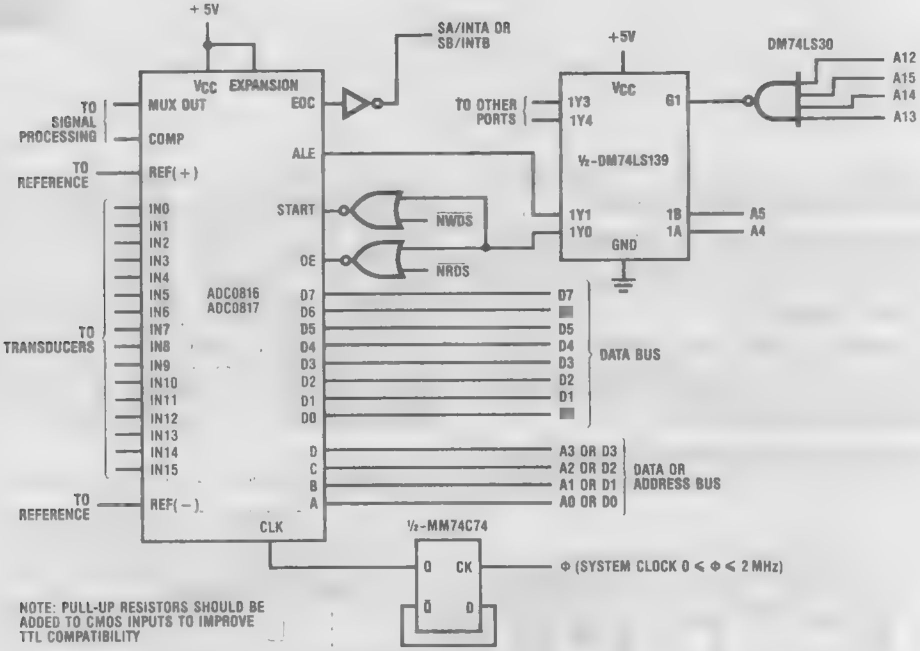
VI. Conclusion

The ADC0816/ADC0817 are easy to use general purpose A/D converters with the additional benefit of a 16 channel analog multiplexer. The IC's can become a simple standard 8-bit data acquisition circuit or the basis of a more powerful data acquisition system. Both integrated circuits provide features to enable easy microprocessor interface, yet also allow hardwired control logic to be used. In those applications which require less accuracy, the less expensive ADC0817 can be used to reduce overall system cost.



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

Figure 31. Simple INS8060 (SC/MP) to ADC0816/ADC0817



NOTE: PULL-UP RESISTORS SHOULD BE ADDED TO CMOS INPUTS TO IMPROVE TTL COMPATIBILITY

Figure 32. Simple INS8070 Interface to ADC0816/ADC0817

Digital Weight Scales

National Semiconductor
Carson Chen
March 1978

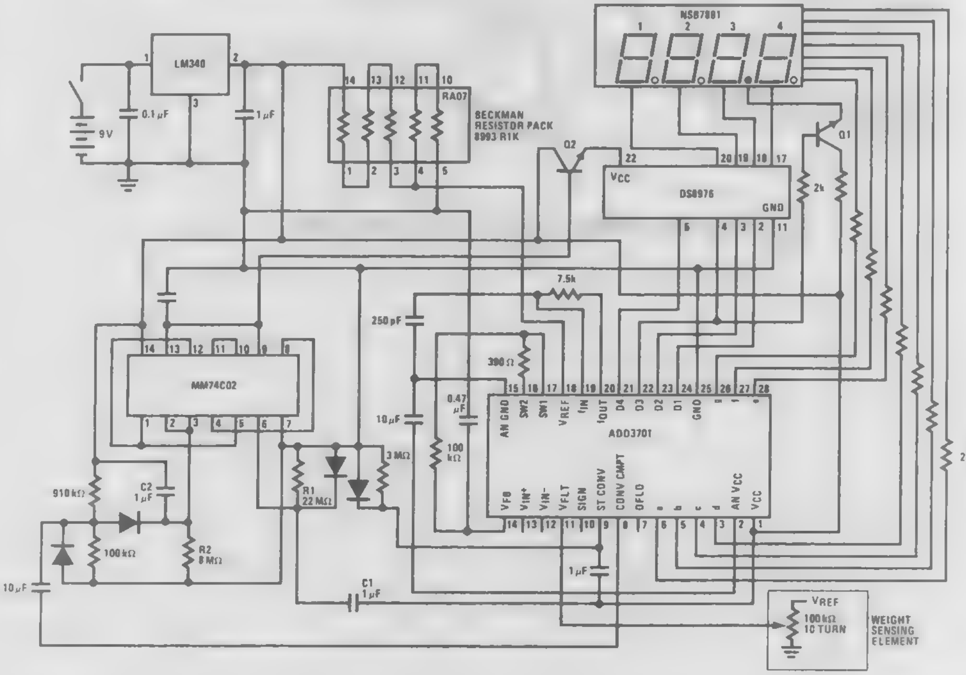
The application of digital systems to detect weight provides for low cost, accurate weight scales.

A developed system using the 3¾-digit DVM IC, ADD3701,* shown in figure 1, allows for conversion of an analog voltage to digital information linearly related to the weight being sensed.

Support circuitry for the DVM IC consists of a voltage regulator, a reference voltage, a weight sensing element, display drivers, and an LED display. Additional circuitry may be implemented for added features.

The weight scale circuit of figure 1 employs a potentiometer as the weight sensing element and functions as a variable voltage divider from ground to V_{REF}, 2 volts. An object placed upon the scale displaces the potentiometer wiper, which is connected to the scale mechanics, an amount proportional to its weight. Conversion of the wiper voltage to digital information is performed, decoded, and interfaced to the numeric display by the ADD3701. The LM340 regulates the V_{CC} supply voltage and the RA07 resistor array is connected as a voltage divider to generate the ADD3701 2V reference voltage. The NSB7881 is driven by the ADD3701 segment drivers and the DS8976 digit drivers.

*See ADD3701 data sheet for details of DVM operation.



Notes:

1. R1, C1 defines POWER ON display blanking interval. R2, C2 defines display ON time.
2. All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.
3. Display sequence for Rev A ckt implementation:

t = 0 sec	● power ON
t = 0 → 5 sec	● display blanked
	● system converging
t = 5 → 10 sec	● conversion complete
	● display ENABLE
t ⩾ 10 sec	● display blanked
	■ wait for new POWER UP cycle

Figure 1

Q2, the MM74C02 and surrounding circuitry generate the display sequence explained in Note 3 of figure 1.

The ADD3701 3¾-digit DVM displays a maximum of 3999 counts, full scale, having a resolution of 500 µV per LSD.

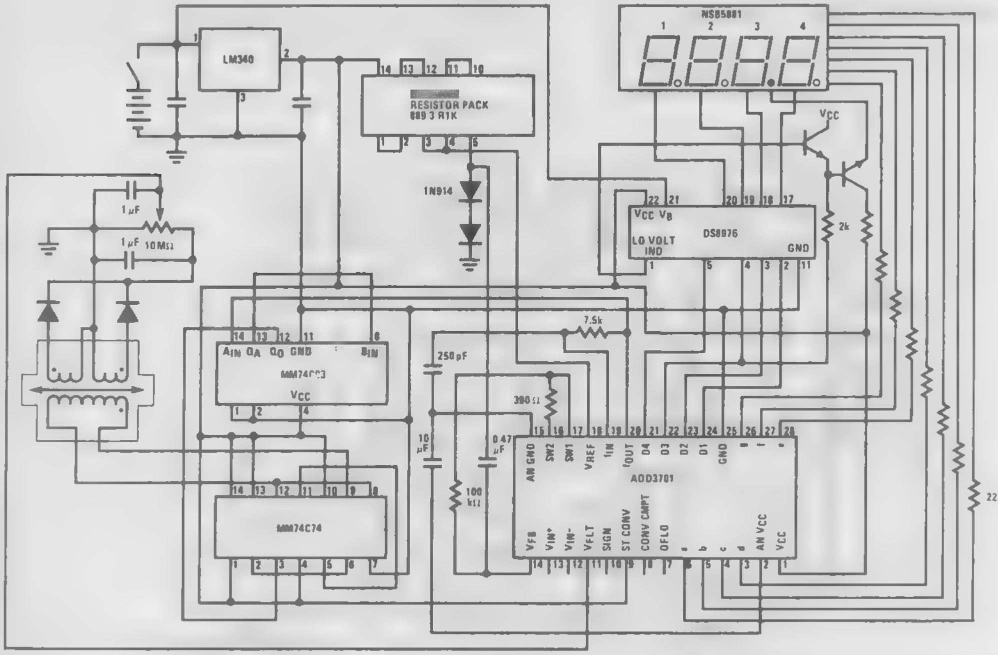
With the decimal point of digit 3 forced "ON" by Q1 the maximum displayed reading of figure 1 would equate to 399.9 units of weight.

Figure 2 is a weight scale sensor similar to that in figure 1, differing only in the weight sensing element and its related support circuitry.

The transformer of figure 2 is rectified to a DC voltage, proportional to a weight displacement, and then converted to its digital equivalent with the ADD3701.

The purpose of setting analog ground two diode drops above digital ground is to help cancel the inherent air coupling offset voltage generated by the transformer.

Figure 2 is also connected to display a maximum of 399.9 units of weight. The accuracy of both systems without the transducer elements is ±1 LSD at 25°C ± 15°C.



Notes:

1. Excitation to the LVDT (i.e., outputs of the MM74C93 and MM74C74) may be altered to compensate for the varying frequency ranges of LVDTs.
2. All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.

Figure 2

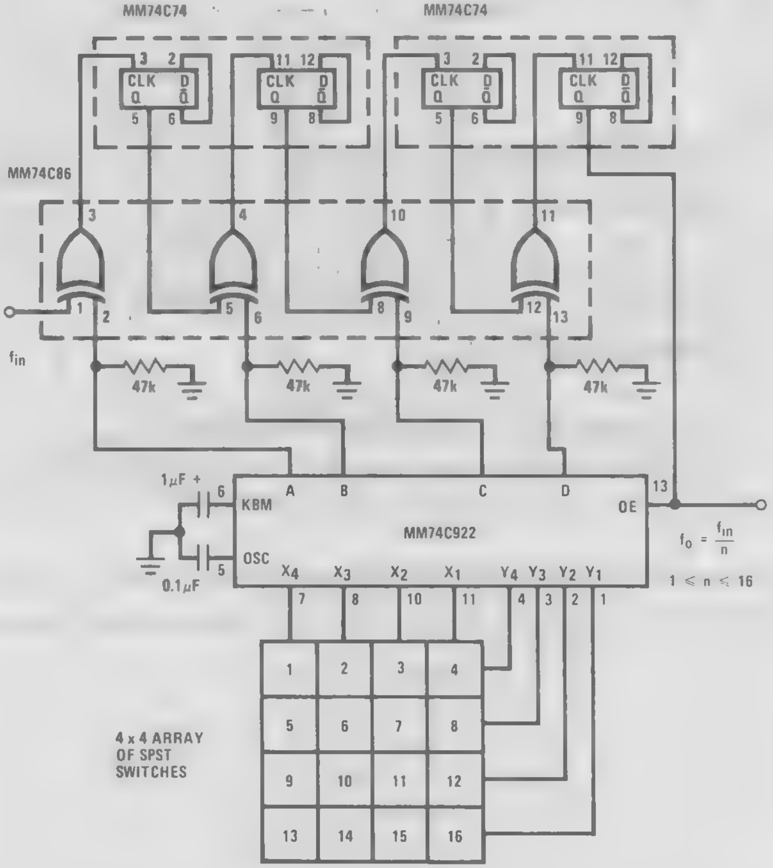
Keyboard Programmable Divide-by-N Counter with Symmetrical Output — DB-5

Keyboard Programmable Divide-by-N Counter with Symmetrical Output

National Semiconductor
Digital Brief 5
Gerald Buurma

A CMOS key encoder combines with a couple of Dual D flip-flops and an exclusive OR package to form a simple but versatile programmable divider. The input frequency can be divided by any number n between 1 and 16 by simply pressing the appropriate key. The counter output is symmetrical for both odd and even divisors.

This circuit is useful for simple frequency synthesis or as an oscilloscope triggering unit where the displayed signal is applied to the counter input and the external trigger of the oscilloscope is connected to the counter output. The trigger signal is then some submultiple of displayed signal which often results in a more stable trace. Different divisors can be easily keyed in as the input signal varies.



Simply press the key and the input frequency is divided by that number. The output frequency is symmetrical for odd and even divisors. Use it for simple frequency synthesis or as a keyboard controlled oscilloscope triggering unit.

The key encoder scans the key array which is set up so the key labeled "16" is in the matrix position which causes "0" to be encoded, the key labeled "15" causes "1" to be encoded, and so on until we find that the key position labeled "1" causes a binary "15," or all ones, at the output of the encoder. The key arrangement converts a key position so that any number n from 1 to 16 is encoded as 16 – n at the encoder output. For example, if the key labeled 5 is pressed the binary number 1011 = 11 appears at the encoder output. The MM74C922 key encoder scans the keys, detects, debounces, and encodes any entry. An internal register remembers the last key pressed and presents it to the Tri-State® outputs.

The input to the exclusive OR is a "zero" when the respective encoder output is a "zero" or when the feedback signal from the last counter stage forces the encoder outputs into Tri-State. When in Tri-State the pull down resistors feed a "zero" into the exclusive OR inputs.

When the output is an active "one," the clock signal from one flip-flop to the next is inverted by the exclusive ORs. When the output is a "zero" or the encoder is in Tri-State, due to the feedback signal, the clock signal from one flip-flop to the next is the same phase. For every n/2 input time period, the counter output and feedback change state. Whenever the feedback signal changes state, all flip-flops programmed with a "one" by the encoder change their phases; this effectively adds a clock pulse to that stage of the counter. The addition of clock pulses to the 2^0, 2^1, 2^2 or 2^3 stages allows us to divide by any number between 1 and 16. Since the feedback changes state every n/2 input time period, the output frequency is symmetrical for any divisor.

The unit operates over the standard CMOS supply range of 3 to 15 volts and has a typical upper frequency limit of one megacycle with a 10 volt supply.

REFERENCE

1. M. V. Subba Rao, "Programmable Divide by n Counter Provides Symmetrical Outputs for all Divisors," *Electronic Design*, no. 2, January 19, 1976, p. 82.

MM54C/MM74C Voltage Translation/Buffering

National Semiconductor
Memory Brief 18
John Jorgensen
Thomas P. Redfern

INTRODUCTION

A new series of MM54C/MM74C buffers has been designed to interface systems operating at different voltage levels. In addition to performing voltage translation, the MM54C901/MM74C901 through MM54C904/MM74C904 hex buffers can drive two standard TTL loads at $V_{CC} = 5V$. This is an increase of ten times over the two LpTTL loads that the standard MM54C/MM74C gate can drive. These new devices greatly increase the flexibility of the MM54C/MM74C family when interfacing to other logic systems.

PMOS TO CMOS INTERFACE

Since most PMOS outputs normally can pull more negative than ground, the conventional CMOS input diode clamp from input to ground poses problems. The least of these is increased power consumption. Even though the output would be clamped at one diode drop (−0.6V), all the current that flows comes from the PMOS negative supply. For TTL compatible PMOS this is −12V. A PMOS output designed to drive one TTL load will typically sink 5 mA. The total power per TTL output is then 5 mA x 12V = 60 mW. The second problem is more serious. Currents of 5 mA or greater from a CMOS input clamp diode can cause four-layer diode action on the CMOS device. This, at best, will totally disrupt normal circuit operation and, at worst, will cause catastrophic failure.

To overcome this problem the MM74C903 and MM74C904 have been designed with a clamp diode from inputs to V_{CC} only. This single diode provides adequate static discharge protection and, at the same time, allows voltages of up to −17V on any input. Since there is essentially no current without the diode, both the high power dissipation and latch up problems are eliminated.

To demonstrate the above characteristics, *Figures 1, 2, and 3* show typical TTL compatible PMOS circuits driving standard CMOS with two clamp diodes, TTL compatible PMOS driving MM74C903/MM74C904, and the TTL compatible PMOS to CMOS system interface, respectively.

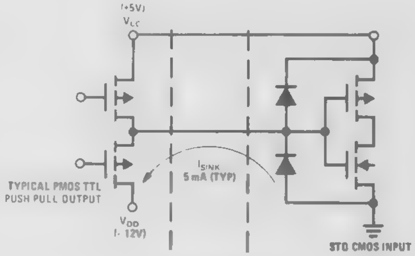


FIGURE 1.

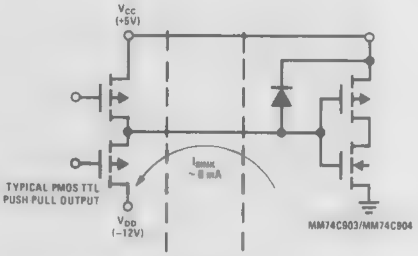
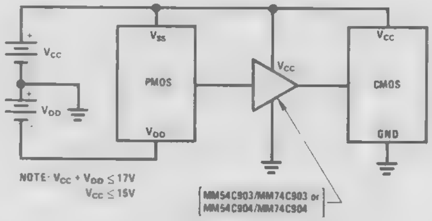


FIGURE 2.



NOTE: $V_{CC} + V_{DD} \leq 17V$
$V_{CC} \leq 15V$

FIGURE 3. PMOS to CMOS or TTL Interface

CMOS TO CMOS OR TTL INTERFACE

When a CMOS system which is operating at V_{CC} = 10V must provide signals to a CMOS system whose V_{CC} = 5V, a problem similar to that found in PMOS-to-CMOS interface occurs. That is, current would flow through the upper input diode of the device operating at the lower V_{CC}. This current could be in excess of 10 mA on a typical 74C device, as shown in *Figure 4.* Again, this will cause increased power as well as possible four layer diode action.

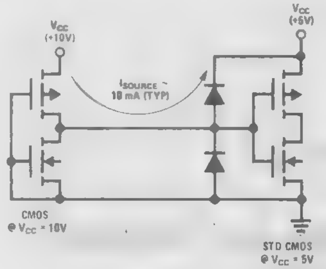


FIGURE 4.

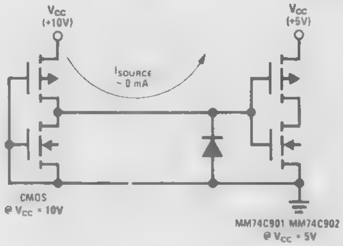
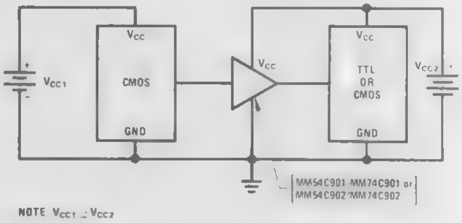


FIGURE 5.

Using the MM74C901 or MM74C902 will eliminate this problem. This occurs simply because these parts are designed with the upper diode removed, as shown in *Figure 5.* With this diode removed the current being sourced goes from about 10 mA to the leakage current of the reverse biased input diode.

Since the MM74C901 and MM74C902 are capable of driving two standard TTL loads with only normal input levels, the output can be used to directly drive TTL. With the example shown, the inputs of the MM74C901 are in excess of 5V. Therefore, they can drive more than two TTL loads. In this case the device would drive four loads with V_{IN} = 10V. If the MM74C902 were used, the output drive would not increase with increased input voltage. This is because the gate of the output n-channel device is always being driven by an internal inverter whose output equals that of V_{CC} of the device.

The example used was for systems of V_{CC} = 10V on one system and V_{CC} = 5V on the second, but the MM74C901 and MM74C902 are capable of using any combination of supplies up to 15V and greater than 3V, as long as V_{CC1} is greater than or equal to V_{CC2} and grounds are common. *Figure 6* diagrams this configuration.



V_{CC1}
V_{CC}
CMOS
GND
V_{CC}
V_{CC}
TTL OR CMOS
GND
V_{CC2}
MM54C901 MM74C901 or MM54C902/MM74C902
NOTE $V_{CC1} \geq V_{CC2}$

FIGURE 6. CMOS to TTL or CMOS at a Lower V_{CC}

The inputs on these devices are adequately protected with the single diode, but, as with all MOS devices, normal care in handling should be observed.

Section 9

Ordering and Package Information

Ordering Information

MM74C Series

Order Number	Package	Temperature Range
MM74CXXN	Molded DIP (N)	−40°C to +85°C
MM74CXXJ	Cavity DIP (J)	−40°C to +85°C
MM54CXXJ	Cavity DIP (J)	−55°C to +125°C
MM54CXXD	Cavity DIP (D)	−55°C to +125°C
MM54CXXW	Cavity Flat Pack (W)	−55°C to +125°C
MM80CXXN	Molded DIP (N)	−40°C to +85°C
MM80CXXJ	Cavity DIP (J)	−40°C to +85°C
MM70CXXJ	Cavity DIP (J)	−55°C to +125°C
MM70CXXD	Cavity DIP (D)	−55°C to +125°C
MM70CXXW	Cavity Flat Pack (W)	−55°C to +125°C

CD4000 Series

Order Number	RCA Equivalent Designation	Motorola Equivalent Designation	Package	Temperature Range
CD40XXCN	CD40XXAE	MC140XXCP	Molded DIP (N)	−40°C to +85°C
CD40XXCJ	CD40XXAY	MC140XXCL	Cavity DIP (J)	−40°C to +85°C
CD40XXMJ	CD40XXAF	MC140XXAL	Cavity DIP (J)	−55°C to +125°C
CD40XXMD	CD40XXAD		Cavity DIP (D)	−55°C to +125°C
CD40XXMW	CD40XXAK		Cavity Flat Pack (W)	−55°C to +125°C
CD40XXBCN	CD40XXBE	MC140XXBCP	Molded DIP (N)	−40°C to +85°C
CD40XXBCJ	CD40XXBY	MC110XXBCL	Cavity DIP (J)	−40°C to +85°C
CD40XXBMJ	CD40XXBF	MC140XXBAL	Cavity DIP (J)	−55°C to +125°C
CD40XXBMD	CD40XXBD		Cavity DIP (D)	−55°C to +125°C
CD40XXBMW	CD40XXBK		Cavity Flat Pack (W)	−55°C to +125°C
*CD40XXCN	CD45XXBE	MC145XXBCP	Molded DIP (N)	−40°C to +85°C
*CD45XXCJ	CD45XXBY	MC145XXBCL	Cavity DIP (J)	−40°C to +85°C
*CD45XXMJ	CD45XXBF	MC145XXBCP	Cavity DIP (J)	−55°C to +125°C
*CD45XXMD	CD45XXBD		Cavity DIP (D)	−55°C to +125°C
*CD45XXMW	CD45XXBK		Cavity Flat Pack (W)	−55°C to +125°C

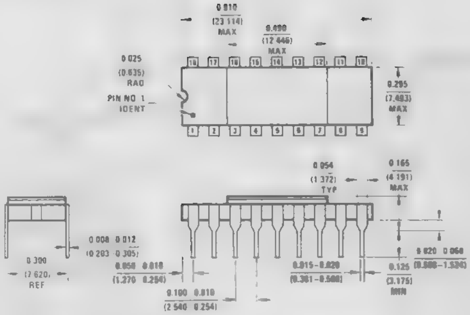
*Equivalent to Motorola MC145XX Series

Dual-in-Line Packages

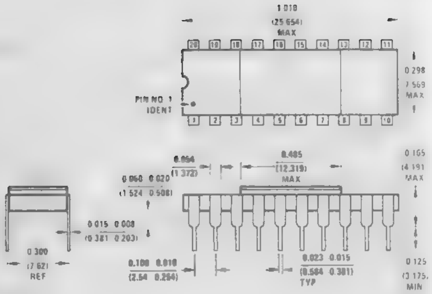
(N) Devices ordered with the "N" suffix are supplied in plastic molded dual-in-line packages. Molding material is a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is copper or alloy 42 with a hot solder dipped surface to allow ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in cer-dip packages (ceramic lid and base sealed with a high temperature vitreous glass). Lead material is solder dipped alloy 42.

(D) Devices ordered with the "D" suffix are supplied in side braze, multi-layered ceramic dual-in-line packages. The leads are Kovar or alloy 42 and either tin-plated, gold-plated, or solder-plated.



18-Lead Hermetic Dual-In-Line Package (D)
NS Package Number D18A



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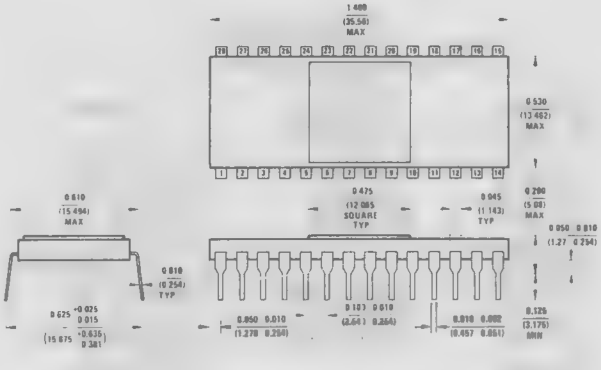
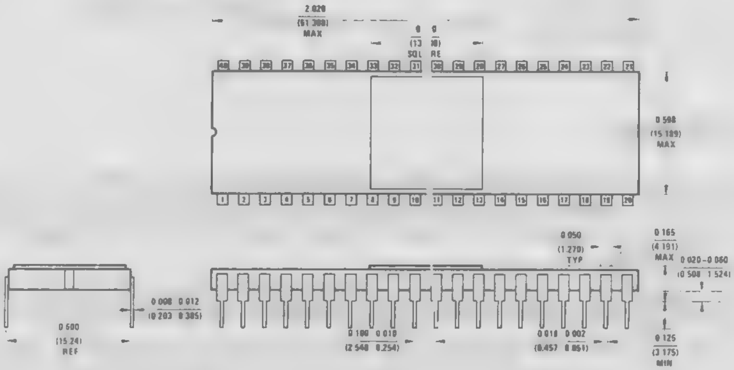


28-Lead Hermetic Dual-In-Line Package (D)
NS Package Number D28A



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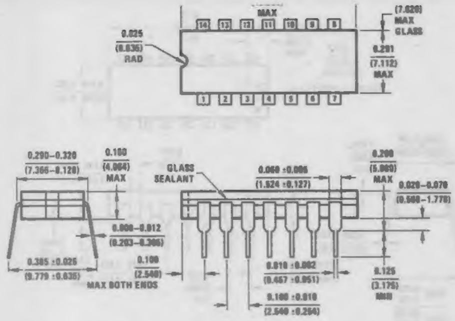
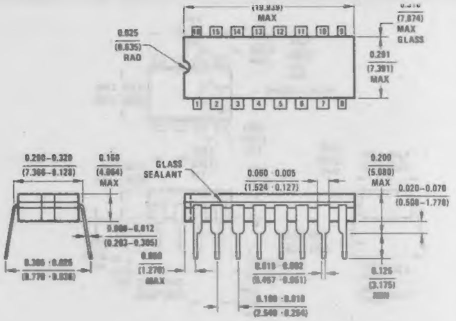
NS Package Number D40C



14-Lead Hermetic Dual-In-Line Package (J)
NS Package Number J14A



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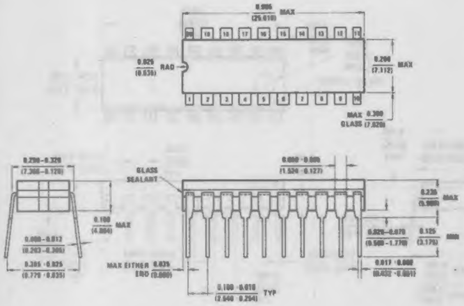

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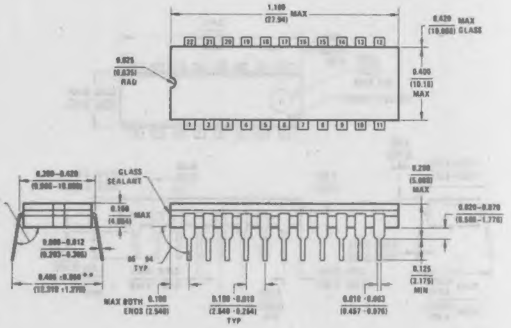

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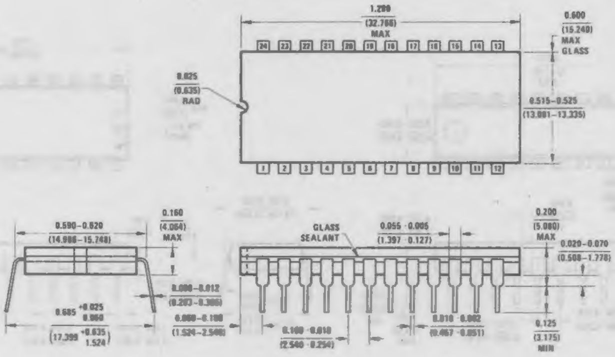

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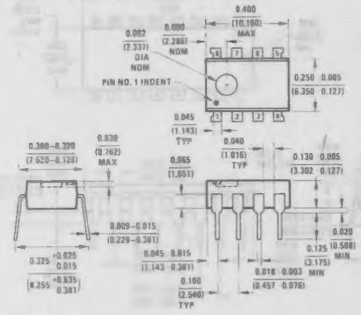

8-Lead Molded Mini Dual-In-Line Package (N)
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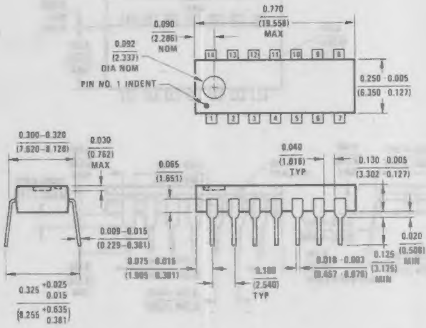

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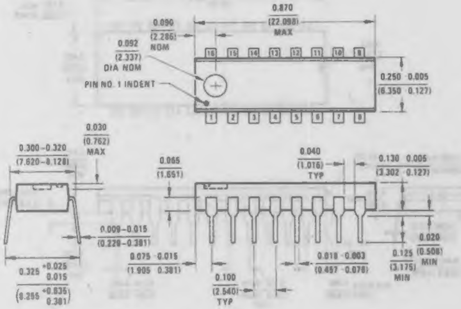

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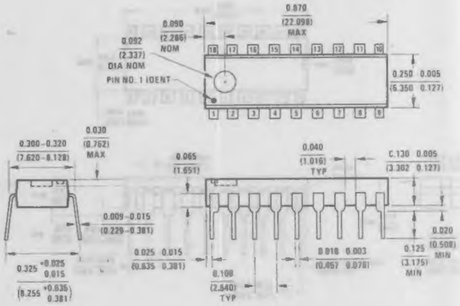

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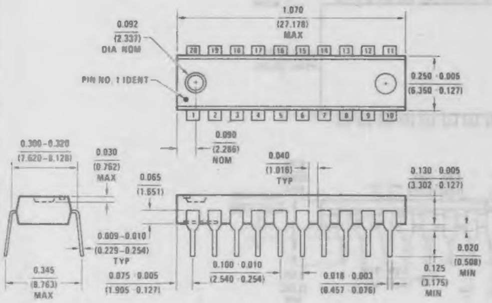

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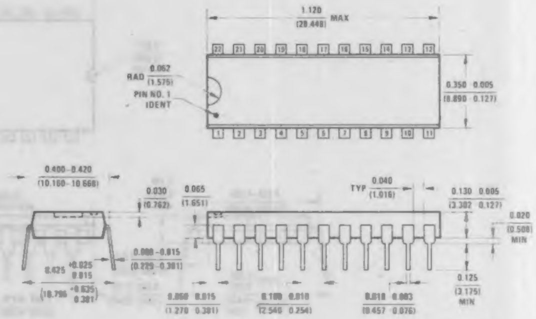

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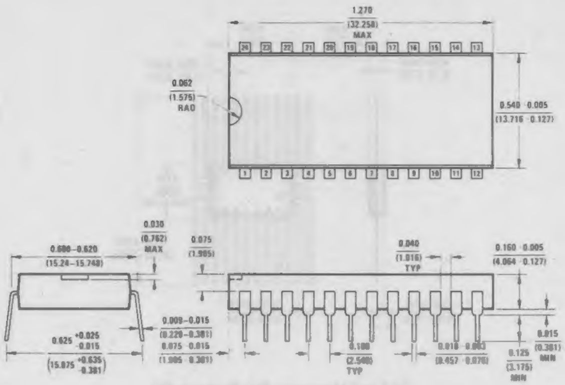

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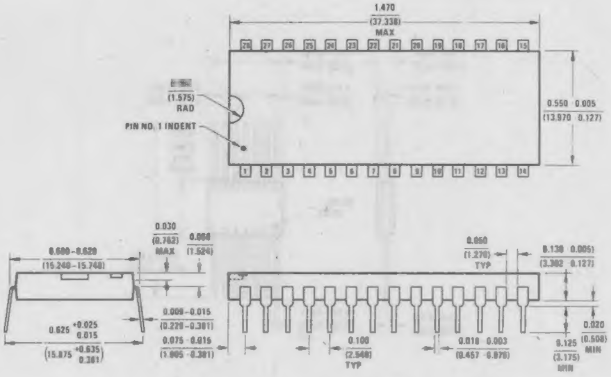

28-Lead Molded Dual-In-Line Package (N)
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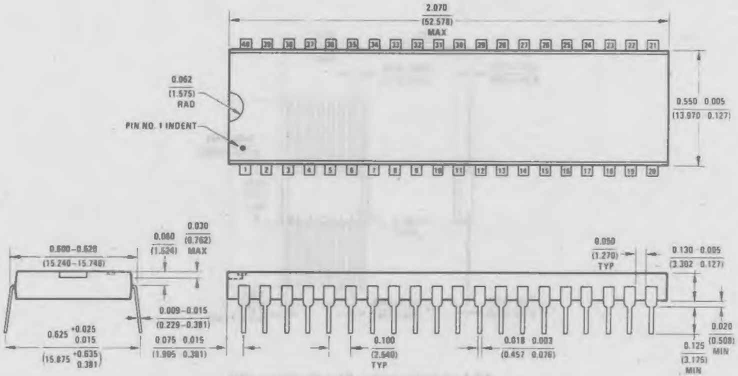

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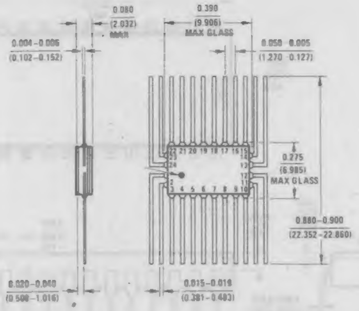
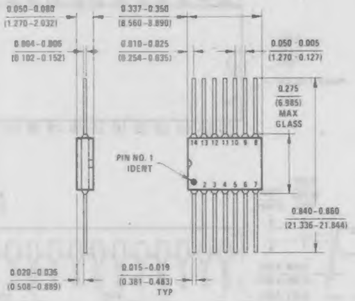


24-Lead Hermetic Flat Package (F)
NS Package Number F24A



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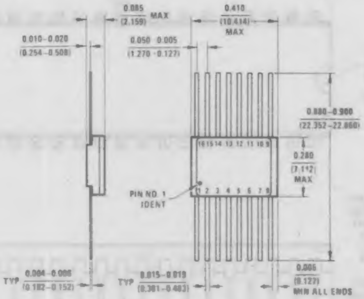

16-Lead Hermetic Flat Package (W)
NS Package Number W16A